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Feasible device architectures for ultra-scaled CNTFETs

Anibal Pacheco-Sanchez, Florian Fuchs, Sven Mothes, Andreas Zienert, Jörg Schuster, Sibylle Gemming and Martin Claus

***Abstract*—Feasible device architectures for ultra-scaled CNTFETs are studied down to $5.9\,\mathrm{nm}$ using a multiscale simulation approach covering electronic quantum transport simulations and TCAD numerical device simulations. Schottky-like and ohmic-like contacts are considered. The simplified approach employed in the numerical device simulator is critically evaluated and verified by means of comparing the results with electronic quantum simulation results of an identical device. Different performance indicators such as the switching speed, switching energy, the subthreshold slope, $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio, among others, are extracted for different device architectures. These values guide the evaluation of the technology for different application scenarios. For high-performance logic applications, the buried gate CNTFET is claimed to be the most suitable structure.**

***Index Terms*—CNTFET, multiscale modeling, atomistic simulation, electronic quantum simulation, TCAD, channel scaling, $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio, subthreshold slope, switching characteristics.**

I. Introduction

The semiconductor industry has been facing a major challenge since the silicon-based semiconductor technology has come close to reaching its technological and device performance limits, while still trying to push the system performance forward [1]. One potential solution for further improving the performance already at the device level is the replacement of the silicon channel by a different semiconducting material, such as carbon nanotubes (CNTs). The corresponding CNT field-effect transistors (CNTFETs) have been predicted to outperform silicon FETs [2]-[4]. Due to their predicted linear characteristic, CNTFETs are especially interesting for analog high-frequency applications [5]-[9]. In addition to this, it is argued in [12] and [13] that CNTFETs are well suited for high-performance logic applications because of the high carrier velocity and quasi-ballistic transport [14], [15]. From a technology point of view, the reduced device footprint of CNTFETs is another improved feature in comparison to silicon-based transistors.

The aim of this work is to study and evaluate feasible device architectures for ultra-scaled CNTFETs by analyzing the device performance and comparing it with state-of-the-art experimental results. Numerical device simulations (NDSs) as well as electronic quantum transport simulations (EQSs) are two methods with potential for exploring feasible device architectures. NDS is capable of describing the behaviour of CNTFETs with large dimensions considering the overall device electrostatics and the overall device footprint within an acceptable time for engineering purposes. This allows also the description of high-performance CNTFETs [7]. However, as NDS does not treat the CNTFETs at an atomistic level, simple parameterized models are required to describe e.g. the band structure of the simulated CNTs. The description of the physics near the contacts of the device must be done thoughtfully in NDS [10], whereas it could intrinsically been considered in EQS [11].

NDS can be calibrated by adjusting the model parameters either to experimental data or to simulation data of more fundamental methods, such as EQS. In this work, the latter approach has been used. The core functionality of the NDS is tested critically, which can be the base of future improvements towards a closer physical description of CNTFETs, while keeping the numerical efficiency and minor simulation times of the NDS approach.

II. Simulation methods

In this work, EQS is based on the non-equilibrium Green's functions formalism in combination with the extended Hückel theory (EHT) as it has been implemented in the Atomistix ToolKit [16]-[19]. The simulation setup consists of two semi-infinite leads and a central region as shown in [20]. The gate electrode is modeled by a fixed potential. Neumann boundary conditions are used in the spacer regions. Dirichlet boundary conditions are used in the electrode region to shield the electrostatics from the boundary conditions. The parameter set presented in [21] has been used in this work in order to describe the shape of the the band structure of the CNT with density functional theory (DFT)-like accuracy. EQSs using this parameter set for CNTs with metal contacts have been demonstrated in [20]. The mesh cutoff, which determines the degree of fineness of real-space grids, is set to $272.11\,\mathrm{eV}$. The Brillouin zone is sampled by 25 k-points in the transport direction.

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The required parameters for the description of the CNT within NDS, such as effective mass and band edge energies, are extracted from DFT calculations. Here, a mesh cutoff of $2040.85\,\mathrm{eV}$, a k-point sampling of $50 \times 1 \times 1$ and an expanded wave function in a double-zeta plus polarization (DZP) basis is used.

The employed numerical device simulator has been described in [22]. It provides a self-consistent solution of the one-dimensional effective-mass Schrödinger equation and the three-dimensional Poisson equation. The simulator has been successfully verified with experimental data taken from [24] and [25] in [7], [22] and [35]. For the NDS included in this study, only the first 2 conduction subbands and the first 2 valence subbands have been considered since detailed previous studies reveal the first two subbands to dominate the transport [22], [23].

The main difference in both simulation methods is the contact modeling. In EQS, the properties of the contacts are calculated based on the atomic coordinates using EHT. By doing so, all bands and thus the complete density of states of the CNT, as well as the 3D electrostatic potential, are considered. In contrast, in the NDS, the effective mass and the band edges are used to describe the transport properties. In this work, the corresponding model parameters for the contact description in NDS, i.e., the band alignment of the subbands, are extracted from the local density of states calculated with EQS.

III. NDS RELIABITY

A. Comparison with EQS

1) Simulated device structure: In order to compare the simulation methods, EQS and NDS are applied to the same simplified *n*-type gate-all-around (GAA) CNTFET with the physical dimensions shown in Fig. 1 to meet the simulation constraints of the employed electronic quantum transport simulator in terms of possible device architectures. The channel is a (16,0) CNT with a diameter d_{CNT} of $1.25\,\mathrm{nm}$, a similar diameter as used in recent experiments involving short CNTFETs [25]. The diameter is also big enough to reduce the impact of curvature effects [26]. Default values of channel length L_{ch} and gate length L_{g} are $10.2\,\mathrm{nm}$ and $5.9\,\mathrm{nm}$, respectively. The length between each contact and gated CNT portions, known as spacer length L_{sp}, is then equal to $2.15\,\mathrm{nm}$. The Schottky barrier height for electrons (holes) is set to $0.02\,\mathrm{eV}$ ($-0.58\,\mathrm{eV}$), which have been extracted from the local density of states in EQS.

In EQS, drain and source contacts are n-doped. A doping concentration of 0.05 electron per contact cell, corresponding to 5.86×10^{-2} electrons/nm, is chosen for each contact. This doping concentration shifts the Fermi level close to the conduction band edge in the EQS. It has been assumed that doping affects the Fermi energy level but not the effective mass. Similar doping type and Schottky barrier height is expected for Cr contacted CNTs [11]. In NDS, the band edges have been fitted to the ones from EQS and the simulation boundaries are set directly at the interfaces between the coated and uncoated CNT portions.

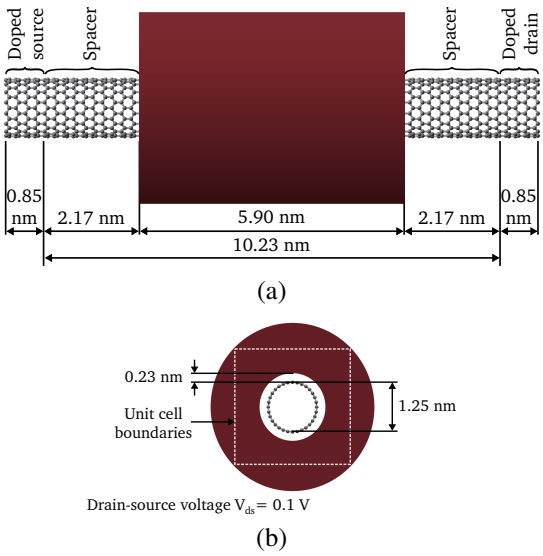

Fig. 1. (a) Cross sectional view and (b) frontal view of the gate all-around CNTFET used for EQS and NDS. Gate and channel lengths are modified along this study. Device dimensions shown here are approximated to two digits after the decimal point.

The distance between the Fermi energy and the first and second conduction (valence) subband is set to $0.30\,\mathrm{eV}$ and $0.62\,\mathrm{eV}$ ($0.30\,\mathrm{eV}$ and $0.56\,\mathrm{eV}$), respectively. The effective mass of injected carriers is set to $0.06m_{\mathrm{e}}$ ($0.06m_{\mathrm{e}}$) for the first conduction (valence) subband and to $0.26m_{\mathrm{e}}$ ($0.23m_{\mathrm{e}}$) for the second conduction (valence) subband, where m_{e} represents the electron rest mass. These values have been extracted from the DFT band structure.

Vacuum padding between CNT and gate is implemented since no current flow from the gate to the CNT is considered, thus, reducing the computational burden for the EQS. The separation between CNT and gate material corresponds to an equivalent oxide thickness of $0.9\,\mathrm{nm}$. The drain-to-source voltage V_{DS}, used for the studies in this section is set to $0.1\,\mathrm{V}$.

2) Device performance in different bias regions: Fig. 2(a) shows the transfer characteristic of the $5.9\,\mathrm{nm}$-GAA CNTFET obtained from EQS and NDS using the default parameters described above. The device shows ambipolar behavior. A similar analysis as the one presented in [27] for a slightly larger device can be derived here for the different bias regions identified as follows: region (i) for $V_{\mathrm{GS}} > -0.1\,\mathrm{V}$ at which the device is considered to be in on-state, region (ii) for $-1.2\,\mathrm{V} < V_{\mathrm{GS}} < -0.1\,\mathrm{V}$ at which the off-state is found, and region (iii) for $V_{\mathrm{GS}} < -1.2\,\mathrm{V}$ at which another increase of the current can be seen. In each of these bias regions, different transport mechanisms contribute to the corresponding current. This can be understood from Figs. 2(b) and 3 where the band diagram and the transmission spectrum T are shown for representative bias points. Notice that the transmission from EQSs inside the band gap region is only non-zero due to numerical reasons and these contributions are too small to influence the calculated currents.

In region (i), the transmission of electrons into the channel is enabled by the low potential barrier formed in this bias region

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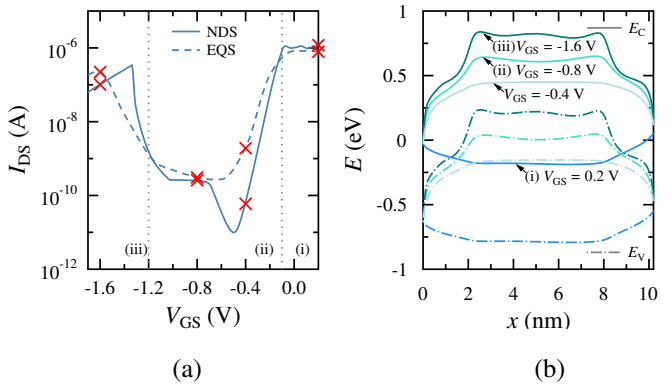

Fig. 2. (a) Transfer characteristic of an n-type GAA CNTFET with a gate length of 5.9 nm at $V_{DS} = 0.1$ V. Solid line: results from the numerical device simulator, dashed line: results from electronic transport simulations. Markers represent the voltages at which the band profile and the transmission spectrum are analyzed from both simulation results. (b) Band profile of the same device obtained with NDS for representative bias points in each bias region.

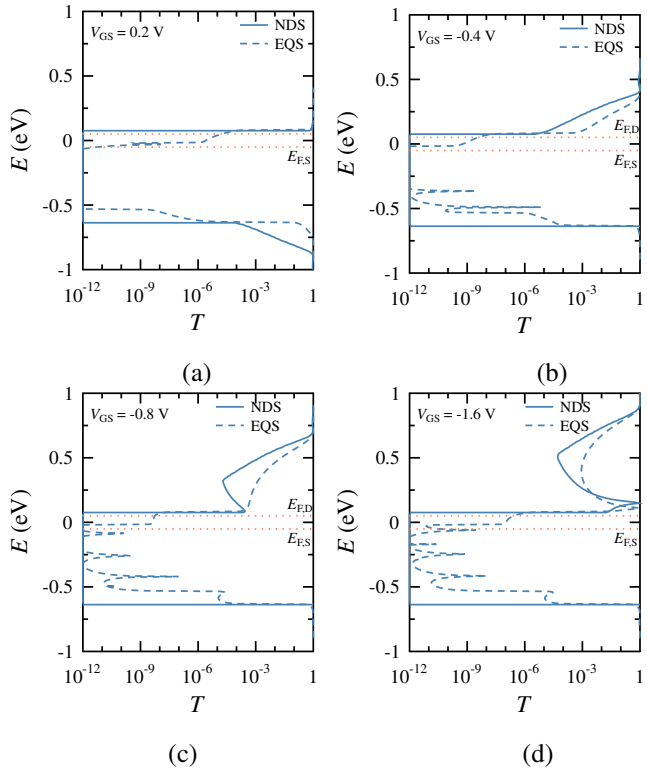

Fig. 3. Transmission spectra for the 5.9 nm-GAA CNTFET calculated with NDS (solid lines) and EQS (dashed lines) at three different bias regions defined in the text: (a) region (i), (b) and (c) region (ii) and (d) region (iii). The Fermi energies of source ($E_{F,S}$) and drain ($E_{F,D}$) contacts are marked as horizontal dashed lines.

as shown in Fig. 2(b), leading to a thermionic current. The high value of the electron transmission probability in region (i) close to the Fermi energy level at the source can be seen in Fig. 3(a). The on-state current $I_{on} = I_{DS}|_{V_{GS}=V_{DS}=0.1\,V}$ is 0.80 µA for the EQS results and 0.95 µA for the NDS results.

The representative band diagram for region (ii) at $V_{GS} = -0.8$ V presented in Fig. 2(b) shows that tunneling is not possible and thermionic emmision occurs only at higher energies as shown in Fig. 3(b), thus the transistor can be considered as switched-off. In this bias range the average value of the current is less than 1×10^{-8} A. NDS results show a dip in the transfer characteristic which is not present in EQS results. From the transmission spectra in the off-state at $V_{GS} = -0.4$ V shown in Fig. 3(b) it can be concluded that the transmission probability calculated by EQS is larger than for NDS, indicating a thinner effective barrier under the gate in the EQS simulations due to a different treatment of the carrier injection from the contacts into the channel and thus a slightly different electrical fields near the contacts. Future studies will focus on improving this modeling issue for this special contact type. The off-state current $I_{off} = \min(I_{DS})$ is 0.27 nA for the EQS results and 0.01 nA for the NDS results leading to an I_{on}/I_{off}-ratio of 2.9×10^3 for the EQS results and 9.5×10^4 for the NDS results. However, the closeness of V_{GS} for which the minimum value of the current is reached and the similar steepness of the plots obtained with both methods (see Fig. 2(a)) validate the NDS model in this bias region.

The increasing current in region (iii) can be explained by band-to-band tunneling (BTBT) which is enabled by the shape of the bands as shown in Fig. 2(b). In addition to this, a significant transmission peak above the drain Fermi level can be seen in Fig. 3(d) which is due to BTBT. The shape and the location in energy of this peak is in good agreement between EQS and NDS results. Both methods predict a decrease of the current in region (iii) when reducing the voltage further. This results from localized energy levels in the channel, which are pushed slightly above the Fermi energy, reducing the density of states in the bias window. Using the NDS model, this effect can be observed at smaller negative voltages compared to EQS, which can be attributed to a different electrostatic control predicted by the NDS model.

The transmission probability in the different bias regions shown in Fig. 3 is to some degree higher for the EQSs than for the NDSs due to the electrical fields near the contacts. However, this difference has a major impact only in region (ii) as described above. NDS and EQS results of the 5.9 nm-GAA CNTFET show good agreement in the trend of the transfer characteristic for different bias regions, thus, validating the model used for NDS, since it describes quantum mechanical effects in a reasonable way. The ambipolarity due to BTBT is also properly described by both models and the results are comparable to other EQS results including this effect [28].

3) Channel length scaling: More detailed insight of the impact of transport mechanims on the current at different bias regions, captured by both simulation approaches, can be obtained with scaling studies. In Fig. 4 the transfer characteristics obtained from EQS and NDS are shown for n-type GAA CNTFETs with L_{ch} equal to 5.1 nm, 6.4 nm, 7.7 nm, 9 nm and 10.2 nm and fixed L_{sp} of 1.28 nm, i.e., L_g is changed accordingly. Devices with ultra-short gate lengths had been expected to be unlikely to fabricate just a couple of years back, however, very recently devices with similar and even shorter gate lengths have been demonstrated [29], [30].

Albeit the different electrical fields near the contacts in EQS, similar trends can be observed from the results of both methods. A thermionic regime can be identified at $V_{GS} >$

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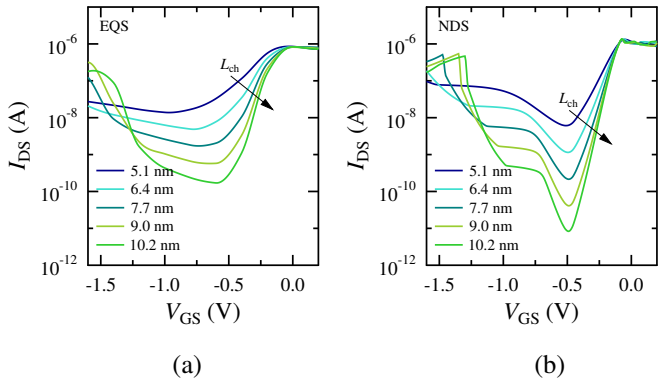

Fig. 4. Transfer characteristics for different channel lengths and fixed spacer length of 1.28 nm obtained with (a) EQS and (b) NDS for n-type GAA CNTFETs.

-0.1 V for all devices in which the best agreement between EQS and NDS results is found. As V_{GS} is reduced, in both simulations the transistor switches off, the threshold voltage V_{th} is decreased and the subthreshold slope SS is increased. At lower V_{GS}, an increase in the current can be observed, which can be attributed to BTBT. For ultra-short channel lengths below 7 nm, ambipolarity is drastically reduced in both simulation results, which can be explained by a dominating intraband tunneling mechanism in this bias region.

In Table I, the values for I_{on}, I_{off} and SS for the devices with different channel lengths are listed. The values of I_{on} are similar for both simulation methods and remain almost unchanged as the channel length increases, since both are ballistic models working in a thermionic regime. The difference in I_{off} and SS values in both methods are due to the different electrical fields near the contacts as discussed above. However, the trend and range of these values are similar, hence validating the tunneling model implemented in NDS.

TABLE I
ON-STATE CURRENT, OFF-STATE CURRENT AND SUBTHRESHOLD SLOPE OF GAA CNTFETS WITH DIFFERENT CHANNEL LENGTHS AND A FIXED SPACER LENGTH OF 1.28 nm OBTAINED WITH EQS AND NDS.

L_{ch} (nm)	I_{on} (μA)		I_{off} (nA)		SS (mV/dec)	
	EQS	NDS	EQS	NDS	EQS	NDS
5.1	0.3	1	14	6.1	325	146
6.4	0.8	1.1	4.9	1.1	232	106
7.7	0.8	1	1.8	0.2	186	84
9.0	0.8	0.9	0.6	0.04	156	71
10.2	0.8	0.9	0.2	0.01	134	64

Considering the EQS results, the I_{on}/I_{off}-ratio of 4×10^3 for the 10.2 nm-GAA CNTFET is the highest for these devices. This value is also higher than the one recently reported for another GAA CNTFET with similar physical dimensions modeled for high-performance logic applications [31]. Additionally, for the device with a channel length of 9 nm it is found that the I_{on}/I_{off}-ratio of 1.3×10^3 is similar to the value obtained from experimental data of a similar device reported in [25].

B. Comparison with experimental data

In addition to the comparison with EQS results presented in this work for different scaling scenarios, the reliability of the numerical device simulator has already been demonstrated in different studies by modeling fabricated CNTFETs and accurately reproducing the corresponding experimental results [7], [22]. A careful calibration of the NDS simulator [32] to a 9 nm-channel length CNTFET [25] showing an excellent agreement between NDS and experimental data suggests that the calibrated numerical device simulator is reliable for sub-10 nm devices. In contrast, a direct verification of EQS with experimental data is not possible due to computational limitations of this simulation approach.

IV. DEVICE OPTIMIZATION

A. Simulated devices

In order to study the performance of ultra-scaled CNTFETs for specific applications, different device architectures are evaluated by means of the calibrated numerical device simulator discussed in Section III. Due to the computational burden of EQSs and restrictions in terms of device architectures, NDS is prefered for engineering studies, such as exploring feasible and optimized device architectures. While Schottky barriers are considered, an additional contact resistance is not included. For the study discussed in this Section, the simulator has been calibrated to experimental data [25] of a p-type CNTFET with a L_{ch} of 9 nm [32], i.e., all devices studied here are p-type.

Four different device architectures are studied: a top gate (TG), a global back gate (GBG), a buried gate (BG) and a GAA structure. The channel length is 5.9 nm for all devices. The schematic cross section of each CNTFET structure is shown in Fig. 5. The high-κ oxide permittivity is 18 for all structures. Design parameters of the simulated devices are listed in Table II where $h_{s/d}$ is the source and drain contact height, h_g is the gate contact height and t_{ox} is the high-κ oxide thickness.

TABLE II
DESIGN PARAMETERS OF THE 5.9 nm CNTFET STRUCTURES.

	L_{ch} (nm)	L_g (nm)	d_{CNT} (nm)	$L_{s/d}$ (nm)	$h_{s/d}$ (nm)	h_g (nm)	t_{ox} (nm)
TG	5.9	3	1.4	5	2	2	2
GBG	5.9	11.9	1	3	3	3	2
BG	5.9	5.9	1	3	3	3	2
GAA	5.9	3.9	1	3	3	3	2

For each simulated CNTFET structure, ohmic-like and Schottky contacts are investigated which corresponds to hole Schottky barrier heights ϕ_{SB} of -0.15 eV and 0.15 eV, respectively, which under some conditions represent Cr and Pd contacts [11]. Following the 2026 ITRS requirements given for the high-performance application scenario, the supply voltage $V_{DD} = V_{DS}$ is set to -0.57 V in the simulations [33].

The simulated single-tube devices have a width equal to a pitch of 5 nm, equivalent to a CNT density of 200 CNTs/μm, as suggested in [25]. By applying periodic boundary conditions it is possible to consider the electrostatic CNT interactions, i.e., screening effects, resulting from such a narrow pitch.

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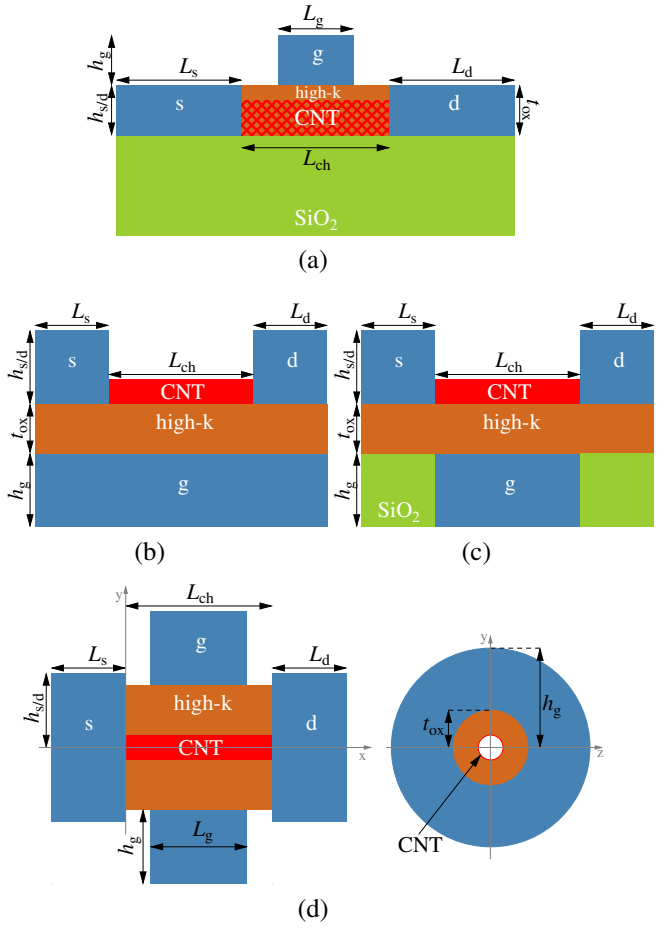

Fig. 5. Schematic cross section of the studied device architectures: (a) top gate, (b) global back gate, (c) buried gate and (d) gate-all-around structure. Right side of (d) shows a frontal view of the device.

B. Device performance

In Fig. 6, the transfer characteristics of the simulated CNTFETs with different gate structures is shown. As expected, the devices with ohmic-like contacts provide higher current in the on-state regime than the devices with Schottky contacts. The first contact type represents ideal devices, while the latter is more likely to be found in realistic devices. BG, GBG and GAA structures have similar I_{off}. The highest value of $|I_{\mathrm{on}}|$ is obtained with the GAA structure while the BG structure delivers slightly higher values in the on-state than GBG. TG structure does not switch-off entirely due to poor gate control.

In Fig. 7, performance indicators extracted from NDS results of each CNTFET structure with both types of contacts are shown. In order to have a straightforward comparison of the device performance, the data is post-processed in such a way that I_{off} corresponds to $\min(|\mathrm{I_{DS}}|)$ at $V_{\mathrm{GS}} = 0\,\mathrm{V}$ while I_{on} is the current at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{\mathrm{DD}}$ after the post-processing. Both of these performance indicators are normalized to the CNT pitch. The transconductance g_{m} is obtained from the derivative of the drain current with respect to the gate-to-source voltage at V_{DD} and it is also normalized to the CNT pitch. The intrinisic transit frequency $f_{\mathrm{T,i}}$ is obtained using $f_{\mathrm{T,i}} \approx g_{\mathrm{m}}/(2\pi C_{\mathrm{g,tot}})$, where $C_{\mathrm{g,tot}}$ is the total gate

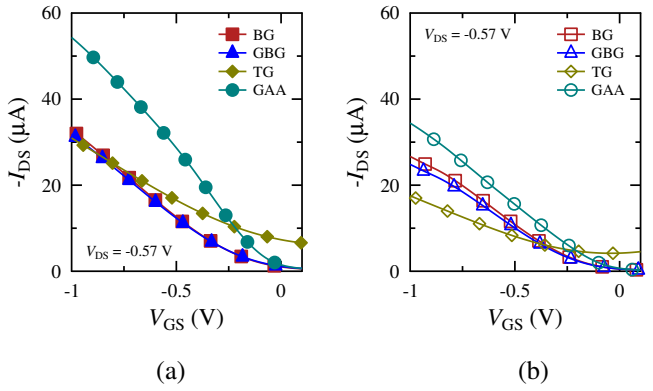

Fig. 6. Transfer characteristics of the simulated top gate, global back gate and buried gate *p*-type CNTFETs with a channel length of 5.9 nm and using (a) ohmic-like and (b) Schottky contacts. Markers are included for guidance, however, more points have been calculated.

capacitance including the oxide capacitance and the fringing capacitances between the contacts. The intrinsic gate delay CV/I and the dynamic power indicator CV^2 are calculated using $C_{\mathrm{g,tot}}$, V_{DD} and I_{on}. The subthreshold slope of each device is calculated as the inverse of the derivative of the logarithm of the drain current with respect to the gate-to-source voltage. A comparison with data available in the literature of devices with similar L_{ch} is included in the following analysis for reference purposes, however, the main scope of this study is the comparison between different simulated gate structures.

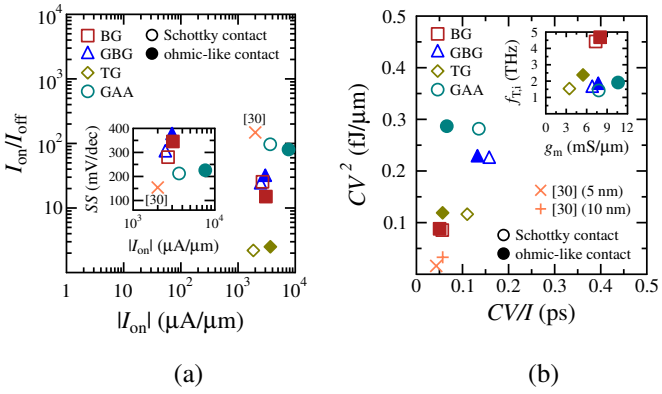

Fig. 7. Performance indicators of the simulated CNTFET structures with ohmic-like (filled markers) and Schottky contacts (empty markers). (a) $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio versus $|I_{\mathrm{on}}|$. Inset: subthreshold slope over $|I_{\mathrm{on}}|$. (b) Switching energy versus intrinsic gate delay. Inset: intrinsic cutoff frequency versus transconductance. Crosses indicate data reported in [30] (Figure S3 used for (a) and Table I used for (b)) for CNTFETs with similar dimensions to the studied here but taken at a lower V_{DD} than the used in this work.

The plot of $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio versus $|I_{\mathrm{on}}|$ of the simulated CNTFETs is shown in Fig. 7(a). Since there is no potential barrier for carriers in ohmic-like contacts, these CNTFET structures have higher $|I_{\mathrm{on}}|$ than the devices with Schottky contacts. For Schottky contacts, the highest values of $|I_{\mathrm{on}}|$ for the BG and GAA structures overcome the experimental value reported in [30] at a different bias point ($V_{\mathrm{GS}} = V_{\mathrm{DD}} = |0.4\,\mathrm{V}|$) for a 5 nm *p*-type CNTFET. However, due to a higher $|I_{\mathrm{off}}|$ predicted in NDS, $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio deviates from the experimental data which can be explained by the difference in the bias points

at which these indicators are extracted and by the different electrostatics due to distinct contact properties [30]. These differences explain as well the discrepancy between the lowest SS of 212 mV/dec obtained with the Schottky GAA structure and the 154 mV/dec obtained for the fabricated 5 nm-GAA CNTFET [30] as shown in the inset of Fig. 7(a).

In the inset of Fig. 7(b), the $f_{\mathrm{T,i}}$ versus g_{m} plot for the simulated devices is shown. The devices with the best channel control, i.e., highest g_{m}, are the BG and GAA structures, which can be explained by a reduced parasitic coupling in comparison to the other architectures. However, due to a large internal charge, i.e., high $C_{\mathrm{g,tot}}$, the GAA device performance is degraded in terms of $f_{\mathrm{T,i}}$. The BG structure has the lowest $C_{\mathrm{g,tot}}$, which translates into an excellent high-frequency behaviour. Regardless of the contact type, the highest g_{m} and $f_{\mathrm{T,i}}$ are obtained with the BG structure.

The switching characteristics of the CNTFET structures are shown in Fig. 7(b). CV/I represents the switching time of the device. The BG structure with both types of contacts is the fastest device. This is directly associated to the improved electrostatics and high I_{on} (see Fig. 7(a)) of the corresponding devices. The switching time of the BG structure for the device with Schottky contacts, is similar to recently reported values for fabricated sub-10 nm CNTFETs [30]. Regarding the dynamic power indicator CV^2, the BG structure is the device consuming the least energy per switching regardless of the type of contact used. The difference between these performance indicators and the corresponding values reported in [30] is due to the low V_{DD} used in the latter, leading to a lower switching energy, and to a different definition of the capacitance used for the calculation of the switching energy and the intrinsic gate delay. The high $C_{\mathrm{g,tot}}$ associated to the GAA structure degrades its switching performance.

The energy delay product EDP, obtained from the product of the switching time and the switching energy, corresponds to 4.79×10^{-30} Js/μm for the BG device with Schottky contacts. When comparing this EDP with EDP of conventional sillicon devices in the 10 nm-node and with sub-10 nm CNTFETs, the values obtained here are less than in the first case, and in a similar range of values as in the latter (see Table 1 in [30]). The trade-off between switching speed and switching energy, as well as the low value of EDP, make the BG structures suitable for high-performance logic applications.

From the results discussed above it can be concluded that the best overall performance of all the simulated devices is achieved with the BG structure. Furthermore, it has been shown that the overall performance of the studied BG CNTFET with Schottky contacts could be suitable for some applications in technology nodes beyond 2023 [35]. However, due to the low barrier height (see Fig. 9) leading to high values of I_{off}, the values of $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio are lower than the ones obtained for devices with similar gate and channel lengths previously studied (see Section III). Thus, further structural changes should be implemented in order to optimize this particular performance indicator.

1) Impact of structural changes: One possible way to improve the $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio is by choosing CNTs with different diameters [36], [37]. On the left side of Fig. 8, the plot of $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio over I_{on} is shown for CNT diameters varying from 0.5 nm to 2 nm using the BG structure with a fixed ϕ_{SB} of 0.15 eV. The smaller d_{CNT}, the larger is the band gap, i.e., the higher $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio.

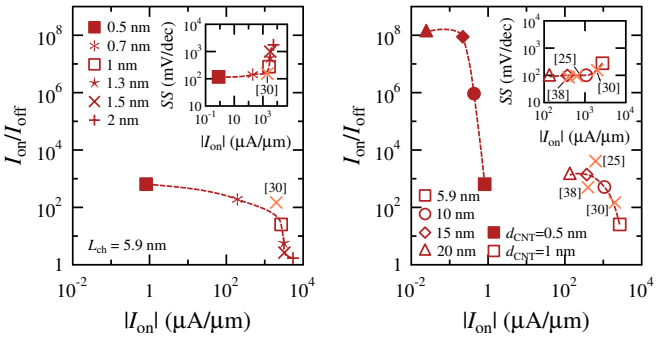

Fig. 8. $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio versus $|I_{\mathrm{on}}|$ for (a) different tube diameters and $L_{\mathrm{ch}} = L_{\mathrm{g}} = 5.9$ nm, and (b) different channel lengths, $L_{\mathrm{g}} = 5.9$ nm and different tube diameters. Results correspond to simulated BG CNTFET structures with Schottky contacts. Dashed lines are added as a guide for the eyes. Experimental data indicated with crosses correspond to devices with L_{ch} of 5 nm [30], 9 nm [25], and 20 nm [38]. In all cases V_{DD} is lower than the used in this work.

The highest $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio and the lowest SS of 116 mV/dec are achieved using a CNT diameter of 0.5 nm. However, these improvements are obtained at the cost of other performance indicators such as I_{on}, $f_{\mathrm{T,i}}$, CV/I and CV^2. In Fig. 9(a), the valence band profiles of the devices with fixed channel and gate lengths of 5.9 nm and different tube diameters are shown. For the device with the shortest d_{CNT}, $|I_{\mathrm{off}}|$ and $|I_{\mathrm{on}}|$ are reduced due to a lower potential barrier for holes compared to the device with d_{CNT} of 1 nm in both, off- and on-state. This severe suppression of current with decreasing the tube diameter and the large $C_{\mathrm{g,tot}}$ associated to small d_{CNT} [9], explain the degraded performance indicators.

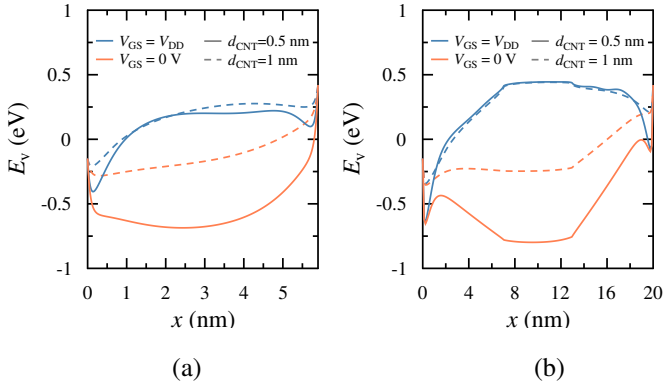

Fig. 9. Valence band profiles along the channel of the BG CNTFET structure with Schottky contacts for $d_{\mathrm{CNT}} = 0.5$ nm (solid lines) and $d_{\mathrm{CNT}} = 1$ nm (dashed lines) with a fixed L_{g} of 5.9 nm and (a) $L_{\mathrm{ch}} = 5.9$ nm and (b) $L_{\mathrm{ch}} = 20$ nm. Blue (coral) lines represent the corresponding valence band in the on-state (off-state).

Another possibility to improve the $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio is to relax L_{ch} while fixing L_{g} as it can be concluded from the results in Section III.A.3. Fig. 8(b) shows the impact of L_{ch} on the device performance indicators for a fixed L_{g} and two tube

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diameters of the BG structure with Schottky contacts and symmetrical and undoped spacers.

The highest I_{on}/I_{off}-ratio is achieved for the devices with the longest channel regardless the tube diameter. The improvement in I_{on}/I_{off}-ratio by increasing the channel length is due to a lower $|I_{off}|$ which results from a better channel control for longer channels as seen in the valence band profiles shown in Fig. 9 for the shortest and longest devices in the off- and on-state regions. While an impractical low $|I_{on}|$ is obtained for a d_{CNT} of 0.5 nm, reasonable values for $|I_{on}|$ and SS are obtained using a d_{CNT} of 1 nm as expected for longer channels [32], [39]. $|I_{on}|$, I_{on}/I_{off}-ratio and SS obtained with the latter simulated device are similar to the reported values for fabricated CNTFETs with channel lengths of 5 nm [30], 9 nm [25] and 20 nm [38] as shown in Fig. 8(b). The slight difference between the simulation and experimental data can be explained by the different electrostatics due to the distinct fabricated gate structures as well as other V_{DD} chosen in the referred publications.

The closeness of the performance indicators of fabricated devices with the ones of ideal simulated conditions shown in this section could be an indicator that ultra-scaled undoped CNTFETs are approaching their technological limits.

2) Impact of doping: The device behavior can also be modified by doping the CNT in the spacer regions [2], [13], [40]. Schottky-like BG CNTFETs with a d_{CNT} of 1 nm, a L_g of 5.9 nm and a L_{ch} of 20 nm are simulated with constant p-type doping densities N_A varying from 1×10^5 cm^{-1} to 4×10^5 cm^{-1}. Other geometrical device dimensions are listed in Table II. These results are shown in Table III where the values for the undoped device are also included.

TABLE III
PERFORMANCE INDICATORS OF A BG CNTFET WITH $L_g = 5.9$ nm AND $L_{ch} = 20$ nm WITH DIFFERENT DOPING DENSITIES.

N_A (cm^{-1})	$-I_{on}$ (μA/μm)	$-I_{off}$ (nA/μm)	CV/I (ps)	CV^2 (aJ/μm)	EDP (J s/μm)
0×10^5	134.5	101.2	0.24	20	4.8×10^{-30}
1×10^5	213.2	107.1	0.16	19.7	3.1×10^{-30}
2×10^5	308.2	156.9	0.11	19.6	2.2×10^{-30}
3×10^5	318.6	243.9	0.10	18.4	1.8×10^{-30}
4×10^5	428.1	291.5	0.07	17.9	1.3×10^{-30}

The valence band profiles for the device with different doping densities at off-state and on-state region are shown in Fig. 10. Due to doping, the spacer regions are significantly modified. The higher the doping density, the thinner the potential barriers at the contacts, i.e., the higher the tunneling probability. This leads to a higher current at higher doping densities, as reported in Table III. The highest value of I_{on}/I_{off}-ratio of 1.46×10^3 and the lowest EDP correspond to the device with the highest spacer doping concentration. This is obtained, however, at the cost of a larger SS of 163.9 mV/dec. Switching time and switching energy also improve with higher doping concentration due to a reduced capacitance.

While an improved I_{on}/I_{off}-ratio and SS are obtained with structural changes and different spacer doping densities, other performance indicators for the same devices are degraded. Thus, other structural changes such as a non-symmetric gate or a feedback gate need to be considered in order to find a balance between all performance indicators.

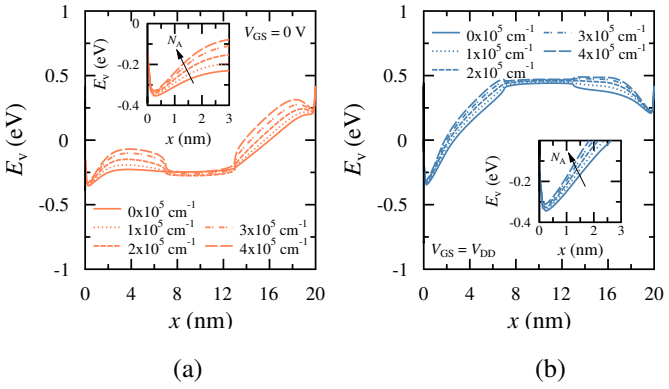

Fig. 10. Band profiles of the BG CNTFETs structure with Schottky contacts and $L_g = 5.9$ nm, $L_{ch} = 20$ nm and different p-type doping densities at (a) $V_{GS} = 0$ V and (b) $V_{DS} = V_{DD}$. The insets show the first 3 nm of the channel where a thinner barrier can be observed as doping increases.

V. CONCLUSIONS

Various device structures of ultra-scaled carbon nanotube field-effect transistors have been studied using a multi-scale approach comprising electronic quantum transport simulation and numerical device simulation.

A comparison between results obtained with an electronic quantum transport simulator and with a numerical device simulator for a 5.9 nm gate-all-around CNTFET model has been shown. Both simulation results show good agreement with respect to the calculated on-currents. Regarding the tunneling currents, which are caused by BTBT, a reasonable agreement has been found as well, since both models predict the same trend and similar values for this transport regime. This justifies to employ the numerical device simulator for device optimization where EQS can not be used due to its numerical complexity.

The performance of ultra-scaled CNTFETs with a top gate, a global back gate, buried gate and a gate-all-around with a channel down to 5.9 nm with ohmic-like and Schottky contacts has been compared. BG CNTFET turns out to be the device achieving the best performance for g_m, $f_{T,i}$, CV/I, CV^2, SS and I_{on} regardless the contact quality. However, the high I_{off} in this device leads to a low I_{on}/I_{off}-ratio. Despite the I_{on}/I_{off}-ratio, this particular device could be suitable for high-performance logic applications according to previous discussions [31].

In order to improve the I_{on}/I_{off}-ratio, structural changes and doped spacers are necessary. It has been shown that higher I_{on}/I_{off}-ratio and lower SS can be obtained, while reaching a reasonable values for $|I_{on}|$, with Schottky-like BG CNTFETs having a gate length of 5.9 nm, a channel length of 20 nm and a tube diameter of 1 nm. These performance indicators are in the same range of values as the ones reported for fabricated devices with similar channel lengths [25], [30] and [38]. Doped spacer regions lead to even higher I_{on}/I_{off}-ratio and lower EDP. These results are suitable to guide the

technology development towards ultra-scaled CNTFETs for various application scenarios.

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