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Dopant Induced Single Electron Tunneling within the Sub-bands of Single Silicon NW Tri-gate Junctionless n-MOSFET

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Abstract- We report one dimensional electron transport of silicon junctionless tri-gate n-type transistor at 4.2 K. The step like curve observed in the current voltage characteristic suggests one-dimensional transport. Besides the current steps for one-dimensional transport, we found multiple spikes within individual steps, which we relate to inter-band single electron tunneling, mediated by the charged dopants available in the channel region. Clear Coulomb diamonds were observed in the stability diagram of the device. It is shown that a uniformly doped silicon nanowire can provide us the window for the single electron tunnelling. Back-gate vs. front-gate color plot, where current is in a color scale, shows a crossover of the increased conduction region. This is a clear indication of the dopant-dopant interaction. It has been shown that back-gate biasing can be used to tune the coupling strength between the dopants.

Keywords— Junction less transistor, One dimensional transport, Single electron tunneling, Coulomb blocked, Dopant-dopant interaction.

I. INTRODUCTION

The extreme downscaling of devices will soon be restricted by the fundamental limit of scaling. This limit has prompted the scientific community to develop novel nano scale devices based on nanowire (NW), thin films and nanotubes. In the last few years, a uniformly doped gated NW resistor, called “junctionless NW transistor (JNT)” [1], has received great attention as a promising candidate due to its excellent gate controllability and simple fabrication technique. JNT supports extreme downscaling (<10 nm) without facing much fundamental challenges, such as excessive gate leakage current, exponentially increasing source to drain sub-threshold leakage current, gate stack reliability and channel mobility degradation. The gate controllability arises due to the fact that the carriers can be electrostatically depleted in extremely thin NW channel [2]. Moreover, this thin channel allows conduction band to split into sub-bands due to two dimensional electron confinements [3]. Conductance oscillations of NW transistors at low temperature have been

reported by several groups and are attributed to successive filling of individual sub-bands [4][5]. On the other hand, there are also reports on the effect of individual dopant atoms on the device characteristics [6]. In conventional semiconductor devices, the dopants are generally used to increase the number of charge carriers. Here they serve as a “bulk type” dopant having averaged potential. However, the need of scaling down devices has brought the dimensions down to few tens of nanometer. In these devices, a dopant atom may behave like a quantum dot [7], [8], [9] having “atom like” potential. This atom like potential, when present in the channel region, provides discrete sub-band for electron transport. This causes fluctuations in the current-voltage characteristics. The impact of dopant-induced fluctuations on electrical characteristics of devices has become a serious problem for further miniaturization [10]. There are, however, many reports available on the understanding of device characteristics influenced by an individual dopant atom such as single atom transistor [11], multiple or few dopant MOSFETs [12], dopant based memories [13] and dopant based photonic devices [14].

To control the number of dopants precisely in the region so as to make single atom transistors, advanced techniques such as ion implantation and focused ion beam (FIB) have been used [15][16]. Low temperature dopant transistors follow laws of quantum mechanics enabling Coulomb effect which allows single electron tunneling from source to drain lead, to take place [17]. Single electron tunneling can also be mediated by multiple dopants in the channel region that facilitates dopant-dopant interactions [18]. This interaction is a prerequisite for the charge based quantum computing [19] and single electron turnstile [20]. Thus, a comprehensive understanding of dopant-dopant interaction in NW sub-bands and single electron tunneling is highly desired. In this regard, we demonstrate a single electron transfer between few dopants in junctionless tri-gate n-type transistor. The low temperature (4.2 K) current vs. gate voltage characteristics at fixed source-drain bias show staircase-like current increase confirming the one dimensional electron transport. We also found multiple spikes in I-V characteristics within the steps, which we relate to inter-band single electron tunneling, mediated by the charged dopants available in the channel region. We show that the stability plot exhibits clear Coulomb diamonds suggesting

single electron tunneling. The current increment while sweeping both the front and back gates shows diagonal lines confirming the Coulomb blockade effect [21]. We have noticed a crossover between the increased conduction lines, a signature of dopant-dopant interactions [22]. The effect of back-gate biasing on the device characteristics is also briefly discussed.

II. DEVICE FABRICATION

Figure 1(a) shows the schematic of the device which was fabricated by simply patterning the silicon-on-insulator (SOI) wafers with a top silicon thickness of 10 nm. Fabrication starts with the arsenic doping into the top silicon layer with ion implantation. Doping concentration was $\sim 3 \times 10^{19} \text{ cm}^{-3}$. These high doping results in average dopant-dopant distance of ~ 4 nm. Source, drain and nanowire channel regions of the device were defined by e-beam lithography followed by a dry etching process. After the selective etching of the top Si layer, single crystal nanowires were obtained. Gate oxide of 10 nm was then grown by thermal oxidation. After thermal oxidation a 40 nm wide and height of 10 nm single crystal Si nanowires were obtained.

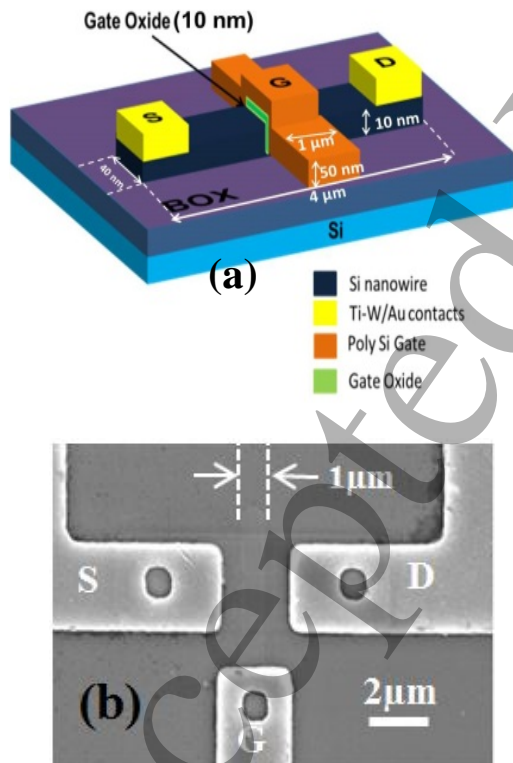


Figure 1. (a) Schematic of the fabricated device where dimension are not on proper scale. (b) SEM image of the JL device showing 1 μm channel

Heavily doped polycrystalline (P^+) silicon (poly-Si) was used as a gate material for which 50 nm thick film of amorphous

silicon was deposited in a low-pressure chemical deposition reactor at 550°C . Film was heavily doped with boron and subsequently annealed at 900°C for 30 min to obtain a low resistance poly-Si film. Poly-Si was then patterned by e-beam lithography and etched by reactive ion etching to define the gate area. Afterwards SiO_2 was deposited for the electrical insulation at source, drain and gate terminal. Contact windows were opened in the deposited oxide and metallization was carried out using Ti/W-Al. Figure 1(b) shows the scanning electron microscope (SEM) image of the fabricated device with gate length of 1 μm . The channel cross-section for similar type of devices can be found in Ref.[23]

III. RESULTS AND DISCUSSION

To investigate the device behavior and the effect of individual dopant atoms present in the channel region, its electrical characterization has been studied in detail. All the measurements were performed at 4.2 K.

A. Stability Plot

The drain current versus gate and bias voltages diagram, where current is shown by a color scale, is called the stability diagram. It gives the information about the source, drain and gate capacitive coupling. Figure 2 (a) and (b) shows the stability diagram of the device at $V_{\text{BG}} = 0 \text{ V}$ and $V_{\text{BG}} = 40 \text{ V}$, in which clear Coulomb diamonds can be observed. It is noticed that there are multiple overlapping diamonds suggesting the resonant tunneling between the multiple dopants [24]. The two different diamonds are shown in Figure. 2 (b) by white and black outlining, respectively. For back gate voltage $V_{\text{BG}} = 0 \text{ V}$, we have calculated the values of source, drain and gate capacitances (C_s , C_d and C_g) for the diamonds shown by white outlining, and found to be $0.07 \times 10^{-18} \text{ F}$ (C_s), $0.38 \times 10^{-18} \text{ F}$ (C_d) and $2.2 \times 10^{-18} \text{ F}$ (C_g) respectively. The dopant is mainly coupled to the gate ($C_g \gg C_{s(d)}$). Capacitances extracted from the stability diagram (figure 2. (a) & (b)) are the measure of the coupling strength of the dopants towards source, drain and gate, which significantly depends on the position of the dopants. Even though the device looks symmetric but position of the dopant may be closer toward drain side ($C_d > C_s$). Another diamond (black outline) is also visible, which suggests the electron transfer via multiple dopants. Interestingly, the diamonds are not closed, indicating the resonant tunneling occurring through multiple dopants even in a long (1 μm) channel. For high backgate bias the vertical electric field ionizes the dopants and then these dopants give rise to attracting Coulomb potentials [21] and induce resonances in the subthreshold conductance due to electron tunneling through their discrete energy levels. In figure 2(b) at high back-gate voltage ($V_{\text{BG}} = 40 \text{ V}$) the number of diamonds increases and they become more overlapping. These indistinguishable diamonds may be a result of the modification of the electronic structure of dopants in the presence of high electric field. This also allows us to control or tune the single electron tunneling, ranging from single or few dopant operations to a multiple/cluster like electronic structure.

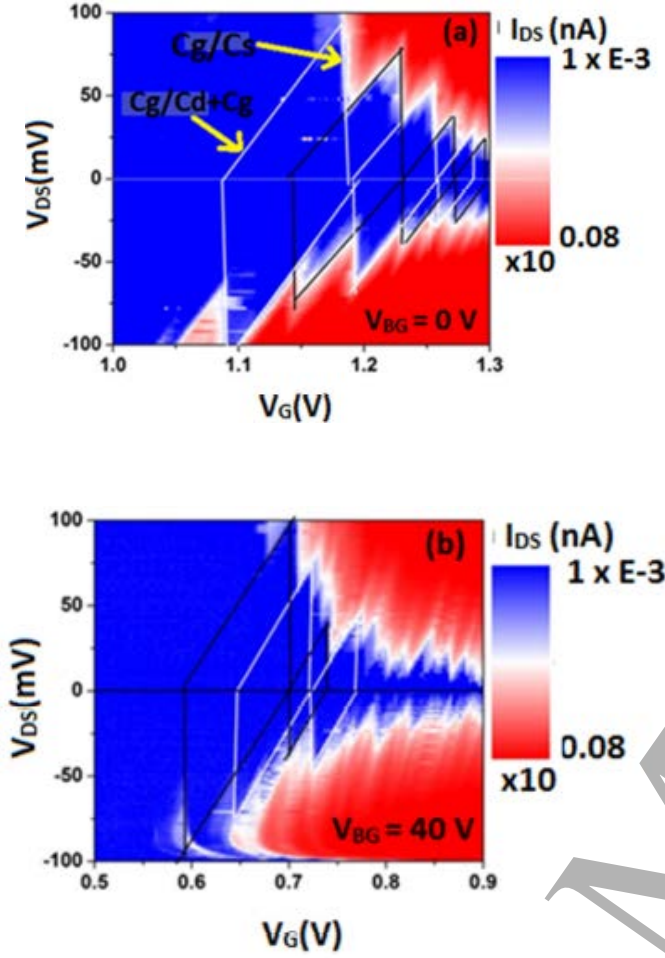


Figure 2. Stability diagram of the device (a) at $V_{BG} = 0$ V and (b) at $V_{BG} = 40$ V, showing multiple coulomb diamonds resulting from resonant tunneling between dopant states.

B. I_D - V_G Characteristic

Figure 3(a) show the schematic cross section of the silicon nanowire of width (W_{Si}) and height (H_{Si}) in which dopants are symbolically represented. Figure 3 (b) shows the drain current (I_D) vs. gate voltage (V_G) characteristics at different drain to source voltages (V_{DS}) at 4.2 K. The threshold voltage of the device was found to be around 1.2 V, beyond which the step-like curve can be observed. These current oscillations are attributed to the one dimensional carrier transport in the NW transistor[5]. The carrier confinement splits the energy band of NW into multiple sub bands of different energy levels, which reflects in the form of step-like current oscillation in the electrical characteristic of the NW transistor. In Figure 3 (b), the arrows showing multiple small spikes within the sub-bands suggest the inter-band single electron tunneling, mediated by the charged dopants available in the channel region. Daniel Moraru et. al. also reported on such fluctuations, however, the spikes were not distinguishable [25]. Contrarily, we observed spikes which are distinct for the lower gate voltages. The individual dopant serves as an artificial atom having discrete

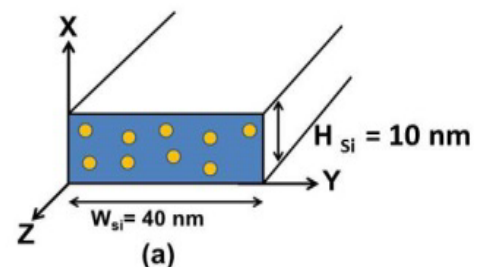
energy levels. The gate voltage spacing for the steps in the I_D - V_G curve (marked by arrows in figure. 3(b)) was found to be 30 mV, 39 mV, 45mV, 52 mV and 70 mV. Positions of the spikes are quite consistent when we characterize the device for various V_{DS} , which is also evident from the coulomb diamonds in Fig 2 (a) and (b). We use the scheme mentioned in [4] to convert the gate voltage spacing to the sub-band spacing (ΔE_{SB}), where ΔE_{SB} is given by

$$\Delta E_{SB} = \frac{Cox \cdot \Delta Vg \cdot \pi \hbar^2}{2 m^* e} \dots \dots \dots (1)$$

Where Cox is the gate capacitance per unit area and we calculated it to be 3.36×10^{-7} F/cm² (10 nm gate oxide), ΔVg is the gate voltage spacing between steps, m^* is the effective mass (0.19 m_0) and e is the electronic charge. We estimated the sub-band spacing to be 3.38 meV, 4.8 meV, 5.7 meV, 6.8 meV and 8.2 meV, respectively, for the aforementioned gate voltage spacing. We use a square well approximation to theoretically calculate the sub-band energies. Eq. 2 represents the discrete energy levels (above the conduction band) for the wire in which the electron is confined in the 'x' and 'y' direction. $W_{Si} = 40$ nm and $H_{Si} = 10$ nm are the width and height of the NW in the 'x' and 'y' direction, respectively (see Figure 3 (a)). Here n_x and n_y are the sub-band indexes for the 'x' and 'y' direction having values from 1 to infinity.

$$E_{n_x n_y} = \frac{\pi^2 \hbar^2}{2m^*} \left[\left(\frac{n_x}{W_{Si}} \right)^2 + \left(\frac{n_y}{H_{Si}} \right)^2 \right] \dots \dots \dots (2)$$

All the possible energy states for $n_x = 1$ and $n_y = 1$ to 6 are shown in Figure 3 (c). The sub-band energy spacing calculated theoretically (see figure 3 (c)) was 3.72 meV ($E_{12} - E_{11}$), 6.19 meV ($E_{13} - E_{12}$), 8.5 meV ($E_{14} - E_{13}$), 11.4 meV ($E_{15} - E_{14}$), and 13.8 meV ($E_{16} - E_{15}$). Theoretical values are comparable with the experimentally obtained values for lower V_G (see Figure 3(d)). However, for higher V_G , the electrostatic depletion of charges changes the effective cross-section of the wire [7]. This might be the possible reason for the deviation between the theoretically calculated and experimentally obtained values of ΔE_{SB} . This is also visible in the form of quasi- periodic step envelopes (see Figure. 3(b)). Within an envelope, a multiple number of spikes are incorporated, suggesting that single-electron tunneling transport is modulated by a complex spectrum of dopant energy states. Figure 3 (e) shows the dopant distribution of the nanowire device along with conduction band edge profile at positive V_{DS} showing dopant states of few dopants. We observed slight shift in position of these spikes towards higher V_G , when device was characterized with higher V_{DS} .



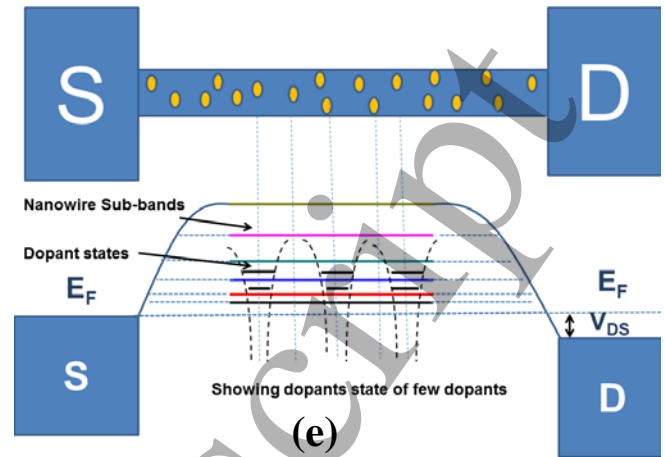
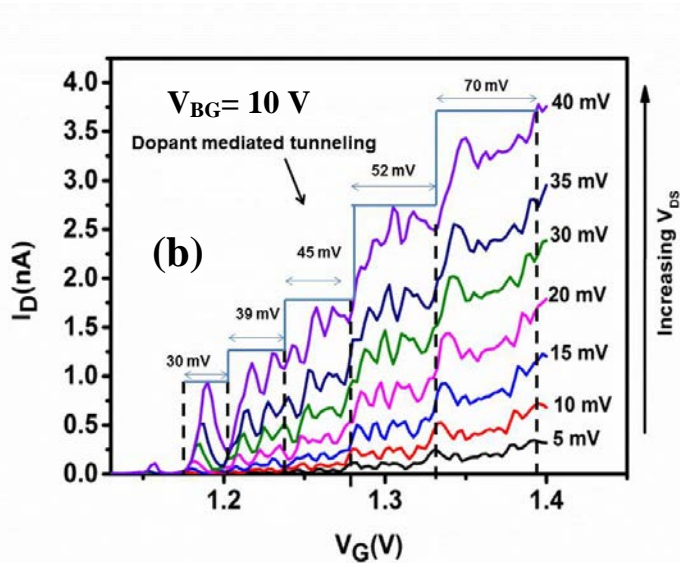
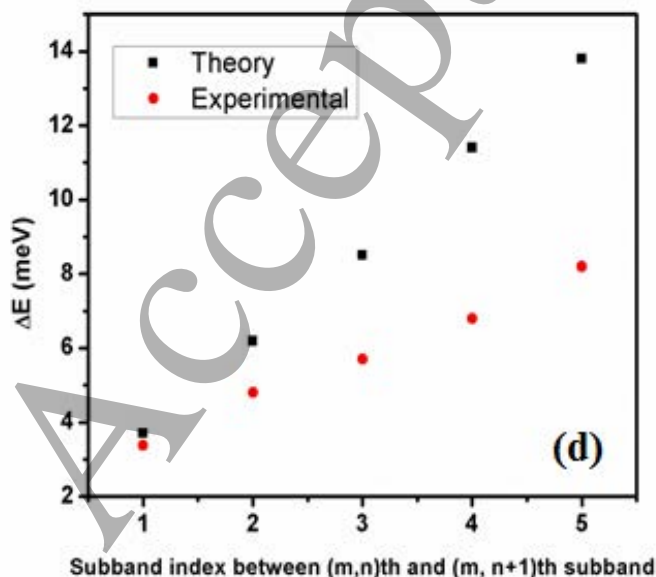
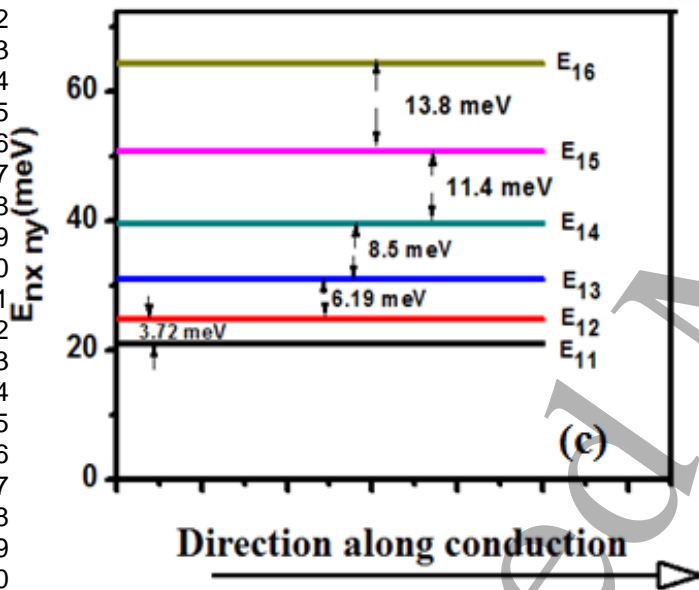


Figure 3. (a) Schematic view of a Si NW showing rectangular cross-section of the wire. (b) Drain current (I_D) vs. gate voltage (V_G) characteristic at different V_{DS} from 10 mV to 40 mV at 4.2 K. (c) Theoretically calculated sub-band energy spacing for the NW using eq. 2., showing discrete energy states from E_{11} to E_{16} and their respective energy spacing. (d) Comparison of theoretical and experimental values of sub-band spacing between (m, n) th and $(m, n+1)$ th sub-band indexes. (e) Simplified conduction band edge profile at some positive V_{DS} showing dopant states of few dopants.



C. Effect of back-gate bias

Figure 4 shows the effect of back-gate biasing on the transfer characteristics of the device. Back gate voltage was varied from -10 V to $+10$ V; we found a direct dependence of drain current on the back-gate bias. When the back-gate bias increased from -10 V to $+10$ V, almost 100% increase in the ON current was observed (at $V_G = 1.35$ V). This increase in current (at higher V_{BG}) is due to mobility enhancement under back gate bias, which is a result of improvement in the Si/SiO₂ interface quality [26]. It also changes the threshold voltage of the device and provides better gate controllability to the device channel. Another and more important effect of the back gate bias is the vertical electric field in the channel region, which modulated the Coulomb potential of each dopant differently. This modulation depends on the position of the dopants in the channel. The effective barrier thickness (provided by superposition of donor states) thus can be controlled by applying the back gate bias. The single electron tunneling within the sub-bands did not altered due to back-gate biasing. The curves follow the same trend; however we have noticed an increase in the number of spikes and a decrease in the spacing between them (within the sub-bands) at higher back-gate bias. This may be attributed to a change in the electrostatic energy resulting in more available states. Each current step in figure 3(b) consist of many sub-peaks. This kind of behavior can be correlated to the complex spectrum initiated by dopants available in the channel region. Here, the interaction between the dopants has an important role to play. Electric field applied vertically to the current flow (V_{BG}) modifies this interaction. This dopant-dopant interaction results in a molecular like energy states [25]. This modification of the spectrum may lead to the formation of deeper energy states as compared to single dopants. By

changing the back gate bias, one can change the dopant-dopant interaction. The number of spikes in the I-V curve depends on the interaction strength. Therefore by changing the back gate bias, we observed more number of spikes with in the sub bands.

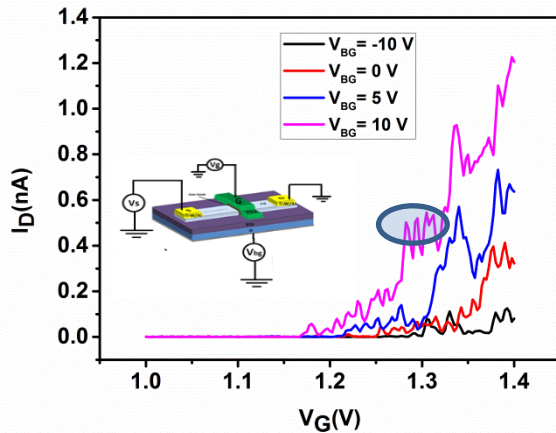


Figure 4. Effect of back-gate bias on the transfer characteristic at fixed V_{DS} of 20 mV

The number of spikes in the I-V curve depends on the interaction strength. Therefore by changing the back gate bias, we observed more number of spikes with in the sub bands. (shown by a circle in Figure 4)

D. Charge stability diagram (current vs. v_g-v_{bg}): dopant-dopant interaction

The plot between current, front gate and back gate bias where the current is the third axis presented by the color contour in the V_{BG} - V_G plane is shown in Figure 5. We have observed increased current regions in the form of diagonal lines in the V_{BG} - V_G plane. The slopes of these lines are different for forward and reverse sweep. Origin of these parallel lines lies in the resonant tunneling through the multiple dopants, arising from the Coulomb blockade phenomenon. To a first approximation, tunneling resonances due to the addition of electrons to the same quantum dot produce parallel conductance lines in the $(V_{BG}$ - $V_g)$ plane. Here the back gate is used as an additional control gate. This 2-D mapping is used as a signature for the donor-donor interaction [27]. We used this mapping to show the crossover of the increased conductance region which is an indication of the resonant tunneling between donors and donor-donor interaction. In Figure 5 (b) line: 1 represents the addition of the first electron to the dot (which is an arsenic donor in our device), and line: 2 and 3 are due to the addition of the next set of electrons, which contributes to the conduction. We have observed the crossover of the line: 2 and line: 3 which is shown by a circle in figure 5 (b). This is due to the alignment of the energy levels of the subsequent donor levels and results in the resonant conditions.

At higher front and back gate voltages, the conduction is dominated by the complex band rather than the electron

hopping mechanism. The dashed square in figure 5 (b) represents this conduction by indistinguishable current lines.

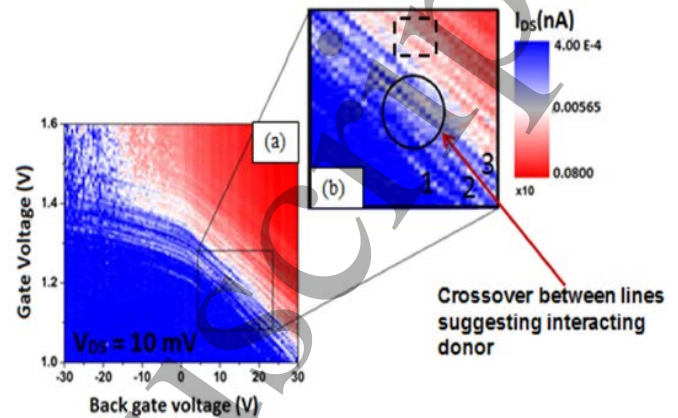


Figure 5. (a) Contour plots, drain current vs. VBG-VG. (b) Enlarge image of figure 5 (a) showing the crossover between the increased current regions

IV. CONCLUSION

1 μm gate length silicon junctionless tri-gate n-transistors were fabricated by E-beam lithography, RIE, thermal oxidation and poly-Si deposition by low pressure chemical vapor deposition. We have studied the transfer characteristic of the device at 4.2 K. Current oscillation confirms the one dimensional carrier confinement. Spikes within the sub-bands suggest the single electron tunneling and Coulomb blockade regime operation of devices mediated by the few dopants available in the NW channel region. The back gate biasing provides 100% increase in the drain current when back gate bias changes from -10 V to +10 V. Also, we have shown that the back gate bias can be used to tune the coupling strength among the dopants. Lastly, the charge stability diagram confirms the interaction among the dopants. This interaction in a long channel NW transistor could open windows for the future quantum electronics devices. However, theoretical calculation or density functional theory (DFT) calculation, incorporating donor atoms in NW, would provide better understanding of the electron transport mechanism

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