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Novel Methods for Controlled Self-Catalyzed Growth of GaAs Nanowires and GaAs/$Al_xGa_{1-x}As$ Axial Nanowire Heterostructures on Si Substrates by Molecular Beam Epitaxy

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submitted by

M.Sc. Tina Tauchnitz

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Erstgutachter: Prof. Dr. Gianaurelio Cuniberti
Technische Universität Dresden

Zweitgutachter: Prof. Dr. Manfred Helm
Technische Universität Dresden
Helmholtz-Zentrum Dresden-Rossendorf

Drittgutachter: Prof. Dr. Henning Riechert
Humbold Universität zu Berlin
Paul-Drude-Institut Berlin

Abstract

GaAs-based nanowires are attractive building blocks for the development of future (opto)electronic devices owing to their excellent intrinsic material properties, such as the direct band gap and high electron mobility. A pre-requisite for the implementation of novel functionalities on a single Si chip is the monolithic integration of the nanowires on the well-established Si complementary-metal-oxide-semiconductor (CMOS) platform with precise control of the nanowire growth process.

The self-catalyzed (Ga-assisted) growth of GaAs nanowires on Si(111) substrates using molecular beam epitaxy has offered the possibility to obtain vertical nanowires with predominant zinc blende structure, while potential contamination by external catalysts like Au is eliminated. Although the growth mechanism is fairly well understood, control of the nucleation stage, the nanowire number density and the crystal structure has been proven rather challenging. Moreover, conventional growth processes are typically performed at relatively high substrate temperatures in the range of 560-630 °C, which limit their application to the industrial Si platform.

This thesis provides two original methods in order to tackle the aforementioned challenges in the conventional growth processes. In the first part of this thesis, a simple surface modification procedure (SMP) for the *in situ* preparation of native-SiO_x/Si(111) substrates has been developed. Using a pre-growth treatment of the substrates with Ga droplets and two annealing cycles, the SMP enables highly synchronized nucleation of all nanowires on their substrate and thus, the growth of exceptionally uniform GaAs nanowire ensembles with sub-Poissonian length distributions. Moreover, the nanowire number density can be tuned within three orders of magnitude and independent of the nanowire dimensions without prior *ex situ* patterning of the substrate. This work delivers a fundamental understanding of the nucleation kinetics of Ga droplets on native-SiO_x and their interaction with SiO_x, and confirms theoretical predictions about the so-called nucleation antibunching, the temporal anti-correlation of consecutive nucleation events.

In the second part of this thesis, an alternative method called droplet-confined alternate-pulsed epitaxy (DCAPE) for the self-catalyzed growth of GaAs nanowires and GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures has been developed. DCAPE enables nanowire growth at unconventional, low temperatures in the range of 450-550 °C and is compatible with the standard Si-CMOS platform. The novel growth approach allows one to precisely control the crystal structure of the nanowires and, thus, to produce defect-free pure zinc blende GaAs-based nanowires. The strength of DCAPE is further highlighted by the controlled growth of GaAs/$Al_xGa_{1-x}As$ axial quantum well nanowires with abrupt interfaces and tunable thickness and Al-content of the $Al_xGa_{1-x}As$ sections. The GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures are interesting for applications as single photon emitters with tunable emission wavelength, when they are overgrown with thick lattice-mismatched $In_xAl_{1-x}As$ layers in a core-shell fashion. All results presented in this thesis contribute to paving the way for a successful monolithic integration of highly uniform GaAs-based nanowires with controlled number density, dimensions and crystal structure on the mature Si platform.

Kurzfassung

GaAs-basierte Nanodrähte sind attraktive Bausteine für die Entwicklung von zukünftigen (opto) elektronischen Bauelementen dank ihrer exzellenten intrinsischen Materialeigenschaften wie zum Beispiel die direkte Bandlücke und die hohe Elektronenbeweglichkeit. Eine Voraussetzung für die Realisierung neuer Funktionalitäten auf einem einzelnen Si Chip ist die monolithische Integration der Nanodrähte auf der etablierten Si-Metall-Oxid-Halbleiter-Plattform (CMOS) mit präziser Kontrolle des Wachstumsprozesses der Nanodrähte.

Das selbstkatalytische (Ga-unterstützte) Wachstum von GaAs Nanodrähten auf Si(111)-Substrat mittels Molekularstrahlepitaxie bietet die Möglichkeit vertikale Nanodrähte mit vorwiegend Zinkblende-Struktur herzustellen, während die potentielle Verunreinigung der Nanodrähte und des Substrats durch externe Katalysatoren wie Au vermieden wird. Obwohl der Wachstumsmechanismus gut verstanden ist, erweist sich die Kontrolle der Nukleationsphase, Anzahldichte und Kristallstruktur der Nanodrähte als sehr schwierig. Darüber hinaus sind relativ hohe Temperaturen im Bereich von 560-630 °C in konventionellen Wachstumsprozessen notwendig, die deren Anwendung auf der industriellen Si Plattform begrenzen.

Die vorliegende Arbeit liefert zwei originelle Methoden um die bestehenden Herausforderungen in konventionellen Wachstumsprozessen zu bewältigen. Im ersten Teil dieser Arbeit wurde eine einfache Prozedur, bezeichnet als *surface modification procedure* (SMP), für die *in situ* Vorbehandlung von nativem-SiO$_x$/Si(111)-Substrat entwickelt. Die Substratvorbehandlung mit Ga-Tröpfchen und zwei Hochtemperaturschritten vor dem Wachstumsprozess ermöglicht eine synchronisierte Nukleation aller Nanodrähte auf ihrem Substrat und folglich das Wachstum von sehr gleichförmigen GaAs Nanodraht-Ensembles mit einer sub-Poisson Verteilung der Nanodrahtlängen. Des Weiteren kann die Anzahldichte der Nanodrähte unabhängig von deren Abmessungen und ohne *ex situ* Vorstrukturierung des Substrats über drei Größenordnungen eingestellt werden. Diese Arbeit liefert außerdem ein grundlegendes Verständnis zur Nukleationskinetik von Ga-Tröpfchen auf nativem-SiO$_x$ und deren Wechselwirkung mit SiO$_x$ und bestätigt theoretische Voraussagen zum sogenannten Nukleations-Antibunching, dem Auftreten einer zeitlichen Anti-Korrelation aufeinanderfolgender Nukleationsereignisse.

Im zweiten Teil dieser Arbeit wurde eine alternative Methode, bezeichnet als *droplet-confined alternate-pulsed epitaxy* (DCAPE), für das selbstkatalytische Wachstum von GaAs Nanodrähten und GaAs/Al$_x$Ga$_{1-x}$As axialen Nanodraht-Heterostrukturen entwickelt. DCAPE ermöglicht das Nanodrahtwachstum bei unkonventionell geringeren Temperaturen im Bereich von 450-550 °C und ist vollständig kompatibel mit der Standard-Si-CMOS-Plattform. Der neue Wachstumsansatz erlaubt eine präzise Kontrolle der Kristallstruktur der Nanodrähte und folglich das Wachstum von defektfreien Nanodrähten mit phasenreiner Zinkblende-Struktur. Die Stärke der DCAPE-Methode wird des Weiteren durch das kontrollierte Wachstum von GaAs/Al$_x$Ga$_{1-x}$As axialen Quantentopf-Nanodrähten mit abrupten Grenzflächen und einstellbarer Dicke und Al-Anteil der Al$_x$Ga$_{1-x}$As-Segmente aufgezeigt. Die GaAs/Al$_x$Ga$_{1-x}$As axialen Nanodraht-Heterostrukturen sind interessant für den Einsatz als Einzelphotonen-Emitter mit einstellbarer Emissionswellen-

länge, wenn diese mit gitterfehlangepassten $In_xAl_{1-x}As$-Schichten in einer Kern-Hülle-Konfiguration überwachsen werden. Alle Ergebnisse dieser Arbeit tragen dazu bei, den Weg für eine erfolgreiche monolithische Integration von sehr gleichförmigen GaAs-basierten Nanodrähten mit kontrollierbarer Anzahldichte, Abmessungen und Kristallstruktur auf der industriell etablierten Si-Plattform zu ebnen.

Index

1 Motivation

In the past decades, the semiconductor industry has been driven by continuous miniaturization following *Moore's* law postulated in 1965. It states the cost-effective increase of the number of transistors per integrated circuit by a factor of two within a period of one year [1], and has been later adjusted to a period of two years. Top-down scaling of electronic components according to the *More Moore* route realized on the planar Si complementary metal-oxide-semiconductor (CMOS) platform has not only reached its physical limitations, but also meets the edge of innovation and economical feasibility. Therefore, future concepts, which accelerate the development of novel high-performance (opto)electronic devices on the Si platform, are strongly required to introduce the post-*Moore* era. Such concepts, in particular the so-called *More than Moore* or *Beyond Moore* concept, rely on the heterogeneous integration of multiple devices and functionalities on a single Si chip. Those System-on-Chip (SoC) modules are thought to be more powerful and less costly compared to the assembly of several separate integrated circuits.

One-dimensional III-V semiconductor nanocrystals, also denoted as nanowires, can provide innovative solutions in order to address the diversity of (opto)electronic components on the Si platform. Nanowires offer lateral dimensions of only a few tens and lengths of several hundreds of nanometers. Their large height and surface area, but small diameter and volume result in a high aspect and large surface-to-volume ratio. Not only the geometry, but also the excellent intrinsic material properties, that are well-known from their III-V bulk counterparts, in particular the direct band gap and the high electron mobility, appear attractive for the fabrication of future (opto)electronic devices on the mature Si platform. Already in the early 1990s, the outstanding potential of III-V nanowires as building blocks for novel devices has been highlighted for the first time by demonstrating light emission from p-n junctions based on GaAs nanowires [2].

Due to their geometry, III-V nanowires exhibit various advantages compared to III-V thin films. One main advantage is that III-V nanowires can be grown free of misfit-dislocations on highly lattice-mismatched substrates owing to their small interface area with the substrate. This advantage opens the promising route for defect-free monolithic integration of III-V semiconductors on low-cost Si substrates. To date, a variety of single III-V nanowire-based devices, that were mainly fabricated on the Si platform, have been presented in the fields of (opto)electronics and photonics. For instance, high-electron-mobility field-effect transistors (FETs) [3, 4, 5] as well as tunnel FETs [6] have been demonstrated for high-speed and low-power computing. The mirror-like top, bottom and side facets of the 1D nanocrystals act as good reflectors due to the material-related high refractive index, and facilitate their application as light sources and wave-guiding components [7, 8]. On that basis, core-multishell nanowire lasers with high emission efficiency at room temperature [9, 10, 11], single photon sources or polarization-entangled photon sources realized via quantum-dot nanowires [12, 13, 14] as well as optical interconnects for photonic circuits and optical data transfer [15] have been presented. Moreover, core-multishell nanowire light-emitting diodes (LEDs) with emission in the near infrared range have been demonstrated [16, 17]. Tuning of the thickness or composition of the active light-emitting shell region allows one to shift the emission towards larger wavelengths, and enables access to the telecommunication bands, which cannot be realized with thin films. Exploiting the reverse concept of a III-V semiconductor light source, photoconductive detectors [18, 19] as well as photovoltaic cells [20, 21, 22] based on III-V nanowires moved into focus of research activities. In particular, the high aspect ratio makes III-V nanowires attractive candidates for photovoltaic cells with higher light absorption efficiency compared to thin films due to concentration of light in the standing nanowires [22]. Therefore, III-V nanowire photovoltaic cells have been suggested as independent power supplies for self-powered Si chips [23]. Furthermore, III-V nanowire sensors have been demonstrated for detection of gases and chemical compounds [24, 25] since they offer higher sensitivities compared to thin films due to their large surface-to-volume ratio, which paves the avenue towards on-chip detection and nanoanalytics. Finally, III-V nanowires have been proposed for an application as thermoelectric cooling elements because they exhibit a reduced thermal conductivity due to strong phonon scattering mechanisms [26, 27].

Besides the potential of III-V nanowires for future (opto)electronic devices, new device architectures are required to overcome the physical limitations in top-down scaling of the conventional Si-CMOS FETs. III-V nanowires are proposed by the *International Technology Roadmap for Semiconductors* to replace the planar Si transistor channel, and to enable gate lengths of 10 nm and below for one-dimensional ballistic transport [28, 29]. Vertical III-V nanowire FETs in gate-all-around configuration grown on the Si platform represent the most promising architecture scheme for nanowire transistors [4, 5, 29].

Despite the recent progress in the development of nanowire-based (opto)electronic devices and device architectures, most of the aforementioned achievements are considered as proof-of-concept laboratory studies and much more basic research is required in order to make the monolithic integration of III-V nanowires fully compatible with the industrial Si platform. One pre-requisite is defect-free and high-quality growth of III-V nanowires on Si while simultaneously meeting the industrial Si-CMOS processing standards. For this purpose, a better understanding of the nucleation and growth mechanism of III-V nanowires on Si substrates is required in order to control the growth of nanowires and to tune their properties.

The present dissertation focuses on the self-catalyzed vapor-liquid-solid (VLS) growth of GaAs nanowires and GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ axial nanowire heterostructures on the Si platform using molecular beam epitaxy (MBE). In the self-catalyzed (Ga-assisted) growth mode, nano-sized liquid Ga droplets are employed to drive the nanowire growth. The demonstration of self-catalyzed growth of GaAs nanowires in 2008 [30, 31] was an important milestone towards CMOS-compatible integration of GaAs-based nanowires on the Si platform because the use of external and absolutely incompatible growth catalysts, such as Au, has been eliminated.

During the past decade, many efforts have been undertaken to control the self-catalyzed growth of GaAs nanowires on Si substrates. Nevertheless, several challenges in the conventional growth processes still exist: That is, (i) insufficient control of the nucleation stage of GaAs nanowires on the substrate due to non-synchronized nanowire nucleation, which in turn, leads to non-uniform

nanowire ensembles with a broad length distribution, (ii) low number yields of vertical GaAs nanowires owing to unintentional growth of faceted GaAs islands, (iii) the inability to control the number density of GaAs nanowires in a wide range without *ex situ* patterning of the substrate, (iv) the inability to control the nanowire diameter independent of their number density, (v) growth reproducibility issues, (vi) limited CMOS-compatibility of the self-catalyzed growth due to relatively high growth temperatures exceeding the industrial Si-CMOS processing standards, (vii) GaAs nanowires with structural polytypes and stacking faults due to an inadequate control of the crystal structure, (viii) the inability to interrupt or terminate the growth without formation of stacking faults, (ix) insufficient control of the thickness, composition and interface sharpness of $Al_xGa_{1-x}As$ ternary sections in $GaAs/Al_xGa_{1-x}As$ axial nanowire heterostructures.
The first aim of this dissertation is to address and overcome the aforementioned challenges in conventional growth processes by developing and investigating original methods for substrate preparation and nanowire growth. In Chapter 4, a new method denoted as surface modification procedure (SMP) has been developed for the *in situ* preparation of Si substrates. By employing the SMP on the substrate prior to nanowire growth, it will be shown that the existing growth challenges (i) to (v) can be successfully tackled. Additionally, it will be demonstrated that the SMP is beneficial for growth of GaAs-based nanowires with high structural quality. In Chapter 5, a novel growth method called droplet-confined alternate pulsed epitaxy (DCAPE) has been developed for the self-catalyzed growth of GaAs nanowires and $GaAs/Al_xGa_{1-x}As$ axial nanowire heterostructures on Si substrates. Using DCAPE instead of conventional growth processes, it will be shown that the ascribed growth challenges (vi) to (ix) can be resolved. Basic information for a better understanding of the context will be given in the beginning of Chapters 4 and 5.
The second aim of this dissertation is to elaborate and provide a fundamental understanding of the physical mechanisms involved in the self-catalyzed nucleation and growth of GaAs-based nanowires on Si substrates. In Chapter 4, it was possible to study the nucleation kinetics of the Ga droplets on SiO_x, the interaction between the Ga droplets and the SiO_x, and the growth of SiO_x openings at high temperatures during the development of the SMP. The pre-growth treatment of the substrate further enabled the observation of a self-narrowing effect (the so-called nucleation antibunching) on the length distribution of GaAs nanowires, which confirms theoretical predictions about temporally anti-correlated nucleation events in VLS-grown III-V nanowire ensembles.
Chapter 2 deals with a general introduction to crystal growth of III-V nanowires on lattice-mismatched substrates. Basic knowledge about the growth mechanism of self-catalyzed GaAs nanowires on Si substrates as well as the evolution of the length distribution and crystal structure in VLS-grown III-V nanowire ensembles is provided. Furthermore, an overview about challenges in the VLS growth of III-V axial nanowire heterostructures is given. Chapter 3 deals with a general description of the growth technique of MBE and the physical characterization methods employed for analysis of the droplet and nanowire samples produced within this research study. The dissertation is concluded in Chapter 6 by summarizing and evaluating the presented results, and by deducing new aspects for future activities in this field of research.

2 Fundamentals of Crystal Growth of III-V Nanowires on Si

This chapter presents fundamental aspects of crystal growth of III-V nanowires on lattice-mismatched Si substrates. An overview about material-related properties of III-V semiconductors is given in Chapter 2.1, and possibilities for engineering of their band gaps are outlined therein. Inherent constraints in thin film growth of III-V semiconductors on lattice-mismatched substrates are described in Chapter 2.2, and the use of nanowires in their place is highlighted. Furthermore, the concept of VLS growth for bottom-up synthesis of III-V nanowires is introduced in Chapter 2.3. In particular, the common understanding of self-catalyzed growth of GaAs nanowires on Si substrates is described including atomistic processes on the substrate surface as well as the physical mechanism of nanowire growth. The theoretical evolution of length distribution in VLS-grown III-V nanowire ensembles and its broadening and narrowing mechanisms are elaborated in Chapter 2.4. The crystal structure of III-V nanowires and its influencing parameters during VLS growth are discussed in Chapter 2.5. Finally, possibilities and challenges in VLS growth of III-V axial nanowire heterostructures are outlined in Chapter 2.6.

2.1 III-V Semiconductors

III-V compound semiconductors offer superior (opto)electronic properties compared to Si, in particular, direct band gaps and high electron mobilities, which emphasize their application as suitable materials in (opto)electronic devices. For the development of (opto)electronic devices, tuning of the basic material properties of III-V semiconductors, i.e. lattice parameter, band gap, refractive index, and optical emission and detection wavelength, is of fundamental importance in order to access, cover and transmit a broad spectral range. Band gap tuning may be realized through different strategies, such as appropriate material selection and combination, size tuning of nanostructures (i.e. nanodots/nanowires), alloying, or application of strain. The simplest approach is based on the combination of various binary III-V materials, each of which offers a unique material-dependent band gap. Binary III-V compound semiconductors are composed of two different types of atoms, i.e. a group-III element (e.g. Al, Ga, In) and a group-V element (e.g. N, P, As, Sb) of the periodic table. Their regular periodic arrangement in the crystal, which is defined by the lattice parameter, represents a minimum of the total internal energy. Depending on the group-V element, III-V semiconductors are further classified into sub-groups such as III-nitrides, III-phosphides, III-arsenides and III-antimonides. With all III-V semiconductors, a spectral range from 200 nm (AlN: 6.2 eV) to 7.3 μm (InSb: 0.17 eV) can be covered at 300 K.

2.1.1 Fundamental Properties of III-Arsenides

Within the sub-group of III-arsenides, GaAs is the most prominent representative next to InAs and AlAs. GaAs and InAs exhibit a direct band gap of 1.42 eV and 0.35 eV at 300 K, respectively. Moreover, an electron mobility as high as $\sim$8000 cm^2/Vs at 300 K has been obtained in weakly doped n-type bulk GaAs [32]. In contrast, Si reveals an indirect band gap of 1.11 eV at 300 K. N-type bulk Si typically exhibits an electron mobility not larger than ~1500 cm^2/Vs at 300 K [33, 34]. This demonstrates that III-arsenides are attractive materials for light emitters and photodetectors as well as high frequency devices with faster switching rates and less power consumption compared to Si-based electronic devices.

III-arsenide compounds crystallize in the cubic zinc blende structure. The atomic arrangement of the cubic unit cell is representatively depicted for GaAs in Fig. 2.1 (a).

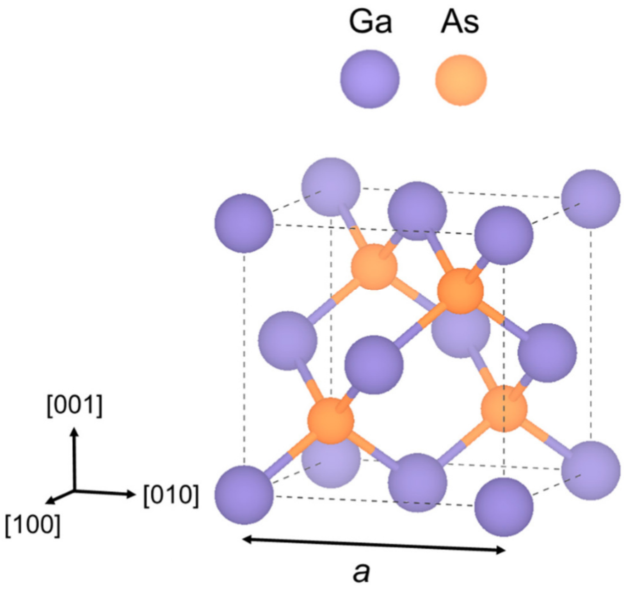

Fig. 2.1: Arrangement of Ga and As atoms inside the cubic unit cell of GaAs. For visualization, the software *VESTA* was used [35].

a is the lattice parameter of the cubic unit cell. The Ga atoms are arranged in a face-centered configuration. The crystal structure of GaAs consists of two interlaced face-centered cubic sublattices, one of Ga and the other of As atoms, displaced by $(\sqrt{3}/4) \times a$ along the diagonal [111] of the unit cell. Each atom forms four bonds in a tetrahedral configuration with a constant angle of 109.5° between all Ga–As bonds. The bond type between Ga and As atoms is a mixture of weak polar (ionic) bonds, that are caused by the difference in the electronegativity of the atoms, and tetrahedral sp^3 covalent bonds due to the electron configuration and radius of the atoms. GaAs exhibits a lattice parameter of a_{GaAs}=5.6533 Å at 300 K [36].

The relationship of the band gap energies and the lattice parameter for all III-arsenides is depicted in Fig. 2.2. As seen, the band gap energies are determined by the lattice parameter, or equivalently size of the crystal. The latter is the result of minimization of the total energy during crystal growth, and strongly depends on the type of atoms in the crystal.

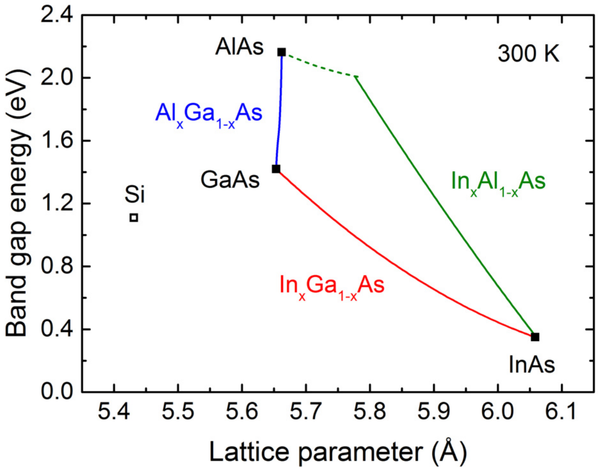

Fig. 2.2: Band gap energy of III-arsenide semiconductors as a function of the lattice parameter at 300 K. Solid (dashed) lines represent direct (indirect) band gaps. The values of the ternary alloys were calculated using the empirical relation of *Vegard's* rule.

Another common approach for band gap tuning of binary III-V semiconductors is based on a compositional change, or equivalently, alloying. Alloying is realized by adding a third or fourth group-III and/or group-V element in order to create a ternary or quarternary III-V compound semiconductor, for instance group-III-arsenide ternary alloys (e.g. $Al_xGa_{1-x}As$, $In_xGa_{1-x}As$, $In_xAl_{1-x}As$), or group-V ternary alloys (e.g. $GaAs_xP_{1-x}$, $InAs_xSb_{1-x}$). In this case, tuning of the band gap is achieved by changing the size and electronic structure of the crystal due to replacement of existing atoms with another type of atoms. The change of the lattice parameter depends on the fraction x of the foreign atoms. Using *Vegard's* rule [37], the average lattice parameter a of a ternary alloy $A_xB_{1-x}C$, that consists of three different atomic species A, B and C, can be estimated empirically by

$$a = a_{BC} + (a_{AC} - a_{BC}) \cdot x, \tag{2.1}$$

where a_{BC} and a_{AC} are the lattice parameters of the binary III-V compounds AC and BC. The resulting average band gap energy E_g of the ternary alloy is then given empirically by

$$E_g = x \cdot E_{g(AC)} + (1-x) \cdot E_{g(BC)} - b_{ABC} \cdot x \cdot (1-x) \tag{2.2}$$

with $E_{g(AC)}$ and $E_{g(BC)}$ being the band gap energies of the binary III-V compounds AC and BC, and b_{ABC} the bowing coefficient. A third strategy for band gap tuning of binary III-V semiconductors relies on the expansion or compression of the lattice parameter without compositional change. Growth of dissimilar semiconductors in heterostructures inherently induces strain as a result of the accommodation of the lattice mismatch. Moreover, external application of strain to the crystal subsequent to its growth also can be used to tune the band gap.

2.1.2 Quantum Heterostructures

Alloying and the combination of various III-V materials, for instance a binary with a ternary compound, paves the way for the design and fabrication of quantum heterostructures. Among the ternary III-arsenides, $Al_xGa_{1-x}As$ and $In_xGa_{1-x}As$ alloys are typically used in quantum heterostructures. Single heterostructures represent the simplest case of a quantum structure. They are made by putting together two different III-V materials. A prominent example is the two-dimensional electron gas, which is confined in modulation-doped single heterostructures such as lattice-matched GaAs/$Al_xGa_{1-x}As$ or $In_xGa_{1-x}As$/$In_xAl_{1-x}As$ (with x_{In}=0.53). Due to spatial separation of the electrons from their donors and thus, reduced scattering, a higher electron mobility compared to bulk material can be obtained. This is the basis for many electronic devices, for instance high-electron-mobility FETs. Double heterostructures are made of a III-V material with a lower band gap sandwiched between another III-V material with a wider band gap. If these materials are grown as stacked layers with a thickness of the intermediate layer comparable to the *de Broglie* wavelength of the electrons, a quantum well is formed. The holes and electrons can move freely in the plane of the layer, but are confined perpendicular to the plane and occupy discrete bound states in the valence and conduction band, respectively. The GaAs/$Al_xGa_{1-x}As$ material system is a prominent example for a quantum well structure because the band gap can be tuned in a relatively wide range of 2.16 eV ($Al_xGa_{1-x}As$ with $x_{Al} < 0.43$ for a direct band gap) and 1.42 eV (pure GaAs) depending on the Al-content x_{Al} without change of the crystal size or lattice parameter between the two end-point binaries AlAs and GaAs (see Fig. 2.2). The electronic band structure of a single GaAs/$Al_xGa_{1-x}As$ quantum well is schematically shown in Fig. 2.3.

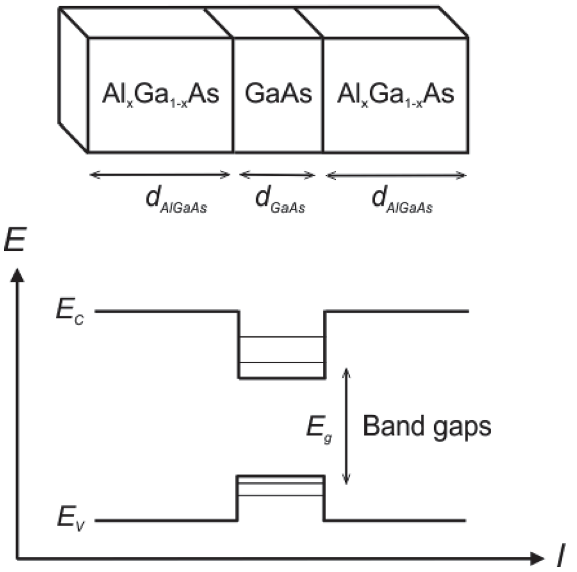

Fig. 2.3: Band diagram of a single GaAs/$Al_xGa_{1-x}As$ quantum well.

Double heterostructures are used for optoelectronic devices such as LEDs, lasers, solar cells and photodetectors. Complex quantum heterostructures, for instance periodically stacked thin quantum well structures known as superlattices are the basis for quantum cascade lasers and

THz devices. Quantum heterostructures can also be realized by compositional variation of the III-V material in low-dimensional structures such as quantum wires and quantum dots. The free carrier motion may be additionally confined by the small size of these structures.

2.2 Heteroepitaxial Growth of III-V Semiconductors on Si

III-V semiconductor crystals are synthesized via epitaxial growth. The growth process of a crystalline layer on a crystalline substrate, in which the atoms of the growing layer adopt the atomic arrangement of the underlying substrate is known as *epitaxy*. Liquid phase epitaxy as well as vapor phase epitaxy such as MBE or metal-organic chemical vapor deposition (MOCVD) are commonly employed for growth.

2.2.1 Misfit Accommodation and Plastic Relaxation in Epilayers

III-V semiconductors are typically grown on crystalline substrates of the same material (homoepitaxy) or different material (heteroepitaxy). In heteroepitaxy, the different thermal expansion coefficients and lattice parameters of the semiconductors result in a thermal and structural misfit. Lattice misfit f is defined by

$$f = \frac{a_{lay} - a_{sub}}{a_{sub}}, \tag{2.3}$$

where a_{sub} and a_{lay} are the unstrained lattice parameters of the substrate crystal and the grown epilayer in the plane of the interface [36]. For instance, the different lattice parameters of InAs, GaP and InP produce a lattice misfit with Si of 11.6% (largest misfit among III-Vs), 0.4% (smallest misfit among III-Vs) and 8.1%, respectively [38]. Lattice misfit creates stress at the interface of the growing epilayer with the rigid substrate. If $a_{lay} > a_{sub}$ (or $f > 0$), the epilayer develops biaxial compressive strain. In the opposite case, if $a_{lay} < a_{sub}$ (or $f < 0$), the epilayer is subject to biaxial tensile strain. During strain accumulation, elastic energy is stored in the epilayer, which increases as the thickness of the layer rises. At a critical thickness, the elastic energy is larger compared to the energy required to form structural defects [36]. In this case, it is energetically favorable to partially or fully release the strain of the epilayer via formation of misfit dislocations. Misfit dislocations are line defects of edge type, which are created at the interface of lattice-mismatched III-V materials. They can be described by removal or insertion of lattice planes in the case of plastic relaxation of biaxial compressive or tensile strain, respectively. Since dislocations can neither begin nor end within a crystal, their ends must lie at the surface of the epilayer [36]. Therefore, misfit dislocations evolve into threading dislocations, which glide or climb along certain crystallographic planes to the surface of the epilayer and finally create large dislocation networks [39]. Thus, depending on the thickness of the epilayer, lattice misfit can be accommodated by elastic or plastic relaxation of the epilayer. Heteroepitaxial growth of elastically relaxed III-V layers without formation of structural defects is referred to as pseudomorphic growth. The strained layers are denoted as coherent epilayers. In this case, the lattice misfit is equal to the biaxial strain of the epilayer [36]. On the other hand, heteroepitaxial growth of III-V layers with formation of structural defects is known as metamorphic growth. These plastically relaxed layers are called incoherent epilayers.

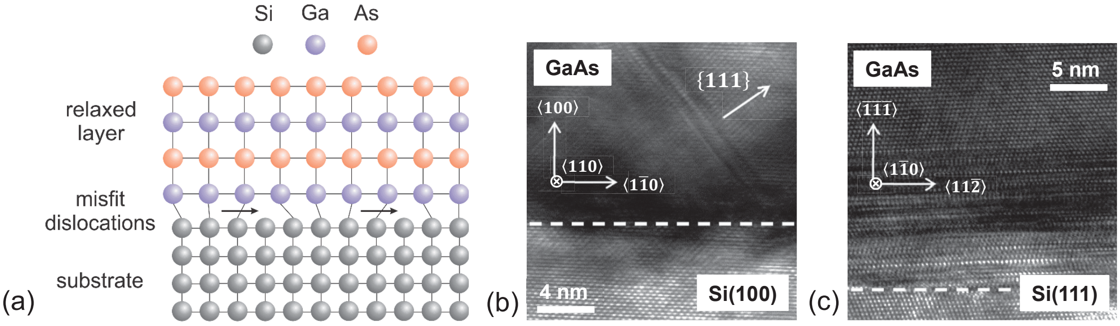

Fig. 2.4: Heteroepitaxial growth of GaAs epilayers on Si substrates. (a) Schematic illustration of the GaAs/Si interface. (b), (c) Cross-sectional HRTEM image of the interface of a GaAs epilayer grown on a Si(100) substrate (b) and on a Si(111) substrate (c). The GaAs/Si interfaces are depicted as dashed lines. Figs. 2.4 (b) and (c) are adapted from [39] and [40], respectively.

Metamorphic growth of incoherent III-V epilayers is representatively depicted for the GaAs/Si material system in Fig. 2.4. The GaAs/Si system exhibits a lattice misfit of 4.1% and a thermal expansion coefficient misfit of 62% [41]. Since $a_{GaAs} > a_{Si}$, the GaAs epilayers develop biaxial compressive strain. A critical thickness of 6.5 nm was reported for GaAs epilayers on Si substrates [42]. As schematically shown in Fig. 2.4 (a), two existing planes are virtually removed for plastic relaxation of a strained GaAs epilayer. Threading dislocations, that move along the {111} planes, are shown by the high-resolution transmission electron microscopy (HRTEM) image of a GaAs epilayer on a Si(100) substrate in Fig. 2.4 (b). In the case of a Si(111) substrate as illustrated in Fig. 2.4 (c), planar defects denoted as twin planes (see Chapter 2.5.1 for a detailed explanation) are formed parallel to the GaAs/Si interface. Any type of lattice defect acts as scattering center for charge carriers, degrades the material properties, and leads to an altering device performance or early device failure.

Another challenge in III-V/Si heteroepitaxy is that the substrate exhibits another crystal structure as the epilayer. Si shows a diamond structure with two interlaced face-centered-cubic sublattices occupied by the same type of atoms. Due to the bonding electrons, that are shared equally between each Si atom and its four neighboring atoms, Si is a non-polar material. In contrast, III-V compounds crystallize in the zinc blende structure (or wurtzite structure for III-nitrides) occupied by two different types of atoms with different electronegativity as described in Chapter 2.1.1. Thus, each atom is tetrahedrally surrounded by atoms of opposite polarity resulting in a polar character of the materials. Due to the lack of inversion symmetry along specific orientations (e.g. ⟨111⟩), antiphase domains with antiphase boundaries may emerge during growth of polar III-V materials on the non-polar Si substrate [43, 44]. Antiphase boundaries evolve as a plane of wrong bonds, i.e. III–III or V–V bonds. They act as non-radiative recombination centers or leakage paths, and may induce spectral broadening, photoluminescence quenching or degraded electron mobilities in (opto)electronic devices [43]. Thus, fully relaxed metamorphic

III-V epilayers are not favorable for the fabrication of high-performance (opto)electronic devices on Si due to dislocation networks and other types of structural defects.

2.2.2 Dislocation-Free Growth of Vertical Nanowires

In contrast to epilayers, III-V nanowires can be grown free of misfit dislocations on highly lattice-mismatched substrates due to their small diameter and interface area with the substrate as shown in Fig. 2.5 (a). As long as the interface area with the substrate stays below a critical material-dependent value, the lattice misfit can be accommodated via elastic relaxation through the lateral free surfaces of the nanowire sidewalls [38, 45, 46].

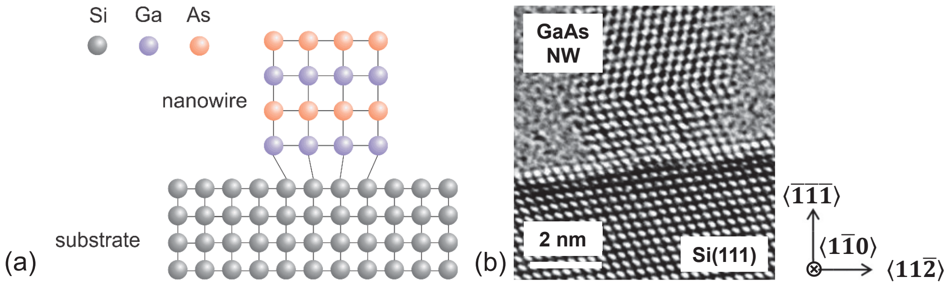

Fig. 2.5: Heteroepitaxial growth of a GaAs nanowire on a Si substrate. (a) Schematic illustration of the GaAs/Si interface. (b) Cross-sectional HRTEM image of the interface of a GaAs nanowire grown on a Si(111) substrate. Fig. 2.5 (b) is adapted with permission from [47]. Copyright (2017) American Chemical Society.

This is schematically depicted in Fig. 2.5 (a) for the GaAs/Si system with biaxial compressive strain. The inherent relief of strain energy in III-V nanowires has opened the promising route for the monolithic integration of III-V materials on the mainstream and cost-effective Si platform and moreover allows great flexibility in substrate selection.

When III-V nanowires commonly adopt the cubic zinc blende structure, crystallization is energetically favorable along the ⟨111⟩ crystallographic directions due to the lower Gibbs free energy of nucleation compared to the ⟨110⟩ and ⟨112⟩ directions [48]. Thus, growth of III-V nanowires on Si(111) substrates naturally leads to bottom-up synthesis of free-standing and vertically aligned 1D nanocrystals as illustrated in Figs. 2.6 (a) and (b), which is highly advantageous for the fabrication of III-V nanowire-based (opto)electronic devices on the Si platform. Besides the vertical ⟨111⟩ growth direction, another three equivalent ⟨111⟩ growth directions exist, where the nanowires grow under an angle of 19.5° with respect to the substrate surface. Their projections on the (111) plane of the substrate are rotated by 120°. As shown in Figs. 2.6 (c) and (d), nanowire growth on Si(100) substrates takes place in four equivalent ⟨111⟩ growth directions under an angle of 35.3° with respect to the substrate, and their projections on the (100) plane are rotated by 90° around the surface normal. If Si(110) substrates are used, two equivalent ⟨111⟩ growth directions exist as illustrated in Figs. 2.6 (e) and (f), which form an angle of 54.7° with the substrate. Their projections on the (110) plane are rotated by 180° around the surface normal of the substrate.

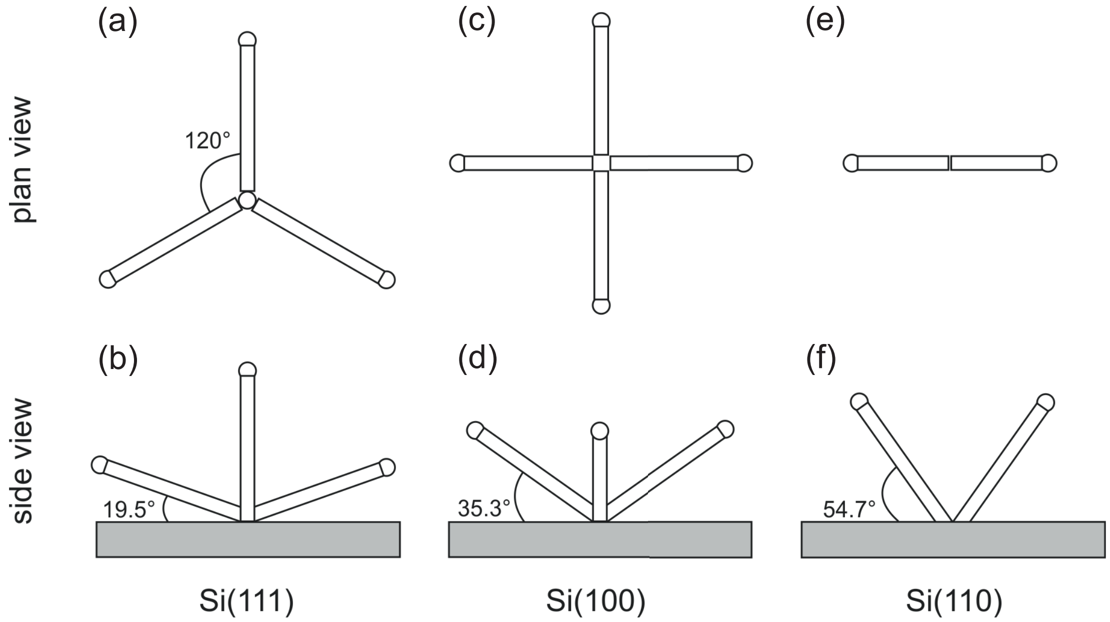

Fig. 2.6: Schematic illustration of $\langle 111 \rangle$ growth directions of III-V nanowires in plan-view and side-view on (a), (b) Si(111), (c), (d) Si(100), and (e), (f) Si(110) substrates respectively. Adapted from [49].

Furthermore, the crystal orientation of the substrate determines the shape of the nanowires. In this work, Si(111) substrates are exclusively used for the growth study of GaAs nanowires due to their vertical alignment on the substrate. On Si(111) substrates, as-grown nanowires are surrounded by six sidewalls of the $\{1\bar{1}0\}$ family as illustrated representatively in Fig. 2.7 for GaAs nanowires.

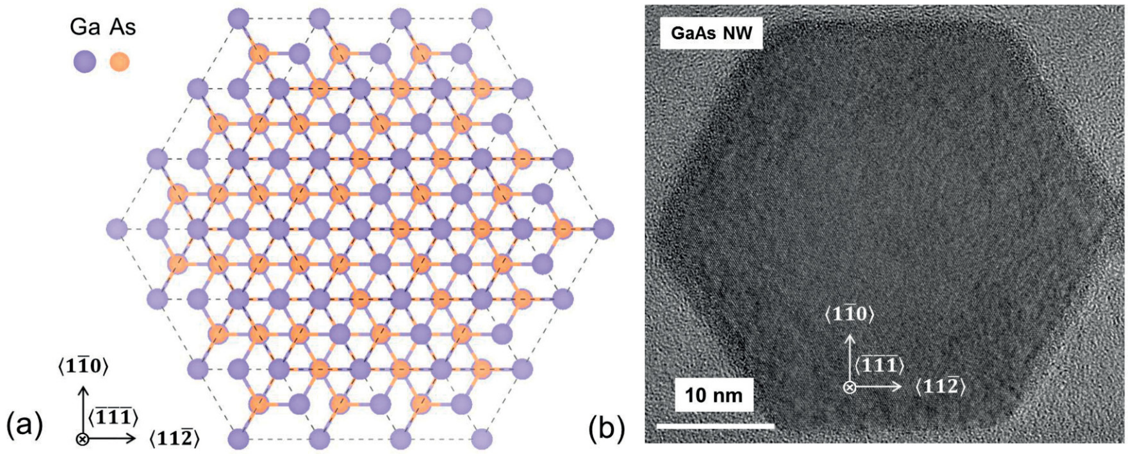

Fig. 2.7: Hexagonal cross-section of GaAs nanowires grown on Si(111) substrates. (a) Bonding configuration of Ga and As atoms in the (111) plane. For visualization, the software *VESTA* was used [35]. (b) Cross-sectional HRTEM image of a GaAs nanowire.

2.3 Self-Catalyzed Vapor-Liquid-Solid (VLS) Growth of GaAs Nanowires on Si(111) by Molecular Beam Epitaxy

All nanowires in this dissertation were grown in the self-catalyzed vapor-liquid-solid mode. VLS growth proceeds in the presence of three thermodynamic phases. That is, a GaAs solid phase (S) grows on a Si substrate from a Ga-As_4 vapor phase (V) in the presence of a Ga liquid phase (L) (see Fig. 2.8 (iv)).

VLS growth has been introduced by *Wagner* and *Ellis* in 1964 as a new technique of crystal growth from a vapor phase, which produces filamentary 1D crystals in presence of small liquid catalyst droplets at their tips. Initially, VLS growth has been demonstrated for micrometer-thick and millimeter-long Si whiskers on Si(111) substrates using Au as the catalyst, which forms an eutectic alloy with Si [50, 51]. In this early work, the self-catalyzed VLS growth mode has already been suggested for growth of III-V whiskers [50]. In 1965, Au-catalyzed VLS growth of GaAs and GaP whiskers on GaAs substrates was presented [52]. In the same study, self-catalyzed growth of GaAs whiskers from pure Ga droplets has been performed, but did not result in the desired morphology. Later works reported self-catalyzed growth of GaAs and GaP whiskers on GaAs films/substrates or GaP films respectively, but growth was not intended and the whiskers considered as a type of defect [53, 54, 55]. In the 1990s, whisker growth has been extended to nanowires, when growth on the nanometer scale was possible [56]. While the rediscovery of Au-catalyzed growth of III-V nanowires was in progress, first systematic investigations of self-catalyzed growth of GaAs nanowires, initially on GaAs(111)B and then on cleaved facets of Si(100) substrates, were performed in 2008 [30, 31, 57].

Self-catalyzed growth of GaAs nanowires on the Si platform has been proven very beneficial compared to Au-catalyzed growth because it avoids the potential contamination of both the nanowire and substrate crystal with Au. It has been shown that Au atoms were incorporated unintentionally in III-V nanowires [58, 59] with concentrations in the order of 10^{17}-10^{18} cm^{-3} [58]. Au impurities create deep energy levels in the band gaps of both the semiconductor nanowires and the Si substrate, which alters the performance and reliability of nanowire-based (opto)electronic devices. Especially, the diffusion of Au into the substrate, for instance during thermally activated post-growth processing steps, is a high risk and the reason why Au-catalyzed growth is absolutely incompatible with the standard Si-CMOS-technology. Moreover, Si has a high solubility inside Au particles, which may lead to unwanted doping of the nanowires with Si from the substrate [60]. For all those reasons, the demonstration of Au-free self-catalyzed growth of GaAs nanowires in 2008 fulfills an important requirement for CMOS-compatible integration of GaAs-based nanowires on the mature Si platform.

2.3.1 The Role of SiO_x

Fontcuberta i Morral *et al.* have found that a thin Si oxide layer on top of a GaAs(111)B substrate was the key ingredient to facilitate self-catalyzed nucleation and growth of GaAs nanowires on the substrate [30]. In consecutive investigations, which were performed on Si(111) substrates, it has been further demonstrated, that self-catalyzed growth of GaAs nanowires on bare Si (without a Si oxide layer) is not possible at all, and rather results in the overgrowth of the substrate with faceted pyramidal GaAs crystals [61]. Moreover, it has been shown that the success of nanowire nucleation and growth is strongly affected by the physical properties of the Si oxide layer. That is, the type of surface oxide and its chemical composition (i.e. native-SiO_x, thermally grown SiO_2, chemically produced SiO_x), the oxide thickness, and the surface roughness [61]. The native-SiO_x has been reported to be highly suitable for the nucleation and growth of self-catalyzed GaAs nanowires, because it provides (i) surface sites for the nucleation of Ga droplets [30, 57, 62, 63], (ii) an enhanced surface mobility of Ga adatoms in contrast to bare Si substrates (i.e. a larger diffusion coefficient) [61, 64], (iii) excellent wetting properties, which favor the formation of Ga droplets with appropriate contact angles for growth of vertical GaAs nanowires compared to bare Si substrates [65, 66], while simultaneously unwanted growth of a GaAs thin film or faceted GaAs crystals (denoted as parasitic growth) on the substrate surface is minimized [67]. Advantageously, native-SiO_x is naturally present on the surface of Si substrates. In contrast to chemically or thermally produced Si oxides, native-SiO_x/Si substrates can be directly used for growth studies without prior *ex situ* treatments.

2.3.2 The Double Role of Liquid Ga Droplets

Self-catalyzed growth of free-standing and vertically aligned GaAs nanowires on native-SiO_x/Si(111) substrates is typically performed under simultaneous and continuous supply of Ga and As beams (either As_4 or As_2) at temperatures (T_{gr}) in the range of 560 to 630 °C [68, 69]. It involves a complex interplay of various physical and chemical mechanisms, which take place in parallel on the substrate surface as illustrated in Fig. 2.8. That is,

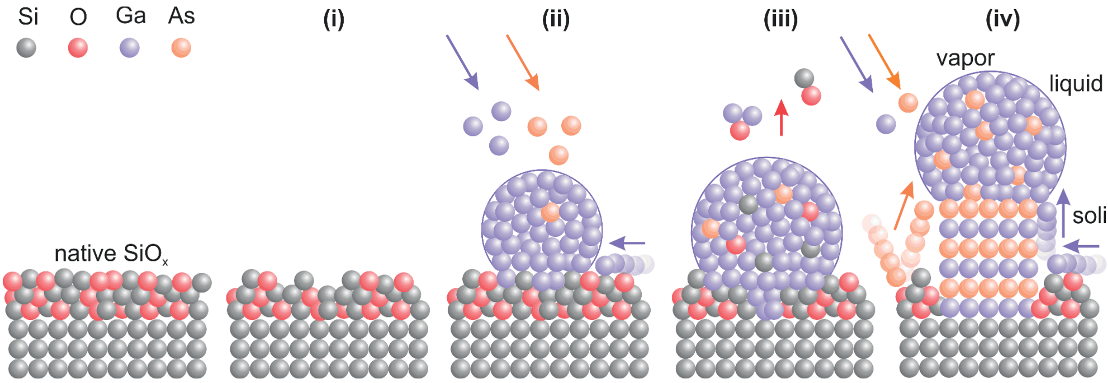

Fig. 2.8: Schematic illustration of the two roles of Ga droplets in the self-catalyzed growth of GaAs nanowires on native-SiO_x/Si(111) substrates. For sake of simplicity, the $As_{4/2}$ molecular species are depicted as single atoms.

(i) modification of the native-SiO_x during the initial thermal annealing of the substrate,

(ii) formation of nano-sized liquid Ga droplets on the SiO_x preferentially at the previously created pinholes via self-assembly [70],

(iii) interaction of the Ga droplets with the underlying SiO_x and formation of nano-sized holes underneath the droplets [30], and finally,

(iv) droplet-assisted nucleation and axial growth of GaAs nanowires inside the SiO_x holes directly on the exposed Si substrate.

The Ga-induced nanohole formation in step (iii), and the Ga-assisted nanowire nucleation in step (iv) take place simultaneously under the very same droplets, which clearly demonstrates the double role of the Ga droplets. The following section describes the formation of Ga droplets on native-SiO_x/Si substrates in step (ii) as well as the formation of SiO_x holes in step (iii).

2.3.3 Formation of Ga Droplets and Etching of Openings in SiO_x

During formation of Ga droplets on native-SiO_x/Si(111) substrates, various atomistic processes take place on the substrate surface as depicted in Fig. 2.9. That is,

(1) impingement of Ga atoms to the substrate and adsorption (requires activation energy E_{ad}),
(2) diffusion of Ga adatoms along the substrate (requires activation energy E_{diff}),
(3) agglomeration of Ga atoms at surface defects,
(4) formation and growth of Ga droplets,
(5) interaction of liquid Ga with the native-SiO_x, and
(6) desorption of Ga adatoms from the substrate.

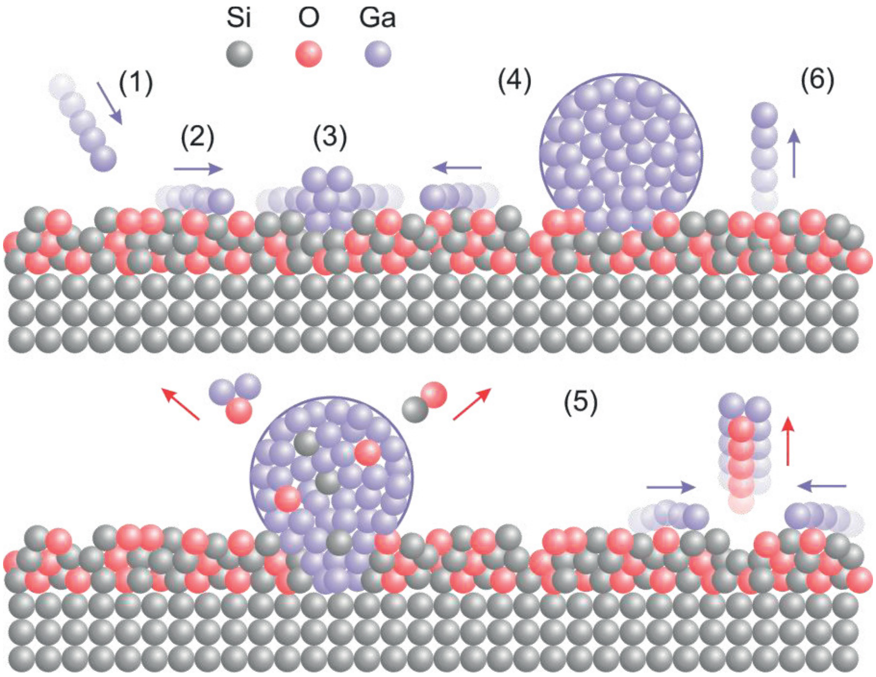

Fig. 2.9: Schematic illustration of physical and chemical processes during formation of Ga droplets on native-SiO_x/Si(111) substrates.

Processes (1), (2), and (6) are thermally activated mechanisms. Surface diffusion of Ga adatoms on the substrate in process (2) is the most crucial process in order to form liquid Ga droplets.

The migration distance of a Ga adatom along the substrate is denoted as surface diffusion length λ_{Ga} and can be expressed by

$$\lambda_{Ga} = \sqrt{D_c \tau_d} = \lambda_0 \cdot exp(\frac{E_{ad} - E_{diff}}{2k_B T}), \tag{2.4}$$

where T is the substrate temperature, D_c the diffusion coefficient (or diffusivity), τ_d the mean time for surface diffusion, and λ_0 a pre-exponential factor that takes into account the effective jump distance [36]. Surface diffusion and desorption of Ga adatoms are competing mechanisms. The relation between the substrate temperature T and the surface diffusion length λ_{Ga} is depicted in Fig. 2.10.

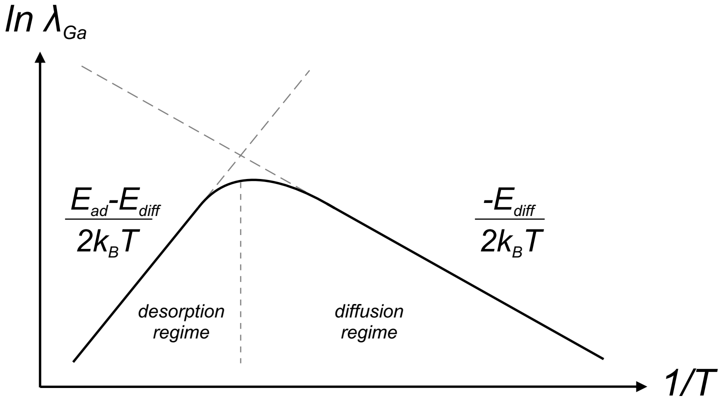

Fig. 2.10: Dependence of the surface diffusion length of Ga adatoms on the substrate temperature. Adapted from [36].

In the high temperature regime, λ_{Ga} decreases with T. The desorption of Ga adatoms from the substrate is more likely before being incorporated to a droplet, thus, their lifetime on the substrate is very short (desorption regime). In the low temperature regime, λ_{Ga} increases with T. The diffusion of Ga adatoms on the substrate and incorporation is dominant because the desorption is negligible and, thus, the lifetime of adatoms on the substrate is relatively long (diffusion regime). Finally, Ga droplets are formed via surface diffusion and capture of Ga adatoms at surface defects.

Assuming stable droplets on the surface (i.e. dissolution is negligible), the temporal evolution of the number density of diffusing Ga adatoms N_{at} and the number density of Ga droplets N_{dr} can be described by the rate equations

$$\dot{N}_{at}(t) = F_{Ga} - D_c \cdot N_{at} \cdot (2\sigma_{at} N_{at} + \sigma_{dr} N_{dr}), \tag{2.5}$$

$$\dot{N}_{dr}(t) = D_c \cdot \sigma_{dr} \cdot {N_{dr}}^2, \tag{2.6}$$

where F_{Ga} is the Ga flux, D_c the diffusion coefficient and σ_{at} and σ_{dr} the capture numbers of Ga atoms and droplets, respectively [71]. The capture number represents the depletion of the atom density around the droplets [71]. N_{at} increases due to arriving Ga atoms on the substrate at a constant rate F_{Ga}, and N_{at} decreases due to nucleation, capture and desorption at mean times τ_n, τ_c and τ_a, respectively. The temporal evolution of N_{at} and N_{dr} is schematically depicted in Fig. 2.11. In the high temperature regime (Fig. 2.11 (a)), loss of Ga adatoms from the substrate by desorption is dominating, and nucleation and capture are negligible. For $t < \tau_a$, N_{at} increases with t. For $t > \tau_a$, N_{at} is constant, reflecting the balance of arriving and desorbing atoms on the substrate without nucleation. N_{dr} increases for $t \geq \tau_a$, and finally, for $t \gg \tau_a$, both N_{at} and N_{dr} decrease due to coalescence of droplets. In the low temperature regime (Fig. 2.11 (b)), nucleation and capture processes are relevant, while desorption is negligible. For $t < \tau_c$, N_{at} increases with t. At $t{=}\tau_c$, N_{at} reaches its maximum and decreases subsequently due to capture of adatoms at previously nucleated droplets. N_{dr} increases after a nucleation time and finally decreases due to coalescence of droplets.

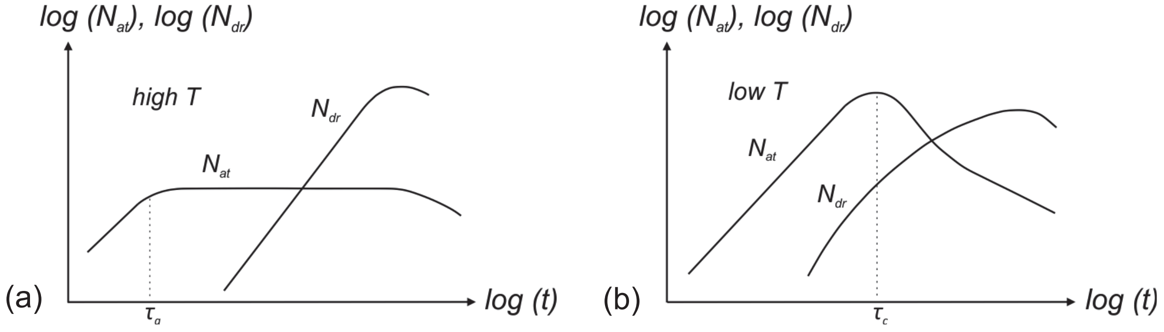

Fig. 2.11: Temporal evolution of the number density of Ga adatoms and Ga droplets on the substrate at high temperatures (a) and low temperatures (b). Adapted from [36].

Based on classical nucleation theory, the dependence of N_{dr} on T can be described by [71]

$$N_{dr} \propto {F_{Ga}}^p \cdot exp(\frac{-E_p}{k_B T}). \tag{2.7}$$

p and E_p are material-dependent parameters and represent the critical size of a nucleus and the energy difference between adatoms and atoms attached to a droplet, respectively. F_{Ga} is the Ga flux and k_B the Boltzmann constant. As seen, N_{dr} is inversely proportional to T. Only one study has been reported so far that deals with the formation of Ga droplets on Si substrates with and without native-SiO$_x$ [63]. It was found that the droplet formation on bare Si(100) follows the classical nucleation theory with an indirect relation between T and N_{dr} and a direct relation between T and the droplet size. The size of the Ga droplets could be further tuned by the amount of deposited Ga. For substrates covered by a native-SiO$_x$, it was shown that N_{dr} is much more affected by T, i.e. a small variation of T by 20-30 °C resulted in a large change of N_{dr} by one order of magnitude. This finding was attributed to a correlation of N_{dr} with the roughness or surface defects in native-SiO$_x$. Interestingly, the droplet diameter was almost independent of T. Despite these basic investigations, a systematic study of the nucleation kinetics of Ga droplets on Si substrates covered by a native-SiO$_x$ is still lacking.

Another relevant process is the interaction of liquid Ga with native-SiO_x. In particular, two Ga adatoms react with one O atom of SiO_x to form Ga_2O as shown in process (5) in Fig. 2.9. The chemical reactions are described by the following reaction equations [72, 73].

$$4\ \mathrm{Ga(l)} + \mathrm{SiO_2(s)} \rightarrow 2\ \mathrm{Ga_2O(v)} + \mathrm{Si(s)} \tag{2.8}$$

$$\mathrm{Si(s)} + \mathrm{SiO_2(s)} \rightarrow 2\ \mathrm{SiO(v)} \tag{2.9}$$

$$2\ \mathrm{Ga(l)} + \mathrm{SiO_2(s)} \rightarrow \mathrm{Ga_2O(v)} + \mathrm{SiO(v)} \tag{2.10}$$

Excess Si atoms are dissolved inside the droplets, and further react with SiO_2 to SiO (Eq. 2.9). Both Ga_2O and SiO are volatile compounds, and easily desorb from liquid Ga or the substrate surface. The overall reaction equation is given by Eq. 2.10. As a result, liquid Ga etches the native-SiO_x at substrate temperatures in the range of 450 to 900 °C [72, 73, 74, 75]. In other words, Ga droplets can be used to locally drill nano-sized openings in SiO_x. Subsequent to droplet-induced formation of SiO_x holes in step (iii) of Fig. 2.8, it is the same Ga droplets that drive the nucleation and growth of GaAs nanowires on the underlying Si substrate under presence of As as shown in step (iv) of Fig. 2.8, which is described in detail in the following section.

2.3.4 Nanowire Growth Mechanism and Growth Kinetics

Crystal growth in MBE takes place far from thermodynamic equilibrium, where kinetic limitations have an important role. Thus, in the following section, the self-catalyzed VLS growth of GaAs nanowires using MBE is described by kinetic considerations. Nevertheless, some aspects of the VLS growth can be well described by thermodynamics, i.e. the driving force for crystallization of a GaAs solid phase from a Ga-$As_{4/2}$ vapor phase. Nanowire growth in VLS mode involves multiple physical mechanisms as illustrated in Fig. 2.12. That is,

(1) impingement and adsorption of Ga and $As_{4/2}$ (1a) on the substrate, (1b) on the nanowire sidewalls and (1c) on the Ga droplets (direct Ga and As fluxes),
(2) desorption of Ga and $As_{4/2}$ (2a) from the substrate, (2b) from the nanowire sidewalls and (2c) from the Ga droplets,
(3) surface diffusion of Ga adatoms (3a) on the substrate and (3b) on the nanowire sidewalls to the Ga droplets at the nanowire tip (diffusion Ga flux),
(4) desorption of Ga and $As_{4/2}$ (4a) from the substrate and (4b) from the nanowire sidewalls and recollection in the Ga droplets of adjacent nanowires (rebound Ga and As fluxes),
(5) nucleation and growth of GaAs monolayers when the droplet is supersaturated with $As_{4/2}$ (axial growth), and
(6) incorporation of Ga and As on the nanowire sidewalls (radial growth).

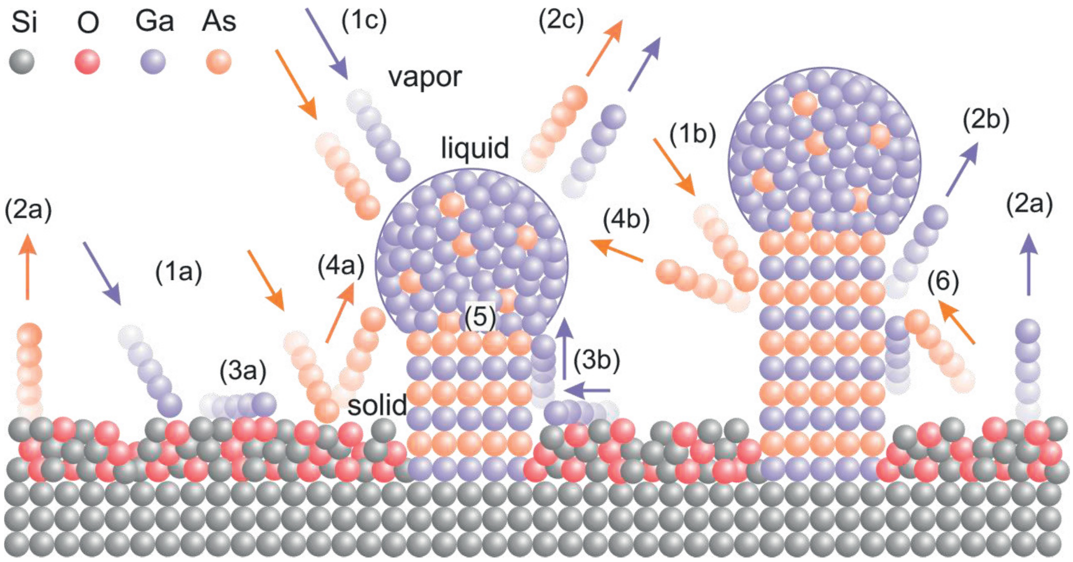

Fig. 2.12: Schematic illustration of physical processes during self-catalyzed VLS growth of GaAs nanowires on native-SiO_x/Si(111) substrates. For sake of simplicity, the $As_{4/2}$ molecular species are depicted as single atoms.

The common understanding of VLS growth of self-catalyzed GaAs nanowires on native-SiO_x/ Si(111) substrates is as follows. Ga droplets efficiently collect Ga and $As_{4/2}$ both from the direct incoming beams as well as from the material that diffuses along or desorbs from the substrate surface and the nanowire sidewalls. Only Ga contributes to the diffusion flux, surface diffusion of $As_{4/2}$ is negligible [76]. The flux of desorbed Ga and $As_{4/2}$ that is collected by the Ga droplets is called rebound flux. The ratio between the rebound and the diffusion fluxes is determined by the sticking coefficient of Ga and $As_{4/2}$ (S_{Ga}, $S_{As_{4/2}}$) on the substrate surface and the nanowire sidewalls and can be expressed by

$$S_{Ga(As_{4/2})} = \frac{k_{a(Ga(As_{4/2}))}}{k_{a(Ga(As_{4/2}))} + k_{d(Ga(As_{4/2}))}}, \tag{2.11}$$

where $k_{a(Ga)}$ and $k_{a(As_{4/2})}$ and $k_{d(Ga)}$ and $k_{d(As_{4/2})}$ are the adsorption and desorption rates of Ga and $As_{4/2}$ from the substrate, respectively [77]. S_{Ga} and $S_{As_{4/2}}$ strongly depend on the growth temperature, surface coverage and structural conditions of the substrate [78, 79]. While Ga atoms preferentially adsorb to the substrate, more specifically to the nanowire sidewalls, and diffuse along its surfaces, As_4 and As_2 molecules easily desorb from the substrate unless they are immediately captured on the surface by available Ga adatoms [80, 81]. In other words, on native-SiO_x/Si(111) substrates, $S_{As_{4/2}}$ is close to zero, whereas S_{Ga} is much larger than zero. From thin film growth, it is known that $S_{As_2} > S_{As_4}$ [79]. As a result, the substrate and nanowire sidewalls re-emit a significant amount of $As_{4/2}$ (origin of rebound As flux), a part of which is subsequently collected by the Ga droplets and contributes to axial growth [80]. The diffusion Ga and rebound As fluxes are directly proportional to the direct fluxes (F_{Ga}, F_{As}) and depend on the growth temperature. The large contribution of the diffusion Ga flux to axial growth (with growth rate GR_{ax}) is evidenced by the fact that GR_{ax}=50×F_{Ga}. On the other hand, we also found that GR_{ax}=3–4×F_{As}, which demonstrates the large contribution from the rebound As flux.

The concentration of $As_{4/2}$ (c_{As}) inside the droplets is approximately 1 at% and determined by the low solubility of $As_{4/2}$ in liquid Ga [76, 82]. c_{As} also depends on the growth temperature and on the droplet volume (Gibbs-Thomson effect) [76]. When more $As_{4/2}$ is added (supersaturation of the droplets with $As_{4/2}$), nucleation of GaAs takes place at the droplet/substrate interface. The growth of a complete monolayer involves the formation of a 2D nucleus and its instantaneous step-flow expansion along the liquid/solid interface [83]. Depending on c_{As} inside the droplets, one nucleation event triggers the formation of one monolayer of GaAs (mononuclear regime) [84, 83]. Subsequent to the nucleation event, the Ga droplets are depleted by the amount of $As_{4/2}$ that has been used for the formation of one monolayer, and need to be re-filled with $As_{4/2}$ from the incoming As fluxes. After the droplets have been re-filled again up to a critical c_{As}, the formation of another monolayer of GaAs takes place at the liquid/solid interface of the individual nanowire. As a result, VLS growth of self-catalyzed GaAs nanowires essentially operates in pulsed mode and in a layer-by-layer fashion at the liquid/solid interface of the nanowire and the axial growth rate is limited by the As flux [57, 76].

The thermodynamic driving force for crystallization of a GaAs solid phase from a Ga-$As_{4/2}$ vapor phase is the supersaturation. Supersaturation $\Delta\mu$ is defined as the difference in the chemical potential between the supply atoms and the growing surface [85], and can be expressed by

$$\Delta\mu = \mu_V - \mu_S, \tag{2.12}$$

where μ_V and μ_S are the chemical potentials of the vapor and solid phase, respectively [86]. Supersaturation is affected by the temperature, pressure and concentration of the supply atoms (i.e. c_{As}) at the liquid/solid interface [85]. The vapor-(liquid-)solid phase transition is induced by controlling the pressure in a way that μ_S is smaller than μ_V at a fixed temperature. If $\mu_S < \mu_V$, $As_{4/2}$ species from the vapor phase have to cross first the phase boundary to the liquid and then solid phase in order to allow the system to approach a new equilibrium by minimization of the Gibbs free energy. This is reached by spending a minimal energy to overcome the nucleation barrier given by the surface energy of the vertical edge of the GaAs nucleus at the liquid/solid interface [76]. According to Gibbs' phase rule, the self-catalyzed VLS growth cannot be thermodynamically stable due to the absence of a third element [87]. But it has been shown that it is dynamically stable, since the transport kinetics of the growth species lead to a kinetic self-regulation of the droplet size and thus, steady-state nanowire growth far from thermodynamic equilibrium [87].

In addition to VLS growth, III-V nanowires can be also synthesized by VS growth, without the use of a liquid droplet, where the nanowires grow directly from the vapor phase inside SiO_2 openings of pre-patterned Si substrates (selective area epitaxy), but they commonly suffer from a poor crystal quality [88, 89].

2.3.5 Nanowire Dimensions

Besides axial VLS growth of GaAs nanowires, radial VS growth of GaAs takes place by incorporation of Ga and As from the vapor phase on the nanowire sidewalls as depicted in process (6) of Fig. 2.12. The radial growth rate (GR_{rad}) is very low with respect to the axial growth rate (GR_{ax}), since the incoming material fluxes at the droplets are higher compared to the nanowire sidewalls. $As_{4/2}$ is incorporated into the surface of the nanowire sidewalls only when it is captured by diffusing Ga adatoms. The dependence of the length and radius of GaAs nanowires grown at T_{gr}=615 °C on the growth duration is plotted in Fig. 2.13. The growth rates are extracted from the slopes of the linear fits. As seen, GR_{ax}/GR_{rad}=185. The axial growth rate depends on the As flux, the growth temperature and the nanowire diameter. The nanowire length is controlled by the growth duration at a fixed axial growth rate.

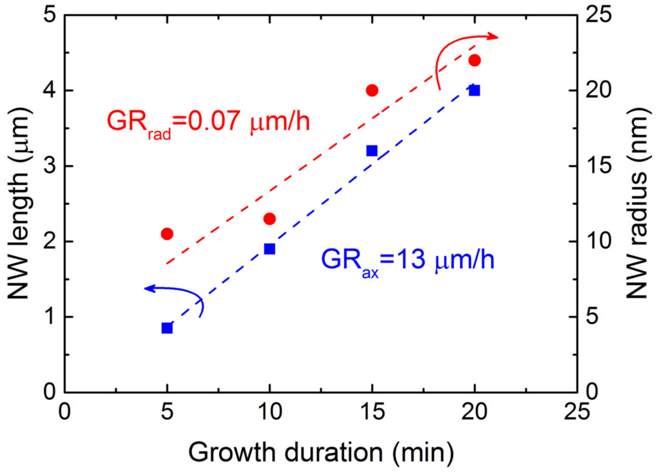

Fig. 2.13: Plot of the length (left axis) and radius (right axis) of GaAs nanowires as a function of the growth duration. The nanowires were grown at 615 °C under As-rich growth conditions using a V/III flux ratio of 11.

Typically, self-catalyzed growth of GaAs nanowires is performed under As-rich growth conditions ($F_{As} > F_{Ga}$, V/III flux ratio > 1). However, the local V/III ratio at the nanowire tip, more specifically at the liquid/solid interface, is typically 1 (after adding the diffusion and rebound fluxes). The nanowire diameter is dictated by the diameter and contact angle of the Ga droplet and can be expressed by

$$d_{NW} = 2r \cdot sin\theta, \tag{2.13}$$

where r is the droplet radius and θ the droplet contact angle [76]. The droplet size can be tuned by varying the V/III ratio. For high V/III ratios, the droplet volume decreases, while it increases for low V/III ratios, which leads to tapering (the nanowire diameter decreases along the growth direction) or inverse tapering (the nanowire diameter increases along the growth direction) [87]. The degree of tapering of the nanowire t_{NW} is defined as

$$t_{NW} = \frac{d_{tip} - d_{base}}{L_{NW}}, \tag{2.14}$$

where d_{tip} and d_{base} are the diameters of the nanowire at the tip and base respectively, and L_{NW} is the nanowire length [57]. For a given growth temperature and vapor pressures, the volume of the Ga droplet evolves towards a stable value and then remains constant as the nanowire grows [87, 90]. Consequently, the nanowire diameter also converges towards a steady-state value [87, 90]. Recently, the existence of two stable droplet configurations (i.e. contact angles θ) at the nanowire tip has been demonstrated [91]. For $\theta \approx 130°$, the nanowire diameter increases continuously during growth, while it remains constant for $\theta \approx 90°$ [91]. However, due to the self-equilibration of the droplet size, nanowire ensembles with very uniform diameters can be realized even if they are grown from droplets with different initial diameters [90]. Finally, nanowire tapering may not only result from the evolution of the droplet size, but also from direct, non-uniform VS growth on the nanowire sidewalls [92].

2.4 Length Distribution in VLS-grown III-V Nanowire Ensembles

III-V nanowire ensembles with identical dimensions and narrow size distributions are highly desired for the fabrication of III-V nanowire-based (opto)electronic devices in order to ensure a stable device performance and uniform device properties. In particular, theoretical predictions by Glas and Dubrovskii from 2017 reveal that the length distribution (LD) of VLS-grown III-V nanowire ensembles can be narrower than Poissonian, i.e. sub-Poissonian [93, 94]. A sub-Poissonian distribution is attributed to the presence of a physical effect denoted as nucleation antibunching [84, 93, 94, 95, 96], which leads to self-narrowing of LDs in VLS-grown III-V nanowire ensembles [93, 94, 96].

In practice, the LD of self-catalyzed GaAs nanowires grown on native-SiO_x/Si(111) substrates is much broader than theoretical predictions, and a narrow (sub-Poissonian) LD is challenging to achieve, since various effects may be in place, which initiate broadening of the nanowire LD. That is, (i) asymmetric broadening due to delayed nucleation of the nanowires on their substrate as commonly observed [97], which involves the formation of Ga droplets, the interaction of Ga with SiO_x, the formation of nano-sized SiO_x openings, and finally the droplet-assisted nucleation of GaAs nanowire inside those openings, (ii) asymmetric broadening due to continuing nucleation of catalyst droplets, and thus nanowires, on the substrate in the self-catalyzed growth mode [98], (iii) symmetric broadening due to kinetic fluctuations during nanowire growth [99, 100], and (iv) symmetric broadening due to the diffusion-induced character of growth [101]. All these effects inherently restrict the LD of VLS-grown III-V nanowire ensembles in the best case to a Poissonian shape [98, 101], but even a narrowing of the nanowire LD towards a Poissonian shape is far from trivial.

In the following section, narrowing of the LD due to nucleation antibunching is outlined for self-catalyzed growth of GaAs nanowire ensembles, although first theoretical considerations refer to Au-catalyzed growth of individual $\mathrm{InP}_{1-x}\mathrm{As}_x$ and GaAs nanowires as reported by Glas *et al.* in 2010 [84, 95] and Dubrovskii *et al.* in 2013 [100].

2.4.1 Nucleation Antibunching

Nucleation antibunching is specific to nano-sized catalyst droplets, like Ga droplets in the self-catalyzed growth of GaAs nanowires. Figure 2.14 illustrates the effect of nucleation antibunching in self-catalyzed GaAs nanowire ensembles. GaAs nanowire ensembles are depicted schematically subsequent to filling of the Ga droplets with As in Fig. 2.14 (a), and subsequent to formation of one monolayer of GaAs (bilayers of single atoms of Ga and As), where the droplets are depleted of As, in Fig. 2.14 (b). Figure 2.14 (c) shows the time evolution of the $\mathrm{As}_{4/2}$ concentration c_{As} (dashed curves) and the nucleation probability density P_N (number of nucleation events per time interval and number density of Ga droplets, green curves), while the red curve represents the number of nucleation events (or oscillations of $\Delta\mu$ respectively). The gray areas mark the time interval within each monolayer growth cycle, in which the nucleation event is most likely.

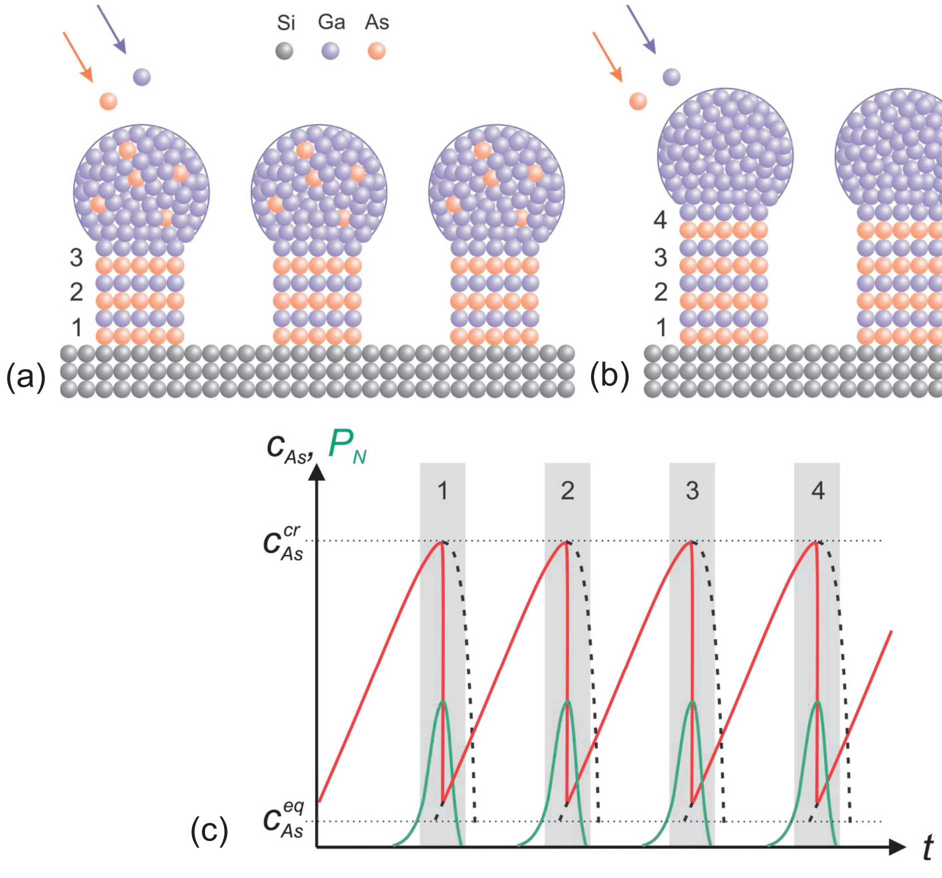

Fig. 2.14: Schematic illustration of temporally anti-correlated nucleation events in self-catalyzed GaAs nanowire ensembles on Si substrates. (a), (b) Ensemble growth of GaAs nanowires in a layer-by-layer fashion (a) after filling the Ga droplets with As, and (b) formation of a monolayer of GaAs instantaneous with depletion of the Ga droplets in As. (c) Plot of the temporal evolution of the As concentration c_{As} (dashed curve), nucleation probability P_N (green curve), and the particular realization of nucleation events (red curve). Fig. 2.14 (c) is adapted from [100].

In the particular stage of nanowire growth depicted in Fig. 2.14 (a), three monolayers of GaAs already nucleated on the substrate below the Ga droplet in every single nanowire, which is equivalent to the first three nucleation events in Fig. 2.14 (c). In order to nucleate a fourth monolayer, the Ga droplets have to be re-filled with $As_{4/2}$ up to a critical c_{As}^{cr} as depicted by in Figs. 2.14 (a) and (c). When the droplets are supersaturated with $As_{4/2}$ (and $\Delta\mu$ has increased), P_N simultaneously increases to a maximum, at which the nucleation event finally takes place. If there is enough $As_{4/2}$ inside the Ga droplets (i.e. equal or more compared to what is needed to form a single monolayer across the liquid/solid interface area), the formation of one complete monolayer of GaAs occurs at the droplet/nanowire interface instantaneously with the abrupt depletion of the droplet in $As_{4/2}$ (drop of c_{As}, and thus $\Delta\mu$) as illustrated in Figs. 2.14 (b) and (c). Simultaneously, P_N decreases immediately after the nucleation event (see Fig. 2.14 (c)), which means that the formation of another monolayer of GaAs right after the previous nucleation event is impossible. Droplet refilling, monolayer formation and droplet depletion are sequentially repeated. In the mononuclear regime, it is assumed that the formation of the monolayer occurs in a very short time compared to the mean time between nucleation events (given by the time for refilling the Ga droplets with $As_{4/2}$) [76]. Since the nucleation of a new monolayer of GaAs is not possible at all before refilling the droplets with $As_{4/2}$, the nucleation events depend on each other, i.e. they are anti-correlated in time. Thus, nucleation antibunching is the temporal anti-correlation of consecutive nucleation events as depicted by the red curve in Fig. 2.14 (c). Nucleation antibunching induces a self-regulation of the nanowire length and thus, leads to a narrow nanowire LD. This LD can be described by sub-Poissonian statistics, but it can be observed experimentally only when broadening effects are absent or successfully suppressed.

Nucleation antibunching emerges only (i) if one growth constituent has a low solubility in the liquid, i.e. group-V species such as As and P, because P_N is much more affected by group-V rather than group-III species, (ii) at low GR_{ax} to ensure a low rate of refill with $As_{4/2}$, and (iii) for thin nanowires (diameter smaller than ~50 nm), where P_N of two consecutive nucleation events do not overlap as shown in Fig. 2.14 [84, 100, 102]. In the opposite case, i.e. when P_N of two consecutive nucleation events overlap (e.g. in thicker nanowires, where “macroscopic” droplets assist growth), P_N does not start from zero, and the time for refilling the Ga droplets with $As_{4/2}$ is shorter (refill is faster). As a result, the nucleation events become random and independent of each other due to absence of nucleation antibunching, which leads to a Poissonian rather than a sub-Poissonian LD [100]. If there is not enough $As_{4/2}$ inside the droplets to form a complete monolayer of GaAs, growth of the 2D nucleus stops due to droplet depletion and new $As_{4/2}$ has to be transferred from the vapor to the droplet/nanowire interface, where completion of the monolayer occurs at the rate of refill from the vapor. The so-called “stopping effect” weakens nucleation antibunching and thus, the achievement of sub-Poissonian LDs in III-V nanowire ensembles [102].

2.4.2 Sub-Poissonian Length Distribution

Classical nucleation theory, which is beyond the scope of this dissertation, is used for modeling of nanowire growth and nanowire LD based on nucleation probabilities. Due to the stochastic nature of VLS growth of III-V nanowires, it is assumed that only discrete nucleation events take place at the droplet/nanowire interface, i.e. nucleation of one complete monolayer in the mononuclear regime or no nucleation event [84]. Therefore, the probability distribution of nucleation events, and thus monolayers along the nanowire axis, must follow a Poissonian statistic. For the description of the temporal evolution of LDs in III-V nanowire ensembles, an analytical approach based on a continuum-growth theoretical model has been developed by Glas and Dubrovskii in 2017 [93]. In the model, the nanowire length is analytically treated as the sum of an integer number of monolayers of a constant height along the growth direction. Moreover, it is assumed that Ga droplets of a certain number density have already nucleated on the substrate, and rest there until nanowire growth is initiated by supply of As. The kinetic processes during droplet formation on the substrate surface are not taken into account in the model. In the ideal case, when all nanowires nucleate at the same time from Ga droplets resting on the substrate (i.e. without nucleation delay), the nanowire LD denoted as $F(s, \tau)$ can be described by a Poissonian Green's function

$$F(s, \tau) = \frac{1}{\sqrt{2\pi\tau}} exp[-\frac{(s-\tau)^2}{2\tau}] \tag{2.15}$$

with $\langle s \rangle = \tau$ and $\sigma_P^2 = \tau$ [93]. $s = L_{NW}/h_{GaAs}$ is the nanowire length (measured in MLs), L_{NW} the nanowire length in nm, h_{GaAs}=0.326 nm the height of one ML of GaAs, τ the mean nanowire length, and σ_P^2 the variance (width) of a Poissonian LD. In reality, asymmetric broadening of the nanowire LD due to nucleation delay has to be considered in modeling of nanowire LDs. Nucleation delay is described by the parameter α, which expresses the ratio of the nucleation probability of the first monolayer of the nanowires to that of the upper monolayers [93]

$$\alpha = \frac{p_0}{GR_{ax}} = \frac{1}{\Delta t \cdot GR_{ax}} = \frac{1}{\Delta t} \cdot \frac{t_{gr}}{\tau}. \tag{2.16}$$

p_0 is the nucleation probability of the first monolayer (number of nucleation events per time interval Δt), Δt the time needed on average to form the first nanowire monolayer from the droplets that rest on the substrate (nucleation delay time, reciprocal value of the nucleation probability p_0), GR_{ax} the average axial growth rate in ML/s, and t_{gr} the growth duration. For $\alpha = 1$, the first monolayer nucleates with identical probability compared to the upper monolayers. For $\alpha \ll 1$, nucleation of the first monolayer from a droplet takes longer compared to the upper monolayers, leading to a broadening of the nanowire LD and a pronounced asymmetry towards shorter nanowire lengths. In presence of nucleation delay ($\alpha \ll 1$), the nanowire LD is obtained by convolution of Green's function $F(s, \tau)$ and the nucleation rate $j(\tau)$. $j(\tau)$ is the product of the nucleation probability of the very first monolayer and the number density of Ga droplets, and is given by [93]

$$j(\tau) = \alpha e^{-\alpha\tau}. \tag{2.17}$$

The slope of the exponentially decreasing function is characterized by α. Convolution of Eq. 2.15 and Eq. 2.17 gives the function of the Poissonian LD denoted as $f(s,\tau)$ for $\alpha \ll 1$ [93]

$$f(s,\tau) = \frac{\alpha}{2} e^{\alpha(s-\tau)+\alpha^2\frac{\tau}{2}} erfc[\frac{s-\tau+\alpha\tau}{\sqrt{2\tau}}]. \tag{2.18}$$

$erfc(x)$ denotes the complementary error function [93]. The nanowire LD depends on s and τ. The time evolution of $f(s,\tau)$ in presence of nucleation delay and absence of nucleation antibunching is shown for various τ as dashed lines in Fig. 2.15. As seen, $f(s,\tau)$ is asymmetrically broadened and σ_P^2 scales with τ. However, the situation is different in presence of both nucleation delay and nucleation antibunching ($\alpha \ll 1$, $\epsilon \ll 1$). The nanowire LD can be simply obtained by replacing the time-dependent variance $\sigma_P^2{=}\tau$ with the time-independent variance $\sigma_{sub-P}^2{=}1/(2\epsilon)$ in Eq. 2.18. The resulting function gives a sub-Poissonian LD [93]

$$f(s-\tau) = \frac{\alpha}{2} e^{\alpha(s-\tau)+\frac{\alpha^2}{4\epsilon}} erfc[\sqrt{\epsilon}(s-\tau) + \frac{\alpha}{2\sqrt{\epsilon}}]. \tag{2.19}$$

Equation 2.19 only depends on the difference $s-\tau$. The time evolution of a sub-Poissonian LD with temporally anti-correlated nucleation events is shown for various τ as solid lines in Fig. 2.15.

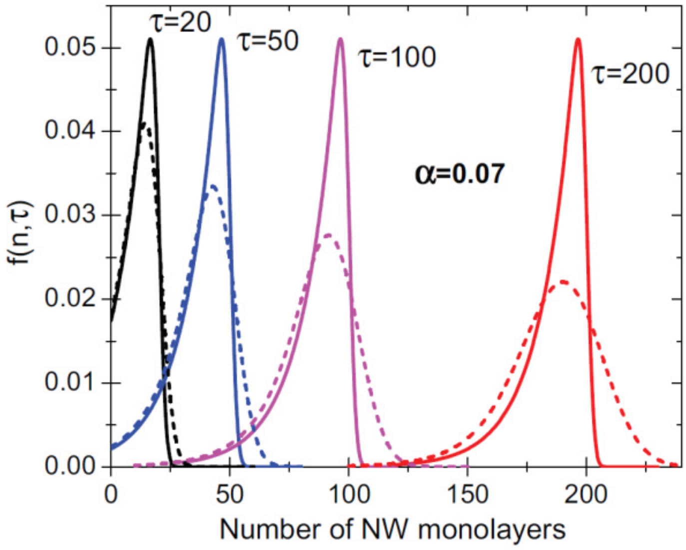

Fig. 2.15: Comparison between the time evolution of the nanowire length distributions with nucleation-induced broadening in the presence (solid lines, $\epsilon = 0.1$) and absence (dotted lines, $\epsilon = 0$) of nucleation antibunching, for the same $\alpha = 0.07$. Reprinted figure with permission from [93]. Copyright (2017) by the American Physical Society. Note that the parameter n in the plot equals s in the main text.

As seen, the variance of the sub-Poissonian LD ($\sigma^2_{sub-P} = 1/(2\epsilon)$) is independent of τ rather than growing infinitely as in the Poissonian case. For all τ, σ^2_{sub-P} is smaller than σ^2_P. Summarizing, it should be possible to grow long III-V nanowires with very narrow (sub-Poissonian) LD if all nucleation events of the nanowires on their substrate are synchronized as assumed in this model. Only one experimental demonstration of a sub-Poissonian LD of self-catalyzed GaAs nanowire ensembles on Si(111) substrates has been reported so far [103].

2.5 Crystal Structure of VLS-Grown III-V Nanowires

The fabrication of III-V nanowire-based (opto)electronic devices requires growth of III-V nanowires with high structural purity and crystal perfection in order to provide a high device performance and long-term reliability. In reality, a typical problem in III-V nanowires is the co-existence of different crystal phases as well as the presence of planar defects. For a better understanding of the structural composition of III-V nanowires, the aforementioned crystal phases and defects are described in this section.

2.5.1 Structural Polytypism and Stacking Faults

While GaAs epilayers crystallize in the cubic zinc blende (ZB) phase, GaAs nanowires can adopt the cubic ZB or hexagonal wurtzite (WZ) phase. In case of VLS-grown GaAs nanowires, the crystal structure depends on the catalyst. While Au-catalyzed GaAs nanowires exhibit mainly the WZ phase as the dominant crystal structure [104, 105, 106], crystallization in the ZB phase is mainly favored in self-catalyzed GaAs nanowires [69, 107, 108, 109]. However, alternations between ZB and WZ phase along the nanowire axis are commonly observed in III-V nanowires. This is denoted as structural polytypism [85, 110, 111]. At this point, it is important to outline the differences in the bonding configuration of the two crystal phases.

Figure 2.16 shows the stacking sequence of atomic planes for the two crystal phases along the $\langle 111 \rangle$ growth direction. As illustrated in Fig. 2.16 (a), the ZB phase exhibits a stacking sequence of ABCABC, whereas the WZ phase illustrated in Fig. 2.16 (b) possesses a stacking sequence of ABABAB. Each plane A, B and C consists of a bilayer of vertically stacked Ga and As atoms that corresponds to one monolayer of GaAs. HRTEM images of the ZB and WZ phase are depicted in Figs. 2.16 (c) and (d), respectively, for comparison. In the HRTEM images, Ga and As atoms within one plane (depicted by the dashed oval in the close-ups of Figs. 2.16 (a) and(b)) cannot be resolved, and emerge as individual dots. Comparing the bonding configuration of ZB and WZ GaAs in the close-ups of Figs. 2.16 (a) and (b) reveals a shorter bond length in the $\langle 11\bar{2} \rangle$ direction for WZ GaAs compared to ZB GaAs if third nearest neighbor atoms are considered. A shorter bond length in WZ GaAs results in a slightly larger formation energy for the WZ phase (by 25 meV per octet pair [110]) compared to the ZB phase. This small difference in the internal formation energy may affect the stacking sequence of Ga and As atoms along the growth direction, which finally results in a complete change of the crystal structure from ZB to WZ GaAs or from WZ to ZB GaAs.

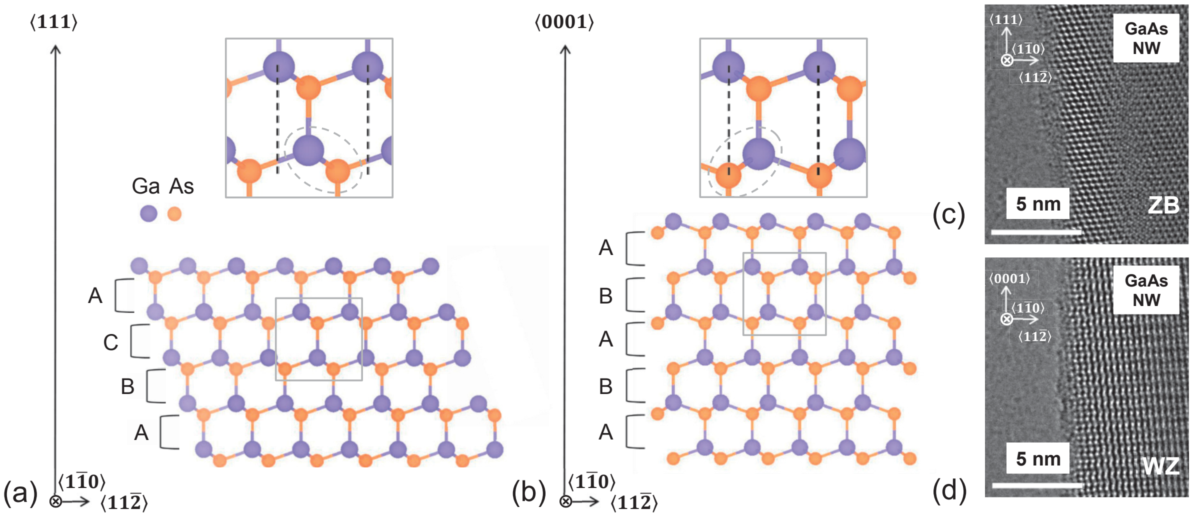

Fig. 2.16: Stacking sequence of Ga and As atoms in (a) the ZB and (b) the WZ crystal phase in the ⟨1$\bar{1}$0⟩ viewing direction. The insets in (a) and (b) show close-up views of the bonding configuration in the ZB and WZ crystal phase respectively. For visualization of the two crystal phases in III-V nanowires, the software *VESTA* was used [35]. Side-view HRTEM images of (c) pure ZB and (d) pure WZ crystal phase in GaAs nanowires in the ⟨1$\bar{1}$0⟩ viewing direction. Figs. 2.16 (a) and (b) are adapted from [85].

Another type of disruption in the regular stacking of atoms along the growth direction that is often observed is the rotational twinning [110]. In particular, the ZB structure is rotated around the ⟨111⟩ growth axis by 60° as shown schematically in Fig. 2.17 (a). This type of stacking fault (SF) changes the original stacking sequence from ABCABC into CBACBA. The crystal plane that separates the two twinned segments is called twin plane (TP). For comparison, a HRTEM image of a twinned ZB GaAs nanowire segment is shown in Fig. 2.17 (b).

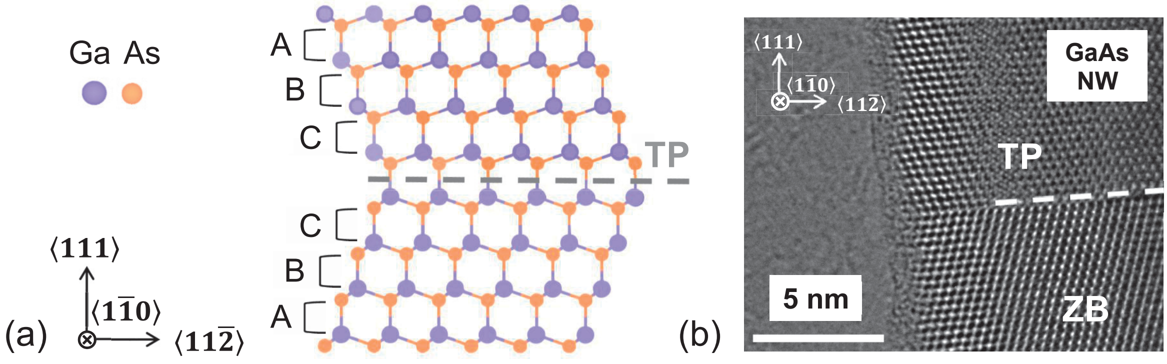

Fig. 2.17: Rotational twinning in ZB GaAs nanowires. (a) Bonding configuration of two twins of the ZB phase with different orientation after rotation of one twin by 60° around the ⟨111⟩ growth axis. For visualization of the twinned ZB structure, the software *VESTA* was used [35]. (b) Side-view HRTEM image of a twinned ZB crystal segment in the ⟨1$\bar{1}$0⟩ direction of a GaAs nanowire. The twin planes are indicated by dashed lines. Fig. 2.17 (a) is adapted from [85].

Polytypes and SFs in III-V nanowires have a crucial impact on their optical properties. In various studies, different band gap energies and band offsets have been demonstrated for polytypic

WZ/ZB GaAs nanowires compared to mainly WZ or ZB GaAs nanowires [112, 113, 114, 115, 116, 117]. For polytypic WZ/ZB GaAs nanowires, numerous radiative recombination paths of photogenerated excitons have been proposed due to a wide range of photoluminescence transition energies (i.e. 1.45-1.55 eV) [116, 118]. Besides planar crystallographic defects, it has been revealed that native point defects such as As vacancies and Ga antisites significantly affect photoluminescence emission in ZB GaAs nanowires [119]. Additionally, planar defects such as SFs and TPs not only break the crystal symmetry, but also act as scattering centers for electrons and holes during 1D transport, which also degrades the electronic properties of III-V nanowires. For instance, an increase in the electrical resistance (up to two orders of magnitude) in polytypic WZ/ZB InAs nanowires compared to single-phase nanowires has been reported [120]. For WZ-free ZB GaAs nanowires, an increase in the electrical resistance and a decrease of the carrier mobility with increasing number of TPs along the nanowire axis have been demonstrated [121]. Therefore, it is clear that all types of crystallographic defects (structural polytypes, planar and point defects) dramatically restrict the efficiency and stability of III-V nanowire-based (opto)electronic devices.

2.5.2 Influencing Parameters and Growth Conditions

The VLS growth of high quality III-V nanowires free of polytypes and SFs is non-trivial and rather complicated since the evolution of the crystal structure during growth is related to various parameters: supersaturation [86, 110, 122], droplet geometry [123, 124], morphology of the droplet/nanowire interface and truncation edge [125, 126, 127, 128], surface and interface energies [110, 127, 129, 130], nanowire diameter [86, 110, 124, 131, 132, 91], and dopants [133, 134]. First, the crystal structure of Au-catalyzed III-V nanowires and its influencing parameters was studied. Glas and Dubrovskii discussed the formation of the predominant WZ phase in Au-catalyzed nanowires on the basis of classical nucleation theory [86, 122]. It has been revealed that the formation of the WZ phase is favored at the VLS triple-phase-line (TPL), where the nucleation energy barrier for WZ formation is smaller compared to ZB, and under high supersaturation of group-V atoms in the liquid [86, 122]. In contrast, nucleation in the ZB phase occurs preferentially away from the TPL (i.e. at the liquid-solid interface), and under a low supersaturation [86, 122]. Moreover, it has been shown that the size of the catalyst droplets, i.e. the droplet contact angle θ, and the morphology of the growth interface determine the type of crystal phase, in which a new monolayer of material nucleates at the droplet/nanowire interface [123, 127, 128]. The role of the interface morphology in the crystal structure is strongly connected with surface energies of the GaAs nucleus at the vapor-liquid and liquid-solid interface [127, 129, 130]. Krogstrup *et al.* found that nucleation in the WZ phase is favored, when the catalyst droplets possess contact angles of $\theta \approx 90°$, and a critical contact angle, at which the phase transition from WZ to ZB occurs, was suggested [123]. Using *in situ* transmission electron microscopy (TEM), Jacobsson *et al.* related the droplet contact angle to the morphology of the droplet/nanowire interface and showed that nucleation in the WZ phase is preferred for planar top facets ($\theta \approx 90°$), while nucleation is favored in the ZB phase in presence of additional truncated edge facets ($\theta > 90°$) [128]. Based on a surface energy theoretical model, Dubrovskii *et al.* confirmed that contact angles θ between 110 and 130° lead to a planar growth interface and thus, predominant WZ phase, whereas $\theta > 130°$ result in truncated interfaces, and pure ZB phase [130]. A complemented insight was given recently by Harmand *et al.* [83]. Using *in situ* TEM, it is experimentally shown that the nucleation of the WZ monolayer occurs at the TPL, which is attributed to a lower surface energy of a WZ GaAs nucleus at the TPL compared to that of the ZB nucleus at the liquid/solid interface [83]. This surface energy is directly related to the droplet contact angle and a critical contact angle of $\theta \approx 121°$ for the WZ-ZB transition was reported [83].

Although these studies untangle the role of various parameters on the crystal structure of Au-catalyzed GaAs nanowires, the situation can be dissimilar for self-catalyzed GaAs nanowires due to different growth conditions and catalyst composition. Only a few studies have been published so far that focus on the investigation of the crystal structure of self-catalyzed GaAs nanowires. The predominant ZB phase in self-catalyzed GaAs nanowires is attributed to a much lower surface energy of liquid Ga compared to Au-Ga alloys that suppresses the nucleation at the TPL [69]. Rieger *et al.* reported that nucleation in the ZB phase is most likely at contact angles of $\theta \approx 90°$, WZ becomes dominant for $\theta > 90°$, and twinned ZB is formed for even larger contact angles, i.e. $\theta = 137°$ [124]. In a recent study by Kim *et al.*, the existence of two stable contact angles θ of approximately 90° (with a planar top facet) and 130° (with a truncated top facet) was demonstrated that result in the WZ and ZB phase, respectively [91]. We also have some indications of a truncated edge facet at the nanowire/droplet interface for $\theta > 130°$. This implies a similar situation as compared to the Au-catalyzed growth mode. It was further shown that the nanowire diameter could also have an effect on the selection of the crystal phase in self-catalyzed GaAs nanowires [91, 124].

Summarizing, control of the crystal structure in VLS-grown III-V nanowires requires control of the droplet/nanowire interface morphology and interface energies through the contact angle of the liquid phase. This can be achieved to some extent by tuning of the basic growth parameters, for instance the growth temperature T_{gr} and the V/III ratio (i.e. the Ga and As beam fluxes – F_{Ga} and F_{As}) as has been demonstrated in numerous growth studies for Au-catalyzed as well as self-catalyzed GaAs nanowires [69, 86, 110, 123, 124, 127, 131, 135, 136, 137, 138, 139, 140]. Moreover, it has been shown that simultaneous interruptions of all beam fluxes and sequential shutter switching procedures for beam flux pulsing are very promising in order to reduce the number of SFs and to control the crystal structure in Au-catalyzed III-V nanowires [141, 142, 143].

Besides the structural control for high phase purity of III-V nanowires, which is required for high mobility or 1D ballistic transport applications, the deliberate selection of the crystal phase during nanowire growth is also of great interest. Crystal phase selection would allow the controlled fabrication of crystal heterostructures, and thus band gap engineering based on WZ/ZB polytypes. Such WZ/ZB superlattices are obtained (i) by inserting thin WZ segments in a ZB nanowire, which leads to the formation of mini-bands for electrons and holes, or (ii) by placing thin ZB sections between thicker WZ units, which form quantum dots along nanowires of thin enough diameter when a type-II band alignment between WZ and ZB is assumed [110, 112]. Moreover, it has been shown that periodic insertions of TPs in pure ZB nanowires create mini-bands for electrons and holes [144, 145].

2.5.3 Structural Composition of Self-Catalyzed GaAs Nanowires

Despite a decent level of structural control, self-catalyzed GaAs nanowires still exhibit a low to moderate number of polytypic WZ/ZB sections as well as SFs and TPs as shown in Fig. 2.18.

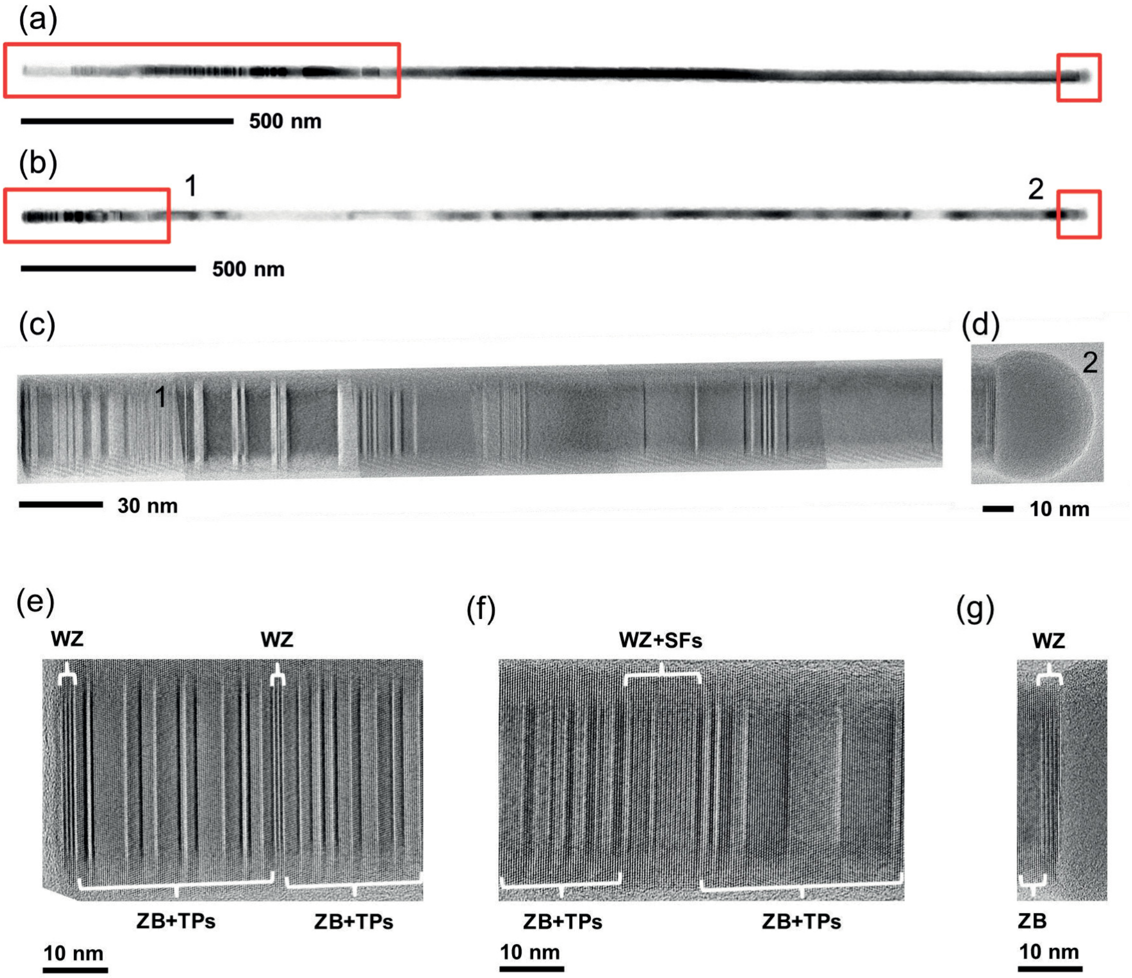

Fig. 2.18: Crystal structure of GaAs nanowires grown in self-catalyzed VLS mode. (a), (b) Overview side-view TEM images of two representative GaAs nanowires with highly defective crystal segments at the base and tip of the nanowires as marked in red color, and denoted as segment 1 and 2 in (b). (c), (d) Close-up TEM images of region 1 and 2 of the nanowire in (b). (e), (f) and (g) Representative HRTEM images taken from defective base and tip segments of the nanowires, which illustrate the co-existence of WZ/ZB polytypes in one individual nanowire as well as SFs and TPs.

Overview TEM images of two representative GaAs nanowires in Figs. 2.18 (a) and (b) reveal relatively long defective crystal segments at the nanowire base with dimensions in the range of ∼400 to 800 nm. Additionally, defective segments with lengths of several tens of nanometers at the nanowire tips are commonly observed. The corresponding segments are highlighted in red color in Figs. 2.18 (a) and (b). Each SF corresponds to a sharp contrast reversal along the nanowire axis. Only the middle segments of the nanowires are pure ZB with occasional TPs. The gradual contrast modulations in the middle segment of the nanowire in Fig. 2.18 (b) are associated with bending contours rather than SFs. Figures 2.18 (c) and (d) illustrate close-up views of the defective crystal segments at the base and at the tip of the nanowire shown in Fig. 2.18 (b). As shown in Fig. 2.18 (c), clearly a high number density of SFs is present at the base segment, which decreases along the growth direction. HRTEM images of selected regions of the defective base segment are shown in Figs. 2.18 (e) and (f). TEM analysis revealed the coexistence of WZ and ZB phases and the presence of SFs, i.e. TPs, perpendicular to the nanowire axis. The high number density of SFs at the nanowire base and its continuous decrease along the axis of the base segment is attributed to a local transient in the size and contact angle of the Ga droplets during growth initiation. After having reached a stable droplet size and contact angle, the growth of GaAs nanowires proceeds without formation of SFs, which is demonstrated by the defect-free middle segments of the nanowires in Figs. 2.18 (a) and (b). The defective segments at the nanowire tips below the Ga droplets exhibit a very short length of ∼10 nm as shown in Fig. 2.18 (d), together with its HRTEM image in Fig. 2.18 (g). Their origin is again attributed to a local transient in the size and contact angle of the Ga droplets during growth termination. They both decrease gradually after the growth termination due to partial consumption of the droplets under the residual As in the growth chamber. Despite simultaneous interruption of the Ga and As beam fluxes, the shut-off transient of the As flux is longer compared to the Ga flux due to slow pumping of the As out of the growth chamber. As a result, axial growth is prolonged unintentionally during droplet consumption, which leads to the formation of SFs or extended WZ sections in the otherwise ZB nanowires. Such structural composition is commonly observed in self-catalyzed GaAs nanowires [69, 109, 111, 124, 146], and implies that reproducible growth of phase-pure and defect-free GaAs nanowires is highly demanding.

2.6 III-V Nanowire Heterostructures

Heterostructures are essential elements for the development of complex functional (opto)electronic devices. III-V nanowire heterostructures can be realized by changing the composition either along or perpendicular to the nanowire axis. Radial nanowire heterostructures, better known as core-(multi-)shell nanowires, are produced by compositional modulations perpendicular to the nanowire axis as schematically depicted in Fig. 2.19 (a). Depending on the selection of the shell material, multiple radial quantum wells can be created, which is for instance the basis for GaAs/$Al_xGa_{1-x}As$ quantum well nanowire lasers [147, 148]. But also the more challenging axial nanowire heterostructures produced by material variation along the nanowire axis as shown in Fig. 2.19 (b) play an essential role in the development of III-V nanowire-based (opto)electronic devices. For instance, quantum dot-in-a-wire structures used as single photon sources and LEDs have been demonstrated [12, 149, 150, 151, 152], and moreover photonic crystal lasers [153], resonant tunneling diodes [154], and single electron transistors [155, 156, 157]. More complex nanowire heterostructures may contain both compositional modulations along and perpendicular to the nanowire axis.

While axial VLS (or VS) growth of pure binary III-V nanowires is fairly well-controlled, synthesis of III-V nanowire heterostructures is more challenging. Growth of radial nanowire heterostructures includes first axial VLS (or VS) growth of binary core nanowires, and second, lateral VS growth of (multiple) shells. In case of self-catalyzed VLS growth of the core nanowires, the liquid droplets have to be consumed under group-V beam flux prior to shell growth. In contrast, VLS growth of axial nanowire heterostructures is not as trivial as synthesis of radial nanowire heterostructures, since all growth species have to find their pathway into the crystal lattice through the liquid droplets. In particular, most applications of axial nanowire heterostructures require atomically sharp interfaces between different III-V materials along the nanowire axis. Pre-requisite for synthesis of nanowire heterostructures with abrupt axial interfaces is a precise level of compositional control along the nanowire axis in order to avoid unintended interface broadening.

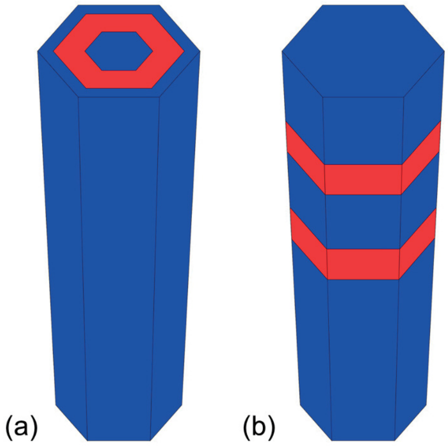

Fig. 2.19: Schematic illustration of (a) radial and (b) axial III-V nanowire heterostructures.

In practice, compositional grading is commonly observed in axial nanowire heterostructures [158, 159, 160], where the width of the transition region between different III-V materials can vary from a few monolayers to several tens of nanometers, and depends on the type of employed growth species. The reason for interface grading, and thus lack of compositional control, is attributed to different solubilities of growth species in the droplet. MBE growth of axial nanowire heterostructures involves at least three beam fluxes of group-III and group-V species. While group-III metals (i.e. Al, Ga, In) exhibit a high solubility in the droplets, group-V species (i.e. As, P) possess a low solubility in the liquid particle (e.g. ~1 at% [76, 82]). In particular, the high solubility of group-III atoms in the droplets leads to accumulation of these species in the liquid phase. Consequently, excess material is removed from the droplet by unwanted incorporation in the crystal lattice during growth of the consecutive nanowire section with different composition even if the beam flux of the previous growth species is switched off instantaneously. Thus, it is more difficult to produce sharp interfaces in III-III-V axial nanowire heterostructures compared to III-V-V axial nanowire heterostructures, where abrupt heterointerfaces have been reported [111, 161, 162]. The phenomena of accumulation of growth species in the liquid phase is known as the reservoir effect [163, 164, 165].

Several growth techniques and strategies have been proposed to suppress the reservoir effect, and to attain sharper axial heterointerfaces, such as the use of solid catalyst particles [166], pulsing of the group-III vapor phase to purge the droplets [163], beam flux interruptions [162, 167], pre-filling of droplets with group-III atoms [167], and slow growth rates in combination with high re-evaporation rates of stored atoms from the droplets (i.e. for P) [162, 168]. In addition to the reservoir effect, further phenomena may be present that prevent the growth of abrupt axial heterojunctions, such as atom interdiffusion [160, 169], and surface segregation [4, 170], which are dominant at high growth temperatures. The interface sharpness in axial nanowire heterostructures furthermore depends on the nanowire diameter [163, 164].

To date, only a few growth studies on Au-catalyzed axial nanowire heterostructures have been reported, for instance, heterostructures based on the material systems GaAs/InAs [158, 163, 171, 172, 173], GaAs/$Al_xGa_{1-x}As$ [174, 175, 176, 177, 178], GaAs/$In_xGa_{1-x}As$ [159], InAs/$In_xGa_{1-x}As$ [160], InP/$InAs_xP_{1-x}$ [161], and InN/$In_xGa_{1-x}N$ [179]. Moreover, growth reports on self-catalyzed axial nanowire heterostructures are even rare, and only a small number was found. These heterostructures, for example, are composed of GaAs/InAs [180], GaAs/$Al_xGa_{1-x}As$ [167], GaAs/$In_xGa_{1-x}As$ [181, 182], GaAs/$GaAs_xSb_{1-x}$ [183], GaAs/$GaAs_xP_{1-x}$ [162] and InSb/InP [184].

3 Growth Technique and Characterization Methods

The main principles of the molecular beam epitaxy, which was employed for the growth of GaAs-based nanowires, as well as the growth system at the Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf are presented in this chapter. Furthermore, an overview of the applied *in situ* and *ex situ* techniques for the characterization of the nanowires is given in the second part.

3.1 Molecular Beam Epitaxy (MBE)

In the present dissertation, MBE is employed as the growth technique for GaAs-based nanowires and Ga droplet samples. MBE has been invented by *J. R. Arthur* and *A. Y. Cho* in the late 1960s. It has been widely established as one of the most important techniques for single crystal growth of various semiconductor materials, such as III-V [185, 186, 187], II-VI [188, 189, 190], and IV-VI [191, 192] compounds. In the following years, extensive development efforts of the MBE technique have not only paved the way towards its introduction to the industry, but also gave rise to a detailed investigation and understanding of the physical mechanisms involved in the crystal growth of semiconductors. A first insight into the interaction of Ga atoms and As_2 molecules with the surface of a GaAs substrate has been provided by *J. R. Arthur* in 1968 [193]. Three years later, epitaxial growth of GaAs thin films with fairly good structural quality on GaAs substrates was reported [194].

3.1.1 General Aspects of MBE

Molecular beam epitaxy is a physical vapor phase deposition method. It produces epitaxial thin films and low-dimensional nanostructures by interaction of neutral atoms and molecules of various source materials, that impinge on a heated crystalline substrate surface in a vacuum environment. The growth species are transported from thermal effusion cells to the substrate via atomic and molecular beams. Epitaxial growth of semiconductor crystals requires ultra high vacuum (UHV) conditions typically in the range of 10^{-8} to 10^{-9} Pa [36] in order to avoid (i) contamination of the substrate surface, (ii) incorporation of impurities from the vacuum ambient into the growing crystal, and (iii) collision of atoms and molecules of the beam with residual gas molecules. Compared to chemical growth techniques, such as MOCVD, no carrier gas flow is needed, which further reduces the risk for contamination.

Crystal growth is commonly performed at pressures in the range of 10^{-7} to 10^{-2} Pa depending on the vapor pressure of the source elements. A low operating pressure P results in a collision-free transport of the atoms and molecules within the beam to the substrate surface due to a large mean free path λ_p that is expressed by

$$\lambda_p = \frac{k_B \cdot T}{P\pi{\sigma_m}^2}, \tag{3.1}$$

where σ_m is the molecule diameter, k_B the Boltzmann constant, and T the temperature [77]. If a molecule of a diameter σ_m of 1 nm at a pressure P of 10^{-5} Pa and a temperature T of 300 K is considered (typical conditions for growth of GaAs), λ_p is in the order of several tens of meters. Depending on the initial state of the source materials at room temperature (i.e. vapor, liquid or solid phase), multiple process variants are established. Elements originating from purely gaseous precursor sources are employed in chemical beam epitaxy. Gas-source MBE uses hydride gas sources and solid sources, while metal-organic MBE uses metal-organic gas sources and solid sources. In solid-source MBE, all source materials exist as ultra-pure solid elements at room temperature. Solid-source MBE is exclusively employed within this dissertation.

In solid-source MBE, the growth species are produced by thermal evaporation (e.g. Al, Ga, In) or sublimation (e.g. As, Si, Be) of the pure elemental source materials. Thermal effusion cells are typically employed for solid (and liquid) source materials. Their source crucibles, that are typically made of pyrolitic boron nitride (in our MBE), quartz or graphite, contain the source material. The crucibles are heated by tantalum filament coils, and are simultaneously cooled by a water-cooling (e.g. the As cell in our MBE) to prevent heat transfer. The temperatures of the effusion cells are controlled via thermocouples that are in direct contact with the source crucible. Owing to the large orifice, real effusion cells are operated in thermodynamic non-equilibrium. Closed effusion cells with a tiny orifice, so-called Knudsen cells, can be used as an approximation of a real cell. At a certain cell temperature T_c, their source material is in thermodynamic equilibrium with its vapor. The corresponding equilibrium pressure P_{eq} is expressed by the Clausius-Clapeyron formula

$$P_{eq} = P_0 \cdot exp(-\frac{\Delta H}{k_B}(\frac{1}{T_c} - \frac{1}{T_0})), \tag{3.2}$$

where P_0 is the equilibrium pressure at a temperature T_0, ΔH the evaporation enthalpy, and k_B the Boltzmann constant [36]. The beam flux F produced by a Knudsen cell is proportional to P_{eq} and can be expressed by

$$F = \frac{P_{eq}}{\sqrt{2\pi k_B m T_c}}, \tag{3.3}$$

where m is the atomic or molecular mass of the source element [36]. The beam flux F_S, which impinge on the surface of a substrate, which is placed in a distance l in front of the effusion aperture of the Knudsen cell with an area A, is given by [36]

$$F_S = \frac{F \cdot A}{\pi l^2}. \tag{3.4}$$

Thus, F and F_S are defined as the number of particles that impinge on a substrate area per time interval ([flux]=atoms/(area×time)).

Besides the application of these conventional effusion cells, special effusion sources denoted as valved-cracker cells are often employed in modern MBE systems. This type of effusion cell is used for thermal evaporation of molecules, such as As_4 or P_4 tetramers, at low to moderate cell temperatures T_c in the range of 300 to 600 °C. Valved-cracker cells are moreover equipped with a heated cracking zone, which is located above the source crucible. Evaporated tetramers are thermally dissociated into dimers when they pass through the cracking zone at high temperatures (e.g. 800 to 1000 °C [36]). Only at high cracking temperatures, a pure dimer beam is created, whereas the beam may consist of both tetramers and dimers at lower cracking temperatures. As_2 and P_2 dimers can be beneficial in some cases of epitaxial growth of III-arsenides or III-phosphides because their sticking coefficient on the substrate in presence of group-III atoms is larger than that of tetramers [79]. Valved-cracker cells are additionally equipped with a motorized needle valve allowing for precise adjustment of the beam flux. Regardless of the type of effusion cell, all cells are mounted in an off-axis configuration with respect to the surface normal of the substrate in order to enable the accommodation of multiple effusion cells.

For the measurement and calibration of the beam fluxes, that are generated by the individual effusion cells, a flux ionization gauge is placed in front of the substrate manipulator. The beam flux F_S is determined by measuring the beam equivalent pressure (BEP) as a function of the cell temperature T_c, when only a single beam is switched on. For valved-cracker cells, the BEP can be also measured as a function of the valve position at fixed T_c. Modern MBE systems are furthermore equipped with multiple analytical tools that enable *in situ* and real-time analysis of crystal growth. In the following section, the MBE system for growth of III-V semiconductors at Helmholtz-Zentrum Dresden-Rossendorf is presented.

3.1.2 MBE System

The solid-source MBE system RIBER Compact 21T was used for the growth experiments (GaAs-based nanowire and Ga droplet samples) within this dissertation. The MBE system is a close-packed research machine equipped with multiple chambers in a modular design, in particular one growth chamber, one buffer chamber and one load lock chamber. The front-view of the MBE system is shown in Fig. 3.1 (a).

The load lock chamber is the interface of the MBE system with atmosphere. 3-inch Si(111) wafers are mounted onto special substrate platens, which are then loaded into a cassette with a capacity of six platens. Subsequently, the cassette is placed into the load lock chamber. The latter is pumped down by a scroll pump (rough pumping) in combination with a turbo-molecular pump (fine pumping). A base pressure in the order of 10^{-6} Pa is reached within a few hours in the load lock chamber. At such a low pressure, the cassette can be transferred through the opened gate valve into the buffer chamber using a vertical transport lift.

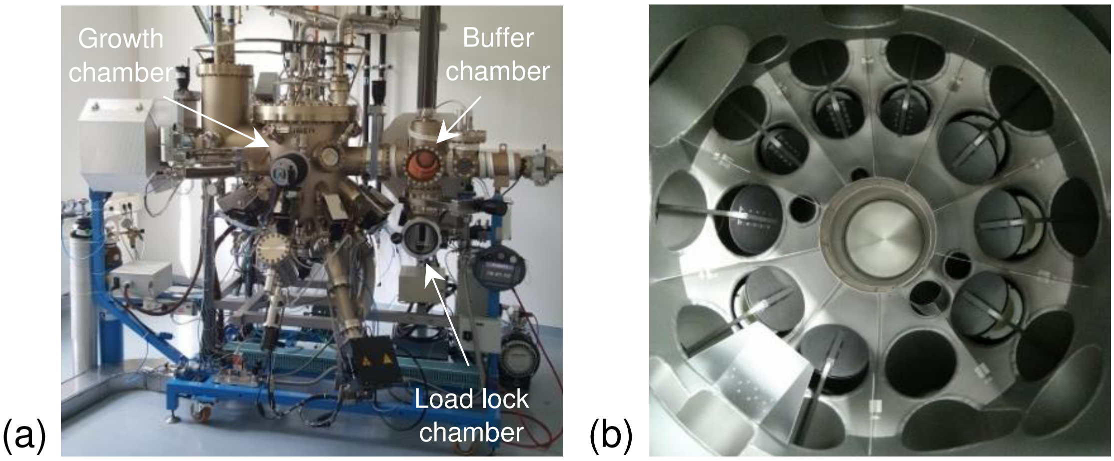

Fig. 3.1: RIBER Compact 21 MBE system for growth of III-V semiconductors at Helmholtz-Zentrum Dresden-Rossendorf. (a) Front-view of the MBE system. (b) Plan-view into the growth chamber with multiple cell ports and mechanical shutters for beam switching.

The buffer chamber is an independent UHV system for storage and preparation of the substrates prior to growth. A base pressure in the order of 10^{-8} Pa is obtained by pumping the buffer chamber with an ion pump. UHV conditions can be improved by activating additionally a titanium sublimation pump. Before a Si substrate is transferred into the growth chamber, it is degassed at an outgassing station in the buffer chamber for 2 hours at a temperature of 450 °C. This is necessary in order to remove potential surface contaminants, and to provide a clean substrate surface for growth. Outgassed substrates can be transferred through the opened gate valved into the growth chamber by a manually operated magnetic transfer rod. The substrate platen is then mounted onto the manipulator.

The growth chamber is a vertical epitaxy reactor as schematically depicted in Fig. 3.2. It consists of a large vessel, an UHV system, a heatable substrate manipulator, thermal effusion cells with mechanical shutters, cryopanels, and measurement instruments for *in situ* and real-time analysis.

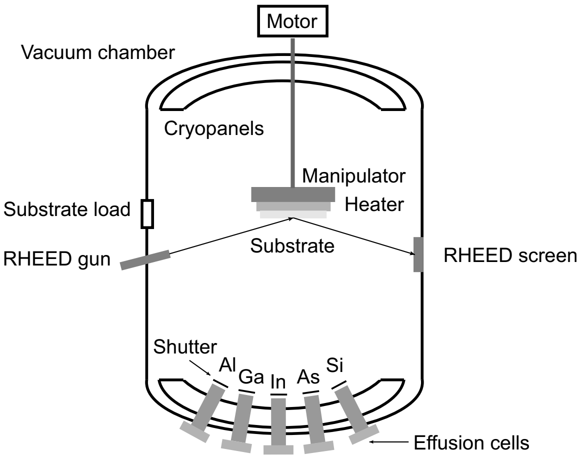

Fig. 3.2: Schematic illustration of the vertical epitaxy chamber of the MBE system.

In order to obtain UHV conditions inside the growth chamber, an ion pump and a titanium sublimation pump are used. Moreover, a cryogenic pumping system is attached to the vessel, and operated by liquid helium at a temperature of 13 K. Additionally, large-area cryopanels, that are filled with liquid nitrogen, are mounted at the inner sidewalls of the vessel. A background pressure of less than $7{\cdot}10^{-9}$ Pa can be achieved in the growth chamber in standby conditions. Thermal effusion cells for group-III elements, i.e. Al, Ga and In, and for dopants, i.e. Si and Be, are mounted to the growth chamber. For epitaxial growth of III-arsenides and III-nitrides, a valved-cracker cell for As, and a valved RF-plasma cell for N are additionally installed at the MBE system. The cryopanels also thermally isolate the effusion cells from each other. The interior view of the clean growth chamber (during the installation of the MBE system) with multiple cell ports and mechanical shutters for beam switching is shown in Fig. 3.1 (b). The substrate manipulator can be heated up to temperatures as high as 800 °C. The substrate can be rotated with a motor to ensure a homogeneous deposition of the materials. The substrate temperature is measured by an optical pyrometer, which was calibrated at an emission wavelength of 900 nm by taking into account the emissivity of silicon (ε_{Si}=0.67). The substrate temperature can be also measured with a thermocouple on the backside of the substrate and in a small distance from it. The background pressures in the load lock, buffer and growth chambers are measured by ion gauges. The substrate temperature, effusion cell temperatures and mechanical shutters are controlled via the dedicated commercial software *Crystal*. The software enables to prepare automated growth recipes that take over the technical implementation of the growth experiments.
The RIBER Compact T21 MBE system is equipped with several measurement instruments. The most important *in situ* analysis technique is reflection high energy electron diffraction (RHEED). RHEED yields structural information of the substrate surface during its preparation and crystal growth, and will be presented in the next section. Furthermore, quadrupole mass spectrometry can be applied to monitor residual gas molecules and impurities. Real-time reflectometry on thin films can also be used in order to determine the thicknesses of the growing layers or the composition of ternary alloys.

3.1.3 *In situ* Reflection High Energy Electron Diffraction

In situ reflection high energy electron diffraction is employed in the present dissertation for real-time monitoring of crystal growth of GaAs-based nanowires. RHEED provides valuable crystallographic information of the growing structure. It is a standard MBE tool, consists of an electron gun and a fluorescent screen, and can be used during crystal growth owing to the UHV conditions.
RHEED is an electron diffraction technique that relies on the elastic scattering of electrons on the atomic planes of a crystallographic surface. The collimated electron beam with electron energies typically in the range of 10 to 15 keV (corresponds to wavelength smaller than 0.1 $\AA$) is generated by the RHEED gun via thermal emission of electrons from a tungsten filament. The electron beam hits the surface under incident angles of 0.5 to 2° with respect to the substrate

surface [195]. The grazing-incidence configuration enables a high surface sensitivity, and allows one to probe the upper most atomic planes of the growing crystal surface. The scattered electron beams hit the fluorescent screen on the opposite site of the RHEED gun. Diffraction patterns are recorded at the RHEED screen. They present a direct map of the reciprocal space ($\vec{k}$ space) of the crystal lattice of the growing surface, and are best dealt within the crystallographic construct of the Ewald sphere. Two conditions must be fulfilled in order to explain the origin of diffraction spots. That is, (i) the magnitude of the wave vector $\vec{k_{in}}$ of the incoming electrons is equal to that of the wave vector $\vec{k_{out}}$ of the scattered electrons, whereas only the direction of $\vec{k_{out}}$ has changed (elastic scattering on a crystal surface), and (ii) the difference between both wave vectors corresponds to a reciprocal lattice vector $\Delta\vec{k}$ according to Eq. 3.5

$$\vec{k_{out}} - \vec{k_{in}} = \Delta\vec{k}, \tag{3.5}$$

which results in constructive interference [77]. In other words, constructive interference occurs only when the endpoints of both wave vectors are located on a sphere of the radius $|\Delta\vec{k}|=2\pi/a_\perp$ with $a_\perp$ as the out-of-plane lattice parameter of a crystalline surface in the real space (Laue-theory). The sphere construction of RHEED scattering is depicted in Fig. 3.3 (a). Depending on whether the crystalline surface is atomically smooth or rough, streaks or spots appear as diffraction patterns at different azimuths of the rotating substrate due to fulfillment of the interference conditions of the scattered beams. Typical spotty RHEED patterns of twinned ZB and WZ GaAs nanowire sections, that are observed during growth of GaAs nanowires on Si(111) substrates, are shown in Figs. 3.3 (b) and (c) respectively.

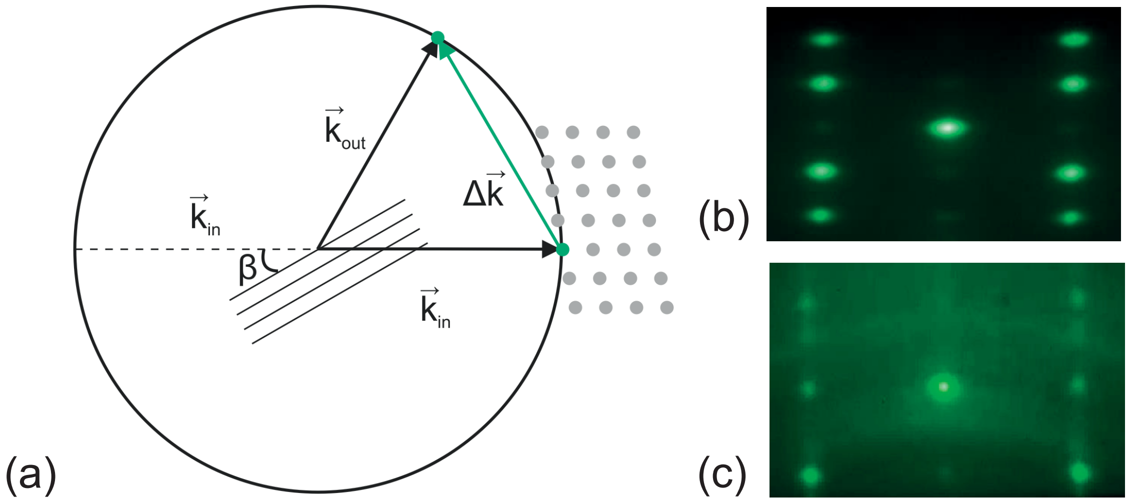

Fig. 3.3: Real-time observation of crystal growth of GaAs nanowires on Si(111) substrates using *in situ* RHEED. (a) Sphere construction of RHEED scattering on crystalline surfaces. (b), (c) RHEED patterns of twinned ZB (b) and WZ GaAs nanowire segments (c) along the $\langle 1\bar{1}0\rangle$ direction.

In the center of the diffraction patterns in Figs. 3.3 (b) and (c), a RHEED spot with high intensity occurred. The so-called specular spot is attributed to scattering of the incident electron beam on the crystal surface under an identical angle. In all as-grown nanowire samples, the specular spot originates from the Si(111) substrate, since the GaAs structures only cover a small fraction of the total surface area of the substrates. Scattering angles, that are different from the incident angle, and that satisfy the interference conditions, appear as spots of lower intensity. The bright diffraction spots, that are not on the azimuth of the specular spot originate from GaAs nanowires. The onset of these diffraction spots on the screen as well as their intensity correlates with the number density of GaAs structures (i.e. nanowires) on the substrate. Besides the qualitative information of the type of crystal phase, in which the nanowires grow, RHEED is furthermore employed for real-time measurement of growth rates of crystalline thin films on their substrate. Since the effective growth rates of nanowires are different from thin films due to a different growth mechanism and growth kinetics (i.e. significant contribution of surface diffusion of growth species to nanowire growth), all beam fluxes are employed within this study as calibrated for planar growth of GaAs thin films on GaAs(001) substrates. For determination of growth rates of GaAs thin films on GaAs(001) substrates, oscillations of the intensity of the specular spot are recorded as a function of the growth duration at the RHEED screen. The period of oscillations corresponds to the time, that is needed for growth of one complete monolayer of GaAs in the $\langle 001 \rangle$ direction. In other words, the growth rate can be measured by counting single monolayers of deposited material during a certain time interval. For *in situ* monitoring of crystal growth using the RIBER Compact T21 MBE system, an electron gun of STAIB Instruments is used. It is operated by a voltage of 12 kV and a filament current of 1.55 A. All RHEED patterns are recorded and evaluated using the software *Safire*.

3.2 *Ex situ* Characterization Techniques

The most important analysis techniques for post-growth investigation of the nanowire samples are electron microscopy methods. Scanning electron microscopy (SEM) analysis is performed routinely on all as-grown samples in order to study the growth-related properties of the nanowires, such as shape, dimensions and number density on the substrate. Different transmission electron microscopy (TEM) techniques are employed to selected nanowire samples for analysis of the crystal structure of the nanowires, the nanowire/substrate interface, and the composition of GaAs-based nanowire heterostructures. Atomic force microscopy (AFM) is used for the development and investigation of the *in situ* surface modification procedure of native-SiO_x/Si(111) substrates, but also for the analysis of the size and number density of the Ga droplets in the droplet samples. Spectroscopic ellipsometry (SE) and X-ray photoelectron (XPS) spectroscopy are employed for determination of the thickness and composition of the native-SiO_x. The combination of all analysis results allows one to draw conclusions about the physical processes, that take place on the substrate during droplet formation and nanowire growth. Finally, photoluminescence (PL) spectroscopy is performed on a selected nanowire sample to study the photon emission of complex nanowire heterostructures.

3.2.1 Scanning Electron Microscopy

Scanning electron microscopy is applied to examine the shape, dimensions (diameter and length), size uniformity, number density, number yield, verticality and growth direction of the as-grown nanowires on their substrate. Moreover, the number density of the Ga droplets is determined by SEM analysis. SEM samples are prepared by cleaving the Si(111) substrate with the deposited Ga droplets or as-grown nanowires into ~0.5×0.5 cm^2 specimens. The specimens are then mounted on special SEM sample holders using conductive copper tape. Two types of SEM samples holders are used, which enable the investigation of the as-grown nanowires in plan-view and side-view configuration respectively. In plan-view configuration, the electron beam scans perpendicular to the sample surface (parallel to the nanowire axis), while the electron beam scans parallel to the sample surface (perpendicular to the nanowire axis) in side-view configuration. By tilting the sample holders in both configurations, tilt angles in the range from 0 to 90° can be covered, and selected scan positions in tilt-view configuration realized.

A Zeiss NVision 40 Cross Beam microscope is used for analysis of the Ga droplet and GaAs-based nanowire samples. The system is equipped with a high-resolution SEM and a Ga-focused-ion-beam (FIB) column to provide imaging and machining of nanoscale samples. SEM of all as-grown droplet and nanowire samples is applied regularly for imaging, while FIB finds its application in the preparation of ultrathin lamellae of selected nanowire samples for HRTEM analysis. The SEM is equipped with a Schottky field-emission electron gun, where a local electric field is generated in order to extract primary electrons from the cathode. These primary electrons are accelerated to anode using voltages in the range of 5 to 20 kV, and then pass through a system of electromagnetic coils. The coils shape the primary electrons to a finely focused beam before it hits the sample. In imaging mode, the sample is systematically scanned line-by-line using an electron beam deflection system. During scanning, the primary electron beam interacts with the atoms of the sample and various types of signals are produced in different depths of the sample, i.e. secondary electrons, back-scattered electrons, Auger electrons, and characteristic x-ray radiation (including bremsstrahlung). A SEM micrograph contains topographic and material information. The topographic information is obtained from the secondary electrons, while the material contrast is produced by the back-scattered electrons, and the result of different atomic species in the sample. The SEM is equipped with an Everhart-Thornley secondary electron detector for topographic imaging, and a back-scatter electron detector for material imaging. Moreover, an in-lens detector is installed for the detection of both secondary and back-scattered electrons. The in-lens detector is exclusively used for imaging of the droplet and nanowire samples. Electron gun operation voltages in the range of 5 to 10 kV, working distances in the range of 3 to 5 mm, and magnifications in the range of 10000 to 80000 are found as appropriate imaging conditions for the droplet and nanowire samples. Special care was taken to reduce image drift prior to scanning of the sample, which may be caused by vacuum instabilities, stage tilting or thermal effects. This is a crucial pre-requisite for accurate length and diameter measurements of the nanowires from side-view SEM micrographs. For reliable statistics, multiple SEM images are recorded at randomly selected positions of each SEM sample, and a few tens of droplets and nanowires are analyzed per sample. The median values of the measured lengths, diameters and number densities as well as their standard deviations are calculated from the measured data. The number density of vertical GaAs nanowires is determined from plan-view SEM micrographs using

$$N = \frac{n_{NWs}}{A_{sub}}, \tag{3.6}$$

where n_{NWs} is the number of vertical nanowires, and A_{sub} the substrate surface area. Based on the number density of vertical GaAs nanowires N, the number yield of vertical GaAs nanowires Y is calculated by

$$Y = \frac{N}{N_{GaAs}} \cdot 100\% \tag{3.7}$$

with N_{GaAs} as the number density of all GaAs structures. Thus, the number yield of vertical GaAs nanowires is the ratio of the number densities of vertical GaAs nanowires and all GaAs structures. Using Eqs. 3.6 and 3.7, the number densities and number yields of inclined GaAs nanowires and parasitic GaAs crystallites are calculated congruently. Furthermore, the length distributions of selected nanowire samples are analyzed. In these samples, the length measurements are extended to ∼130 nanowires per sample. The software *ImageJ* was used for evaluation of the SEM micrographs.

3.2.2 Transmission Electron Microscopy and Energy Dispersive X-ray Spectroscopy

Transmission electron microscopy is employed for the analysis of the crystal structure of selected GaAs nanowire samples. In particular, high-resolution TEM allows one (i) to identify the crystallographic phase, i.e. cubic ZB and hexagonal WZ, as well as the crystal orientation, (ii) to visualize misfit dislocations at the nanowire/substrate interface and planar defects along the nanowire axis, i.e. SFs and TPs, and (iii) to correlate the crystal structure of the nanowires with the contact angle of the Ga droplets. TEM samples are prepared as follows. Si(111) substrates with as-grown nanowires are cleaved into 0.5×0.5 μm^2 small specimens. Subsequently, the free-standing nanowires are mechanically transferred from their substrates onto meshed carbon-coated Cu-grids. For this purpose, the TEM grids are placed upside-down on the specimens and rubbed carefully against the substrates by applying a gentle force. For cross-sectional HRTEM analysis of the nanowire/substrate interface, TEM lamella preparation was done by *in situ* lift-out using the Zeiss Crossbeam NVision 40 system. To protect the nanowire, a carbon cap layer was deposited beginning with electron-beam-assisted and subsequently followed by Ga-FIB-assisted-precursor decomposition. Afterwards, the TEM lamella was prepared using a 30 keV Ga FIB with adapted currents. Its transfer to a 3 post copper lift-out grid (Omniprobe) was done with a Kleindiek micromanipulator. To minimize sidewall damage, Ga ions with only 5 keV energy were used for final thinning of the TEM lamella to electron transparency. Before inserting into the microscope, the sample holder with the TEM grid is cleaned for 2-3 s using a plasma cleaner to remove potential carbon-based contaminants.

Structural analysis of the nanowires is performed using an image-C_s-corrected Titan 80-300 analytical microscope (FEI). Electrons are supplied by a Schottky field emission electron source. Broad-beam illumination of the TEM specimen is realized by several condenser lenses. While the electron beam passes through the TEM specimen, the electrons are scattered at the atoms of the sample. The type of electrons, that is used for imaging, can be selected by e.g. the objective aperture also called contrast aperture. Non-scattered electrons and electrons scattered into the original beam direction (direct beam) are typically used in bright-field TEM mode, while electrons scattered into finite angles (e.g. diffracted beams) are used in dark-field TEM mode. In HRTEM, the objective aperture is removed from the beam path, and all transmitted electrons are used for the formation of an image, which is captured by a CCD camera. Strictly speaking, HRTEM images are phase contrast images originating from the interference of all transmitted electrons in the image plane. The intensity of the measurement signal at the detector depends on the sample thickness, atomic number and arrangement and accelerating voltage. In this work, an accelerating voltage of 300 kV is used for all structural investigations in HRTEM mode. The microscope employed is C_s-corrected to account for the minimization of the spherical aberration of the objective lens. As a consequence, the information limit is 0.1 nm. All HRTEM images are taken in $\langle 1\bar{1}0 \rangle$ zone axis geometry to ensure a low-index crystal orientation, in which the nanowires exhibit a high crystal symmetry. In particular, fast Fourier transform (FFT) analysis of HRTEM images is carried out to provides structural information of the nanowires in reciprocal space. Complementary, selected area electron diffraction (SAED) is performed at specific positions along the nanowire axis to identify the crystallographic phases, i.e. pure ZB and WZ, and twinned ZB regions, in the GaAs nanowires. For this purpose, a selected area aperture with a diameter of 90 nm is employed to confine a specimen area from which the SAED pattern is captured. For single-crystalline materials, SAED patterns consist of diffraction spots, that are of the same origin as compared to RHEED patterns (Bragg diffraction).

High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) in combination with energy-dispersive X-ray (EDX) spectroscopy is carried out to analyze the chemical composition of the GaAs-based axial nanowire heterostructures. Samples for STEM investigations are used as prepared for HRTEM studies. Compositional analysis of axial nanowire heterostructures is conducted using a Talos F200X scanning/transmission electron microscope (FEI). Here, the electron beam is generated by a high-brightness Schottky field emission electron source using an accelerating voltage of 200 kV. In contrast to HRTEM, a convergent electron beam is focused into a small spot and scanned across the TEM specimen. In HAADF-STEM mode, electrons scattered incoherently and elastically (dominating Rutherford scattering) into high angles (on the order of 3°) are captured with an annular dark-field detector, the so-called HAADF detector. The spatial resolution is 0.16 nm at 200 kV. Besides the qualitative atomic-number contrast HAADF-STEM images, compositional analysis of the nanowire samples is complemented by EDX spectroscopy. In particular, spectrum imaging analysis based on EDX spectroscopy enables the element mapping of selected nanowire segments by detecting the electron-induced X-ray emission of those atoms, that are contained in the sample. For this purpose, at each point in the scanned area, an EDX spectrum is recorded. EDX element maps of the GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures reveal the distribution and concentration of Al inside the $Al_xGa_{1-x}As$ nanowire segments. All TEM, STEM and EDX measurements for this dissertation were performed by **René Hübner** at the Institute of Ion Beam Physics and Materials Research at Helmholtz-Zentrum Dresden-Rossendorf.

3.2.3 Atomic Force Microscopy

Atomic force microscopy is employed to analyze the size of the Ga droplets, i.e. the diameter, height and contact angle. Surface scans are performed in order (i) to determine the diameters and contact angles with high accuracy, which was not possible by SEM since the droplet dimensions are close to its resolution limit, and (ii) to characterize the native-SiO_x at different stages of the *in situ* surface modification procedure, i.e. detection of surface roughness, and nano-sized openings in the SiO_x.

The MultiMode 8 HR-AFM system (Bruker) is employed for surface analysis. The system is operated in tapping mode. AFM samples are prepared equally to SEM samples by cleaving the as-received or processed native-SiO_x/Si(111) substrates into small specimens. After mounting the specimens on the AFM system, the cantilever is attached to the tip holder, which is then placed face-down on the AFM sample. Al-coated Si cantilevers with a nominal tip radius of 7 nm and a resonance frequency of 190 kHz are employed for the measurements. The laser diode of the system is aligned with respect to the cantilever by maximizing the reflected intensity from the backside of the cantilever at the detector. The reflected light is detected by a position-sensitive photodiode, that is aligned with respect to its zero position. In tapping mode, the Si cantilever is driven by a piezoelectric ceramic, which oscillates at its resonance frequency. A x-y deflection system enables line-by-line scanning of the oscillating cantilever across the sample surface. Due to interactions of the oscillating tip with the sample surface, that is initiated by attractive and repulsive forces as a result of varying surface potentials, the oscillation amplitude and/or resonance frequency changes, but is kept constant by a feed-back loop. The corresponding change of the deflection of the reflected intensity signal is detected at each probe position on the surface by the position-sensitive photodiode. The detected signal is converted into an electrical signal from which the surface morphology of the sample is reconstructed. The advantage of the tapping mode compared to the contact mode is its non-destructive performance. Therefore, degradation of the tip as well as the sample surface can be mostly excluded and comparability of measurements on different AFM samples with the same cantilever can be assured. Since the cantilever is operated at relatively large oscillation amplitudes, where attractive long-range forces, i.e. electrostatic and van-der-Waals forces, are dominant, the lateral resolution is limited to a few nanometers, while a vertical resolution along the z-axis of 0.01 nm can be achieved. Moreover, the resolution strongly depends on the radius of curvature of the cantilever tip. Surface features, that are smaller than

~10 nm cannot be resolved with the employed Si probe. AFM surface scans are performed on a sample surface with an area of 2×2 μm^2. In order to obtain surface scans of high quality, a low scan rate of 1 Hz and a large number of probe positions per line (i.e. 512) is used, that results in a step size of 4 nm.

In addition to conventional AFM in tapping mode, conductive AFM (c-AFM) in contact mode is performed on selected samples for complementing surface analysis. Compared to conventional AFM, the strength of c-AFM relies on the combination of two independent measurement signals at each probe position, which is (i) the deflection of the cantilever, that enables access to the topography information of the surface, and (ii) the electrical current flow between the conductive probe tip and the sample surface, that provides the conductivity information of the surface. Similar to conventional AFM, the deflection of the cantilever is detected by an optical system based on a laser diode and a position-sensitive photodiode, while the electrical current is detected by an amplifier and an analog-digital converter, that translates the analog current signal to a digital voltage signal [196]. Besides the highly conductive probe tip and the amplifier/converter unit, the integration of a voltage supply source is essential in the measurement set-up since a negative bias voltage is applied to the backside of the substrate in all measurements. The measurement signal is the tunnel current density of the injected electrons from the substrate through the native-SiO$_x$ into the conductive Si probe. In the physical sense, the tunnel mechanism is driven by the applied electrical field, that assists the transmission of the injected electrons from the conduction band of the substrate through a SiO$_2$ barrier into the conduction band of the Si probe. The shape of the barrier depends on the applied electrical field, where high electric fields result in tunneling through a triangular barrier (or Fowler-Nordheim tunneling), while low electric fields assist tunneling through a trapezoidal barrier (direct tunneling). The Fowler-Nordheim tunnel current I is given by

$$I = A_{em} \frac{q^2 m_0}{8\pi h m_{eff}} \frac{1}{t(E_{ox})^2} \frac{E_{ox}}{\Phi} \cdot exp(-\frac{8\pi \sqrt{2 m_{eff} q}}{3h} \frac{\nu(E_{ox})}{E_{ox}} \Phi^{3/2}), \tag{3.8}$$

where A_{em} is the emission area, q the elementary charge, m_{eff} the effective electron mass, m_0 the free electron mass, h Planck constant, E_{ox} the oxide electric field, Φ the barrier height, and $\nu(E_{ox})$ and $t(E_{ox})$ constants that account for image charge effects due to the applied electric field [197]. It has been shown that c-AFM measurements enable the detection of local variations of the oxide thickness [196, 198], electrically weak spots [197], oxide inhomogeneities, surface roughness, and nano-sized holes. Compared to surface scans in conventional AFM, c-AFM yields a better lateral resolution down to a few nanometers. This is attributed to nano-sized grains of the conductive coating of the cantilever tips, that offer arrival points for the tunneling current, even when their nominal tip radius of curvature is larger than that of non-coated standard Si tips. Therefore, c-AFM is suitable and exclusively applied in order to detect nano-sized openings in the native-SiO$_x$, which cannot be resolved by the conventional AFM and the employed standard Si probe. The measurements are performed at room temperature under UHV (base pressure of 10^{-7} Pa) at the Variable Temperature Scanning Probe Microscope (Scienta Omicron). Pt/silicide-coated Si probes with excellent electrical conductivity and good wear resistance are employed. The Pt/Si probes exhibit a nominal tip radius of curvature of 20 nm. A gentle force of 3 nN was applied in order to keep the tip in contact with the native-SiO$_x$. A bias voltage of –2 V is applied, and tunneling currents in the range of 1 to 100 pA are measured. Surface scans of areas of 1×1 μm^2 and 75×75 nm^2 are performed at random positions of selected samples. For close-up scans of distinct surface features, the scan area was reduced to 75×75 nm^2. The scan time per probe point was 0.5 ms. For evaluation of all captured surface scans, the software *Gwyddion* was used. All c-AFM measurements for this dissertation were performed by **Martin Engler** at the Institute of Ion Beam Physics and Materials Research at Helmholtz-Zentrum Dresden-Rossendorf.

3.2.4 Spectroscopic Ellipsometry

Spectroscopic ellipsometry is performed in order to determine the thicknesses of the native-SiO$_x$ layer of the employed Si(111) substrates. SE is based on the mathematical relation, that is described by

$$\rho = \frac{r_p}{r_s} = \tan\Psi e^{i\Delta}, \tag{3.9}$$

where ρ is the complex reflectance ratio of r_p and r_s, r_p and r_s are the amplitudes (normalized to their initial values) of the p and s components perpendicular and parallel to the plane of incidence, Ψ is the amplitude ratio after reflectance, and Δ is the phase shift between p and s components. Following Eq. 3.9, the parameters Ψ and Δ are measured as a function of the photon energy using a fixed angle of incidence of 75.2°. The measurements are performed using the variable angle spectroscopic ellipsometer WVASE 32 (J. A. Woollam). Since the film thickness in SE is determined indirectly, a layer model that includes the stack sequence, the thicknesses of all individual layers, and their optical constants (i.e. refractive index and dielectric function) was employed. Here, a native-SiO$_x$ layer with an initial film thickness of 2 nm and an infinitely thick bulk Si were used. The optical constants were applied as provided by the tool manufacturer. Based on the established two-layer model, theoretical Ψ and Δ were calculated by varying the thickness parameters and optical constants. The thicknesses of the native-SiO$_x$ layer are determined by best matching of the calculated Ψ and Δ with the measured ones.

3.2.5 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy is performed for qualitative analysis of the chemical composition of the native-SiO$_x$ layer of the employed Si(111) substrates. XPS is a surface-sensitive analysis technique and based on the external photoelectric effect. According to this effect, irradiation of the sample with a beam of X-rays results in emission of photo-excited electrons from the core levels of the atoms contained in the sample. The kinetic energy of the emitted electrons is detected using a hemispherical energy analyzer. Due to the fact that the emission of the photoelectrons depends on the energy, element and atomic orbital, XPS not only allows one to draw conclusions about the concentration of elements in the sample, but also about its chemical environment, bond ratios, oxidation and valence band states. The binding energy E_B is obtained using

$$E_B = E_{Ph} - E_{kin} - \Phi_S \tag{3.10}$$

with E_{Ph} as the photon energy of X-ray excitation, E_{kin} as the kinetic energy of the emitted photoelectrons, and Φ_S as the work function of the spectrometer. Element-dependent characteristic spectral lines (peaks) of high intensity are present in a XPS spectrum and used for qualitative and quantitative analysis of elements and their concentration in the sample. Due to the spin-orbit-coupling of the electrons, peak splitting with characteristic intensity ratios typically emerges for p-, d- and f-orbitals. Spectral lines produced by Auger-electrons and electron energy loss may be additional present in the spectrum. Spectral lines produced by photoelectrons are shifted to lower or higher binding energies as the result of change of the chemical state of elements (chemical shift). Qualitative XPS analysis of native-SiO_x/Si(111) substrates was performed using the Microlab 310F Auger-electron spectrometer (Fisons) with a hemispherical sector analyzer and an additional Al/Mg X-ray source. For XPS analysis, the monochromatic Al K_α X-ray source operated at 1486.6 eV was used. All XPS measurements were performed with an absolute pressure lower than $2{\cdot}10^{-9}$ mbar. Overview XPS spectra were recorded with a pass energy of 100 eV, a step width of 1 eV and a dwell time of 0.2 s (4 scans). Detailed spectra of the O 1s and Si 2p peak were measured using a pass energy of 10 eV, a step width of 0.2 eV and a dwell time of 0.2 s (20 scans). The binding energy scale of all spectra was calibrated to the C 1s peak at 285.0 eV. For qualitative analysis of the O 1s and Si 2p peaks, the background (O 1s: linear, Si 2p: Shirley) was subtracted. Voigt profiles with 30% Lorentz and 70% Gauss were used for peak fitting. For fitting of the Si 2p peak, the spin-orbit splitting was set to 0.61 eV and the intensity ratio of the peak doublet (Si $2p_{3/2}$:Si $2p_{1/2}$) was set to 2:1 [199]. The effect of electric charge offset could be fully eliminated by using a special specimen holder to avoid an operation with a flood gun. For evaluation of all recorded spectra, the software *CasaXPS* was used. All XPS measurements for this dissertation were performed by **Stefan Facsko** at the Institute of Ion Beam Physics and Materials Research at Helmholtz-Zentrum Dresden-Rossendorf.

3.2.6 Photoluminescence Spectroscopy

Photoluminescence spectroscopy is performed to study the photon emission of single GaAs/ $Al_xGa_{1-x}As$ quantum dots in axial nanowire heterostructures, which are embedded as cores in core-shell nanowires. Luminescence is the emission of optical radiation (photons) from any type of matter. It occurs from transitions of excited states to their ground states in an optoelectronic system. Depending on the source of excitation, various luminescence techniques are distinguished. PL uses excitation via absorption of photons (complementary process to photon emission), whereas other techniques such as cathodoluminescence and thermoluminescence use excitation via energy transfer from electrons or thermal energy, respectively.

PL spectroscopy is used as a standard technique to probe the band gap and electronic structure of semiconductors. In PL spectroscopy, the sample is irradiated with a laser of a certain wavelength. The energy of the laser photons E_{Ph} should be at least equal to or larger than the band gap of the semiconductor to be probed ($E_{Ph} > E_g$). Then, the intensity of the light scattered at the sample surface is measured as a function of its wavelength or photon energy, respectively, and plotted in a PL spectrum. PL measurements are typically performed at cryogenic temperatures to avoid heating effects, i.e. the excitation of carriers in the conduction band by thermal energy. This requires the use of a closed-cycle cryostat for sample cooling. For PL spectroscopy on undoped semiconductors, excitation of electrons from the valence band into the conduction band is necessary. The recombination process can take place via radiative and non-radiative paths. Radiative transitions comprise the emission of photons with an energy equal to or slightly lower than the band gap, that occur for instance from band-to-band recombination, recombination of free excitons or neutral donor-acceptor pairs [200]. Non-radiative transitions arise for instance from excitation of phonons, carriers (Auger electrons) or impurities [200].

In this work, PL measurements were performed at the Institute of Ion Beam Physics and Materials Research at Helmholtz-Zentrum Dresden-Rossendorf, and at the Department of Material Science and Technology at the University of Crete, Heraklion, Greece **in collaboration with Nikos T. Pelekanos and Nikos G. Chatzarakis**. Micro-PL measurements at Helmholtz-Zentrum Dresden-Rossendorf were performed using a commercial PL spectrometer (HORIBA) with a frequency-doubled Nd:YAG laser (wavelength of λ=532 nm) and an InGaAs detector (response up to λ=1.5 μm). The measurements were carried out on ensembles of a very few nanowires at 4 K using a closed-cycle helium-cryostat. The excitation power was 10 μW. The laser spot size was approximately 1 μm. As-grown nanowires were transferred from their original substrate onto a Si wafer. At the University of Crete, time-resolved micro-PL measurements were performed using a home-built PL set-up with a tunable Ti-sapphire laser with a wavelength locked at λ=740 nm and a liquid-nitrogen cooled-CCD camera with a Si chip. The sample was irradiated with femtosecond laser pulses and a duration of 13 ns between two pulses. The measurements were performed on single nanowires at various temperatures in the range from 77 to 130 K using a closed-cycle liquid-nitrogen-cryostat. The laser power was 700 μW, and the spot size approximately 1 μm. Due to the use of several optics between the source and the sample surface, the estimated excitation power on the sample was 35 μW/μm^2. As-grown nanowires were transferred from their original substrate onto an undoped Si wafer with Au pads.

4 *In situ* Surface Modification Procedure (SMP) of native-SiO$_x$/Si(111) Substrates

This chapter presents original results in the self-catalyzed growth of GaAs nanowires on native-SiO$_x$/Si(111) substrates. In particular, it focuses on the development and investigation of a novel *in situ* preparation method of the substrates prior to nanowire growth. The developed method is denoted as surface modification procedure. The SMP successfully decouples the two roles of Ga droplets in the self-catalyzed growth of GaAs nanowires on native-SiO$_x$/Si substrates. The decoupling is a pre-requisite for mastering nanowire growth on the Si platform, and enables an unprecedented level of growth control. The main findings presented in this chapter have been published in the ACS Journal Crystal Growth & Design entitled as "Decoupling the Two Roles of Ga Droplets in the Self-Catalyzed Growth of GaAs Nanowires on SiO$_x$/Si(111) Substrates" [47] as well as in the IOP Journal Nanotechnology entitled as "A simple route to synchronized nucleation of self-catalyzed GaAs nanowires on silicon for sub-Poissonian length distributions" [201].

4.1 Conventional Growth Processes and Their Challenges

During the last decade, self-catalyzed growth of GaAs nanowires on native-SiO$_x$/Si(111) substrates has been studied using MBE [31, 57, 62, 68, 202, 203]. Research efforts have contributed significantly to good control of the nanowire shape, and free-standing nanowires with ZB crystal structure can be produced [69, 112, 124, 137]. Nevertheless, control of the nucleation stage in self-catalyzed growth of GaAs nanowires on native-SiO$_x$/Si(111) substrates is still lacking due to the complex interplay of multiple physical mechanisms that take place in parallel on the substrate surface during supply of Ga and As$_4$ beams as presented in Chapter 2.3.2. In particular, the Ga droplets have a double role in the self-catalyzed growth of GaAs nanowires on native-SiO$_x$/Si(111) substrates: the Ga-induced formation of SiO$_x$ openings, and the Ga-assisted nucleation and growth of GaAs nanowires inside these openings. The difficulty of decoupling these two mechanisms introduces several challenges in the conventional growth process. That is,

1. non-synchronized nanowire nucleation on the substrate, which typically leads to a broad spread in the length distribution of nanowires [69, 202, 203],
2. the inability to deliberately control the number density of GaAs nanowires at fixed growth conditions without prior substrate patterning [62, 69, 97],
3. low number yields of vertical GaAs nanowires compared to parasitic growth of faceted GaAs islands (cannot be suppressed) [68],
4. the diameter of the nanowires cannot be controlled independently from their number density [204],
5. problems to reproduce the growth on substrates from different batches, which strongly depends on the properties of the native-SiO$_x$ [61].

A prevalent but costly approach for solving the aforementioned challenges is the pre-patterning of thermally grown SiO$_2$ layers on Si(111) substrates. This is typically achieved by electron beam lithography [107, 205, 206, 207, 208] or nanoimprint lithography [209, 210], but often involves multiple *ex situ* substrate preparation steps and increases the risk of substrate contamination due to various chemical treatments. Additionally, the presence of a thin SiO$_x$ layer even inside the patterned SiO$_2$ holes has been reported [111, 205], which may raise further complications in the nucleation mechanism of both the Ga droplets and the emerging nanowires. Although the exact nanowire nucleation mechanism on patterned SiO$_2$/Si substrates has not yet been fully unraveled, an exceptionally high length uniformity (standard deviation of ~2% for 5.5 μm long nanowires [209]), high nanowire yields (up to 90-95% [206, 207, 208]), an independent control of the nanowire diameter from their number density (defined by deliberate combination of number and sizes of SiO$_2$ holes within each array), and high growth reproducibility [207] have been demonstrated.

Such a high level of growth control is still lacking for self-catalyzed growth of GaAs nanowires on untreated native-SiO$_x$/Si(111) substrates. But several approaches have been proposed in order to overcome the aforementioned challenges without the need of prior substrate patterning. A simple approach in order to control the number density of GaAs nanowires is based on the tuning of the substrate temperature and/or the Ga flux, which enabled the control of the nanowire number density typically within 1 or 2 orders of magnitude (in the range of 10^7-10^8 cm^{-2}), but had a significant impact on the nanowire diameter and yield [62, 68, 97, 203]. Matteini *et al.* employed a high Ga flux in the nanowire nucleation stage in order to obtain a high number density of nanowires (2-8×10^7 cm^{-2}), and a reduced Ga flux in the nanowire elongation stage in order to decrease the nanowire diameter (40-140 nm) [97]. Although this two-step growth approach resulted in independent control of the nanowire diameter from the number density, the nanowires exhibited a tapered morphology due to decreasing droplet size during growth. An alternative two-step approach involves Ga deposition and droplet formation at high Ga flux prior to nanowire growth (variation of nanowire number density within 1-4×10^8 cm^{-2}), and nanowire nucleation and growth at low Ga flux (small nanowire diameters) [211]. Additionally, the insertion of a short substrate annealing in between the pre-deposition and growth step (performed at the growth temperature) improved the length uniformity (standard deviation less than 2% for ~2 μm long nanowires), although the formation of SiO$_x$ holes and nucleation of the nanowires were induced below the same Ga droplets [211]. Tan *et al.* employed porous oxide templates that were fabricated by controlled chemical oxidation of bare Si substrates subsequent to the removal of the native-SiO$_x$ [204]. Despite the achievement of a fairly good length uniformity (standard deviation less than 4% for ~1.2 μm long nanowires) and the variation of the number density of the nanowires over a wide range (10^7 to 10^9 cm^{-2}), the diameter and number yield of the nanowires show a strong dependence on their number density [204]. More complicated approaches are based on the epitaxial growth of faceted GaAs islands on oxide-free Si(111) substrates using droplet epitaxy. For instance, Hakkarainen *et al.* proposed lithography-free nanohole templates [212]. They were obtained by *ex situ* oxidation of Si substrates subsequent to *in situ* growth of GaAs islands, and by thermal decomposition of the oxidized islands via *in situ* substrate annealing [212]. This approach resulted in a controllable number density of nanowires (within the range of 10^8 cm^{-2}) and, furthermore, in highly uniform nanowire lengths with a remarkable narrow (sub-Poissonian) length distribution as indicated by a standard deviation of less than 0.7% for $\sim$5.1 μm long nanowires [109, 103]. A second approach based on droplet epitaxy relies on the growth of GaAs islands whose flat top facets served as nucleation sites for GaAs nanowires [67]. Although this method enabled independent control of the number density (within the range of 10^7-10^8 cm^{-2}) and diameter (40-120 nm) of the nanowires, an *ex situ* oxidation step of the substrate was performed prior to nanowire growth to reduce parasitic growth of GaAs islands, and therefore to enhance the yield of vertical nanowires. Moreover, it has been shown that the yield of vertical GaAs nanowires compared to parasitic GaAs islands could be increased by using a high V/III flux ratio during nanowire growth [213].

Reviewing the existing literature implies first, that the independent control of all listed growth challenges within one substrate preparation method is extremely difficult (even if additional *ex situ* substrate processing is performed), and second, that a high level of growth control has not yet been achieved in self-catalyzed growth of GaAs nanowires on untreated non-patterned Si substrates, but would be very desirable for their monolithic integration on the Si platform. To that end, the *in situ* SMP has been developed. In the following section, the physical impact of every single step of the SMP on the substrate is investigated. Furthermore, the effect of the SMP in the subsequent growth of GaAs nanowires on native-$SiO_x/Si(111)$ substrates is discussed.

4.2 Effect of the SMP on the Substrate

The SMP is always performed just before nanowire growth and consists of the following three steps:

Step-1: Thermal annealing of the substrate at a temperature denoted as T_{a1}
Step-2: Ga deposition and droplet formation at a substrate temperature denoted as T_d
Step-3: Thermal annealing of the substrate at a temperature denoted as T_{a2}
$(T_d < T_{a2} < T_{a1})$

A temperature profile of the substrate and the corresponding position of the Ga and As_4 shutters during SMP and nanowire growth is shown in Fig. 4.1.

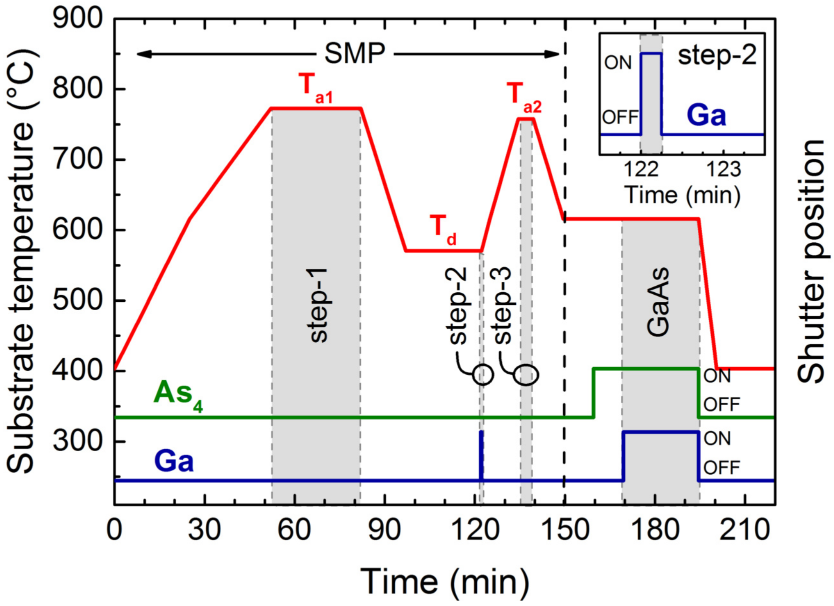

Fig. 4.1: Plot of the temperature of the Si(111) substrate (left axis) and Ga and As$_4$ supply (right axis) during the *in situ* SMP and the nanowire growth process. The inset illustrates a close-up of the Ga supply during SMP step-2. Reproduced with permission from [201]. © 2018 IOP Publishing. All rights reserved.

SMP step-1 concerns an initial thermal annealing of the substrate for 30 min at relatively high T$_{a1}$ in the range of 690 to 770 °C. SMP step-2 comprises the deposition of 2.4 MLs of Ga using a fixed Ga flux of F_{Ga}=0.16 ML/s for 15 s at T$_d$ in the range of 450 to 590 °C. The background pressure in the growth chamber during Ga deposition was in the range of 10^{-11} Torr. SMP step-3 concerns another thermal annealing of the substrate for 5 min (or 20 min) at T$_{a2}$ in the range of 695 to 780 °C in order to evaporate the Ga droplets created during SMP step-2 completely from the substrate surface. All substrate temperatures were measured with an optical pyrometer.

The SMP was performed on 3-inch Sb-doped Si(111) substrates. Two types of Si(111) substrates, that originate from different batches (referred to as batch A and B), are employed for preparation of the nanowire samples. A substrate of each batch was selected and initially characterized with respect to its SiO$_x$ thickness, chemical composition and surface roughness. For determination of the thickness of the native-SiO$_x$ layers, SE measurements were performed on each substrate at various positions. The corresponding spectra of Ψ and Δ (identical for all measured positions) are shown in Fig. 4.2 (a). As indicated, the spectra are overlapping and only a minor difference in Δ was detected. This finding implies that the substrates are uniformly covered by a native-SiO$_x$ layer of a similar thickness. Best fits of measured Ψ and Δ, that are shown for batch A in Fig. 4.2 (b), reveal a SiO$_x$ thickness of 1.9 nm (± 2%) for batch A and 1.5 nm (± 1.5%) for batch B. Second, XPS measurements were performed on each substrate to detect any change in the chemical composition of the native-SiO$_x$. Overview XPS spectra shown in Fig. 4.2 (c) reveal signals from silicon (Si 2p, Si 2s), oxygen (O 1s) and carbon (C 1s). Carbon is attributed to carbon-containing contaminants, that were adsorbed on the surface from the ambient air. The O 1s peak in Fig. 4.2 (d) was fitted with one component at a binding energy of E_B=532.2 eV.

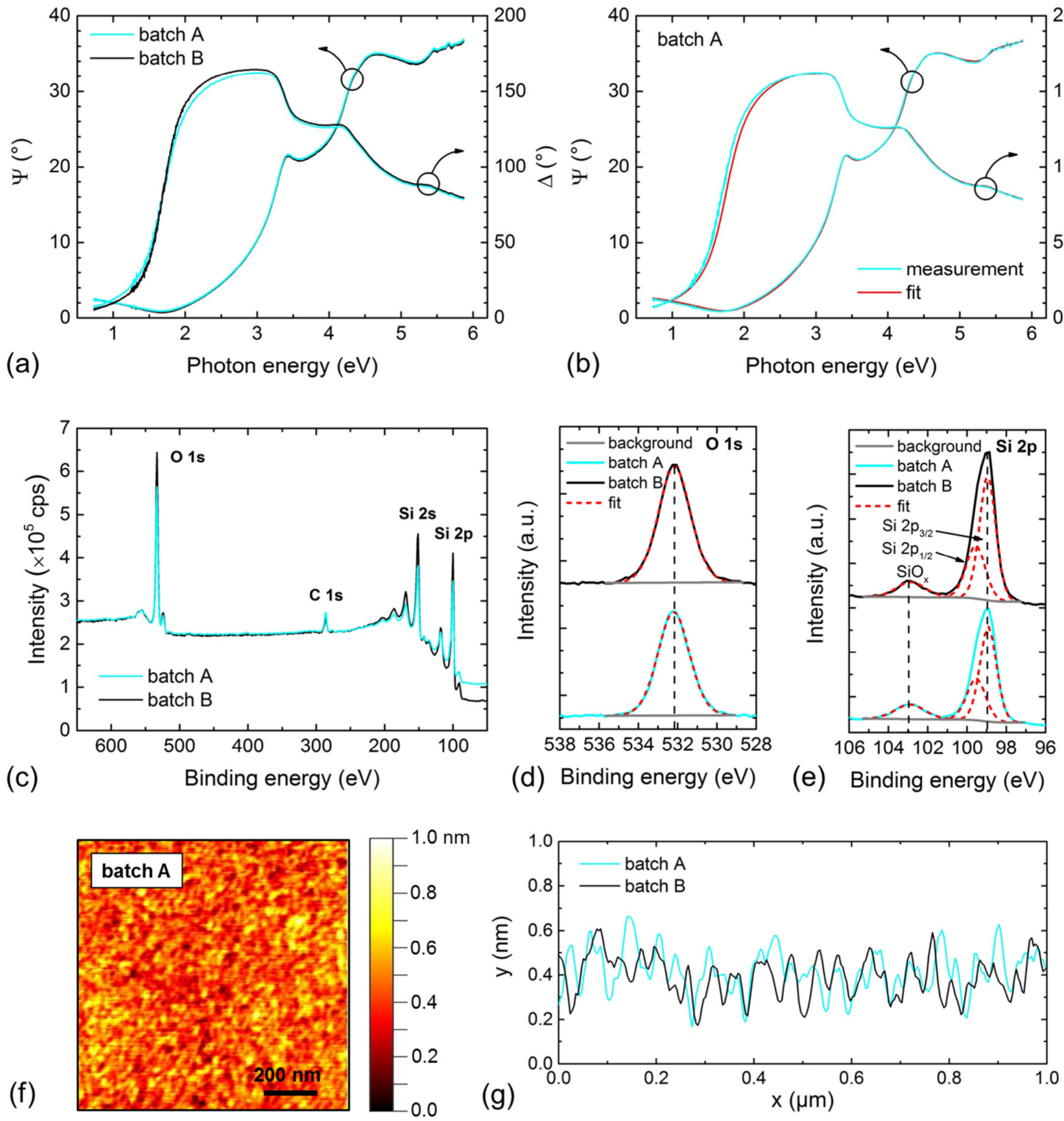

Fig. 4.2: Characterization of native-SiO$_x$/Si(111) substrates of different batches denoted as batch A (cyan color) and batch B (black color). (a) Plot of Ψ (left axis) and Δ (right axis) for both substrates as a function of the photon energy as measured by SE. (b) Best fits of measured Ψ (left axis) and Δ (right axis) for a substrate of batch A revealing a SiO$_x$ thickness of 1.9 nm. (c) Overview XPS spectra of substrates of batch A and B. (d) O 1s and (e) Si 2p peaks of the overview XPS spectra in (c). (f) 1×1 μm^2 AFM image of a substrate of batch A. (g) Representative line profiles of substrates of batch A and B. Figs. 4.2 (a) and (b) are reproduced with permission from [201]. © 2018 IOP Publishing. All rights reserved.

The Si 2p peak was deconvoluted into a metallic Si component (Si 2p$_{3/2}$ at E_B=98.9 eV, Si 2p$_{1/2}$ at E_B=99.5 eV) and an oxidized Si component (SiO$_x$ at E_B=103.0 eV). For a better resolution of the Si 2p doublet (spin-orbit splitting), a lower pass energy would have been necessary. Qualitative XPS analysis of the spectra reveals identical peak positions of the individual components for each substrate. As a result, no change in the chemical composition of the native-SiO$_x$ was found between the different batches. Quantitative XPS analysis was not possible since the native-SiO$_x$ thickness is smaller than the excitation depth, which yields an enhanced generation of photoelectrons from the bulk Si. Finally, AFM measurements were performed on each substrate at various positions to detect any morphological change of the native-SiO$_x$. A representative AFM image of a substrate of batch A is shown in Fig. 4.2 (f). Line profiles along the surface of the substrates (Fig. 4.2 (g)) do not reveal any difference in the surface morphology between the different batches. The average surface roughness of the substrates was (0.5 ± 0.1) nm. Substrates of the same batch are assumed to exhibit identical properties of the native-SiO$_x$.

The substrates were introduced to the Riber Compact T21 MBE system as received without any prior chemical treatment. Before transferring the substrates to the growth chamber, they were out-gassed inside the buffer chamber for ~3 h at 450 °C. The role of every SMP step on the substrate and the underlying physical mechanisms are described in the following.

4.2.1 Roughening of the SiO$_x$ Surface in SMP step-1

First, the role of SMP step-1 in the formation of Ga droplets in step-2 is investigated. For this purpose, four Si(111) substrates with a nominal SiO$_x$ thickness of 1.5 nm (batch B) were annealed at various T_{a1} in the range of 690 to 770 °C and Ga droplets were deposited subsequently in step-2 using always a constant T_d of 570 °C. The SMP was terminated after step-2, and the samples were immediately cooled down to 100 °C in order to maintain the volume and position of the Ga droplets. Subsequently, the size and contact angle as well as the number density of the droplets were determined by AFM and SEM.

For accurate determination of the droplet size and contact angle from AFM surface scans, the effect of the tip geometry and step size on the shape of the droplets has to be considered as illustrated in Fig. 4.3.

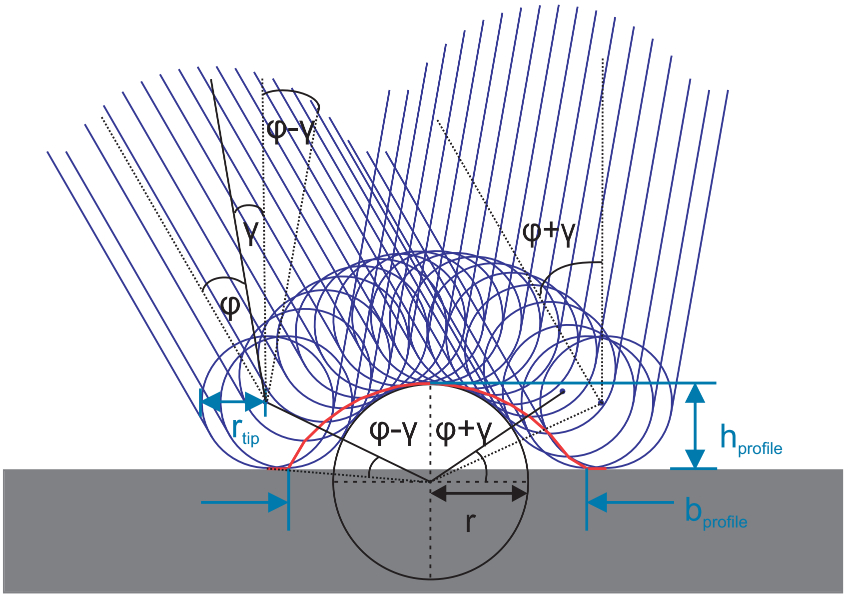

Fig. 4.3: Side-view schematic illustration of the effect of the geometry of the AFM tip on the shape of the Ga droplets. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

Horizontal line profiles through the center of the Ga droplets (in red color) were taken from the surface scans, and analyzed as follows. The base widths $b_{profile}$ and heights $h_{profile}$ as indicated in Fig. 4.3 were extracted from at least 20 line profiles of each sample. In order to calculate the real droplet radii r by taking into account the tip radius r_{tip}, tapering angle φ and tilt angle γ, Eq. 4.1 has been developed from geometrical relations that are shown in Fig. 4.3.

$$r = \frac{h_{profile} - \frac{b_{profile}}{tan(\varphi+\gamma)+tan(\varphi-\gamma)}}{1 - \frac{\frac{1}{cos(\varphi+\gamma)}+\frac{1}{cos(\varphi-\gamma)}}{tan(\varphi+\gamma)+tan(\varphi-\gamma)}} - r_{tip} \tag{4.1}$$

The shape of the droplets was assumed to be partial spheres. A tip radius r_{tip}=7 nm, a tapering angle φ=20°, and a tilt angle γ=10° were used for the calculations. A detailed derivation of Eq. 4.1 is provided in Chapter A. The calculated droplet radii r and the measured AFM profile heights $h_{profile}$ were furthermore corrected by a factor of 0.9093 that takes into account the volume expansion of the droplets due to their oxidation in air after exposure to atmosphere [63]. The corrected droplet radii r_c and heights h_c were used to calculate the contact angle θ as illustrated in Fig. 4.4.

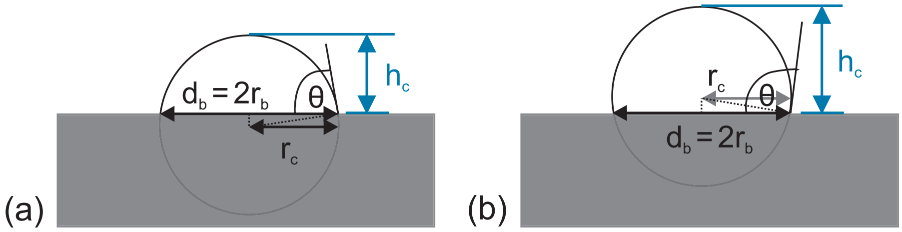

Fig. 4.4: Schematic illustration of the correlation between radius, height, base diameter, base radius and contact angle of a partial sphere shaped droplet on the substrate surface. (a) Droplet with a contact angle smaller than 90°. (b) Droplet with a contact angle larger than 90°. Fig. 4.4 (b) is adapted with permission from [47]. Copyright (2017) American Chemical Society.

The droplet contact angle θ is given by Eq. 4.2 for $\theta > 90°$ and Eq. 4.3 for $\theta \leq 90°$

$$\theta = arcsin(\frac{h_c - r_c}{r_c}) + \frac{\pi}{2}, \tag{4.2}$$

$$\theta = \frac{\pi}{2} - arcsin(\frac{r_c - h_c}{r_c}). \tag{4.3}$$

Both equations return the same contact angle independent of whether the contact angle is larger, smaller or equal to 90°. Therefore, the model is valid for determination of all contact angles of droplets with a shape of a partial sphere.

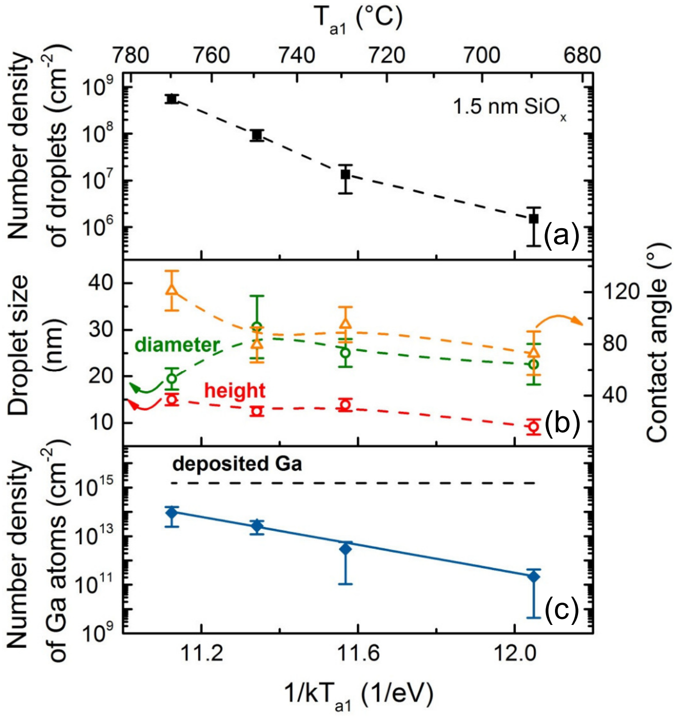

Fig. 4.5: Impact of T_{a1} in SMP step-1 on the formation of Ga droplets on native-SiO$_x$/Si(111) substrates in step-2 (at T_d=570 °C). Analysis of (a) the number density of Ga droplets, (b) the droplet height, diameter, and contact angle, and (c) the number density of Ga atoms on the substrate. The dashed line in (c) indicates the total amount of deposited Ga. Si(111) substrates with a 1.5 nm thin native-SiO$_x$ were used. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

Figure 4.5 presents the analysis of Ga droplets on the substrate in dependence of T_{a1} in SMP step-1. As indicated in Fig. 4.5 (a), the number density of Ga droplets increased from N_{dr}=10^6 cm^{-2} to 10^9 cm^{-2} with increasing T_{a1} from 690 °C to 770 °C. The droplets are characterized by mean diameters in the range of d_c=$2r_c$=19-31 nm, mean heights in the range of h_c=9-15 nm, and mean contact angles in the range of θ=70-120° as shown in Fig. 4.5 (b). From the size and number density of the droplets, the total number of Ga atoms N_{at} inside the droplets per substrate surface area was calculated using Eqs. 4.4 to 4.7, and plotted in Fig. 4.5 (c). First, the calculated contact angle θ was used to determine the droplet base diameter d_b (base radius r_b) in Eq. 4.4 for $\theta > 90°$ and Eq. 4.5 for $\theta \leq 90°$

$$d_b = 2r_b = 2r_c \cdot cos(\theta - \frac{\pi}{2}) = 2r_c \cdot sin\theta, \tag{4.4}$$

$$d_b = 2r_b = 2r_c \cdot cos(\frac{\pi}{2} - \theta) = 2r_c \cdot sin\theta. \tag{4.5}$$

d_b (r_b) is the diameter (radius) of the contact area of the droplet with the substrate surface as shown in Fig. 4.4. Then, r_b and h_c were used to calculate the droplet volume V_{dr}, which is given by

$$V_{dr} = \frac{\pi h_c}{6}(3{r_b}^2 + {h_c}^2) = \frac{\pi h_c}{6}(3h_c \cdot (2r_c - h_c) + {h_c}^2) = \pi {h_c}^2(r_c - \frac{1}{3}h_c). \tag{4.6}$$

Finally, V_{dr} was used to calculate the number of Ga atoms N_{at} inside the droplets per substrate surface area according to

$$N_{at} = n_{Ga} \cdot V_{dr} \cdot N_{dr}, \tag{4.7}$$

where n_{Ga} is the atom density of liquid Ga (n_{Ga}=5.099×10^{22} cm^{-3}), and N_{dr} is the number density of the droplets as measured by SEM. As indicated in Fig. 4.5 (c), the number density of Ga atoms increased from N_{at}=2×10^{11} cm^{-2} to 9×10^{13} cm^{-2} with raising T_{a1} from 690 °C to 770 °C. Compared to the total amount of deposited Ga (dashed line), only a small fraction of supplied Ga atoms sticks to the SiO$_x$ surface, i.e. ∼0.01% at 690 °C, and ∼10% at 770 °C. This finding indicates a significant loss of supplied Ga from the SiO$_x$ surface, which is associated with desorption of Ga adatoms [64, 214], and/or Ga$_2$O molecules [74, 75]. Ga$_2$O molecules emerge from the chemical reaction of Ga adatoms and O atoms of the SiO$_x$ layer as described in Chapter 2.3.3. Both the variation of the number density of Ga droplets and the sticking coefficient of Ga adatoms (just by changing T_{a1}) imply a significant surface modification of the native-SiO$_x$ during substrate annealing in step-1.

Conventional AFM surface scans in tapping mode (using a Si tip with a radius of curvature of less than 10 nm) do not reveal any significant change of the surface morphology or surface roughness of the native-SiO$_x$ as a function of T_{a1}. Only conductive AFM measurements reveal local roughening of the SiO$_x$ surface at higher T_{a1} as indicated in Fig. 4.6.

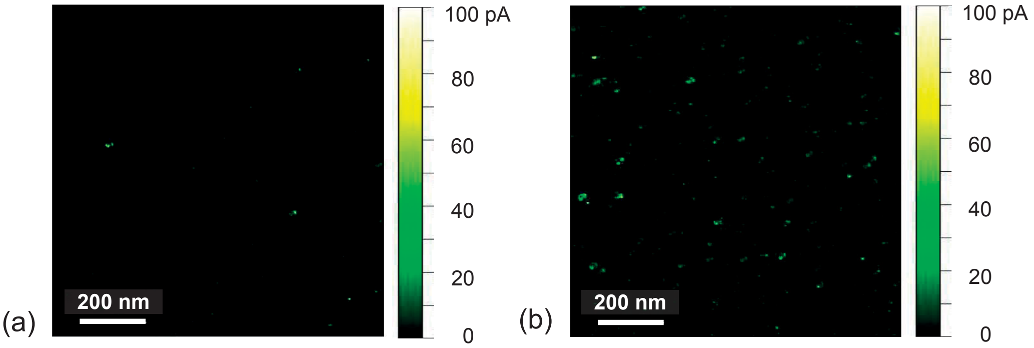

Fig. 4.6: 1×1 μm^2 conductive AFM images of native-SiO$_x$/Si(111) substrates after thermal annealing of the substrate in SMP step-1 at (a) T_{a1}=690 °C, and (b) T_{a1}=770 °C. Si(111) substrates with a 1.5 nm thin native-SiO$_x$ were employed. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

As illustrated, small spots at random positions are found on the SiO$_x$ surface, in which the tunnel current through the native-SiO$_x$ barrier is higher. This finding clearly depicts a morphological roughening of the SiO$_x$ surface during step-1. It is well-known that ultrathin SiO$_x$ layers on Si substrates start to decompose at temperatures of ∼800 °C in UHV, which is initiated by void nucleation and, thus, surface roughening [215, 216, 217, 218].

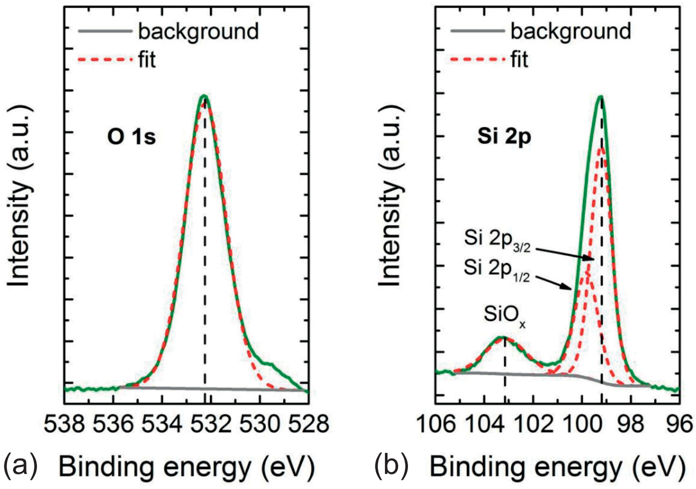

Fig. 4.7: (a) O 1s and (b) Si 2p peaks of a native-SiO$_x$/Si(111) substrate after thermal annealing of the substrate in SMP step-1 at T_{a1}=770 °C. A Si(111) substrate with a 1.5 nm thin native-SiO$_x$ was employed.

The compositional change of the native-SiO$_x$ at higher T_{a1} can be ruled out as a reason of a higher sticking of Ga on the substrate. This was verified by XPS measurements of a substrate after its thermal annealing in SMP step-1 at T_{a1}=770 °C. As shown in Fig. 4.7 (a), the binding energy of the O 1s peak after thermal annealing is constant at E_B=532.2 eV compared to the O 1s peak of the as-received substrates (Fig. 4.2 (d)). The binding energies of the metallic and oxidized Si components (Si 2p$_{3/2}$ at E_B=99.1 eV, Si 2p$_{1/2}$ at E_B=99.7 eV, SiO$_x$ at E_B=103.1 eV) shifted by ΔE_B=0.2 eV and ΔE_B=0.1 eV compared to the Si 2p peak of the as-received substrates (Fig. 4.2 (e)). Within the resolution limit of the measurements (step width of 0.2 eV), no significant change of the chemical composition of the native-SiO$_x$ was found after thermal annealing of the substrate at higher T_{a1}. Therefore, surface roughening in SMP step-1 must be the reason that affects the nucleation kinetics of Ga droplets on the SiO$_x$ surface at a given T_d in step-2.

4.2.2 Nucleation Kinetics of Ga Droplets in SMP step-2

The effect of SMP step-2 on the nucleation kinetics of Ga droplets on the SiO$_x$ surface has also been investigated. For this study, Si(111) substrates with a native-SiO$_x$ thickness of 1.9 nm (batch A) were employed. Six samples were prepared using always a fixed T_{a1} of 770 °C in SMP step-1, which resulted in numerous surface sites for the nucleation of Ga droplets (Fig. 4.5). Subsequently, Ga droplets were deposited in step-2 at various T_d in the range of 450 to 590 °C. Again, the SMP was interrupted after step-2, and the droplets were analyzed by AFM and SEM. Figure 4.8 shows the complete analysis of the Ga droplets as a function of T_d in SMP step-2.

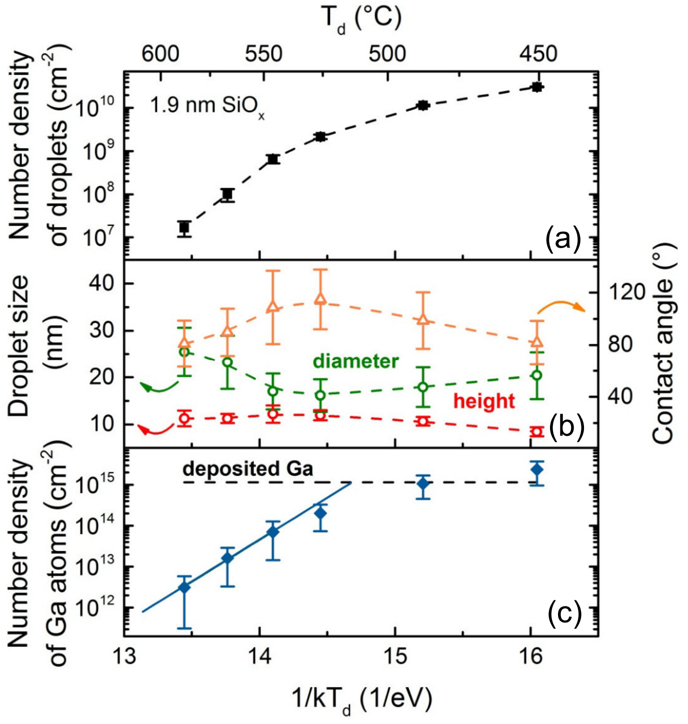

Fig. 4.8: Impact of T_d in SMP step-2 on the formation of Ga droplets on native-SiO$_x$/Si(111) substrates in step-2 (T_{a1}=770 °C in step-1). Analysis of (a) the number density of Ga droplets, (b) the droplet height, diameter, and contact angle, and (c) the number density of Ga atoms on the substrate. The dashed line in (c) indicates the total amount of deposited Ga. Si(111) substrates with a 1.9 nm thin native-SiO$_x$ were used. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

As can be seen in Fig. 4.8 (a), the number density of Ga droplets decreased by three orders of magnitude from 3×10^{10} cm^{-2} to 2×10^{7} cm^{-2} with increasing T_d from 450 °C to 590 °C. Figures 4.9 (a)-(c) show three representative AFM surface scans of the native-SiO$_x$/Si(111) substrates with a different number of Ga droplets per surface area deposited at different T_d. This result is attributed to an increased surface diffusivity of Ga adatoms at higher T_d [67, 71, 219]. As depicted in Fig. 4.8 (b), the Ga droplets possess mean diameters in the range of d_c=$2r_c$=16-25 nm and mean heights in the range of h_c=8-12 nm. This implies that the droplet size is almost independent across the entire range of T_d. Both the droplet diameters and the droplet heights exhibit a Gaussian distribution as illustrated for a representative sample (T_d=490 °C) in the histogram of Fig. 4.9 (d). The mean contact angles of the droplets are deduced to be in the range of θ=80-115°. Like in the previous analysis, the total number of Ga atoms in the droplets per surface area is plotted as a function of T_d in Fig. 4.8 (c). For $T_d < 500$ °C, the entire amount of supplied Ga sticks to the substrate surface, whereas the sticking coefficient decreases for higher T_d. Interestingly, Kumar *et al.* reported an onset of Ga$_2$O loss from the substrate surface at $T_d \approx 520$ °C [74]. Despite the good agreement with the observed behavior in Fig. 4.8 (c), the desorption also of Ga adatoms from the surface cannot be ruled out.

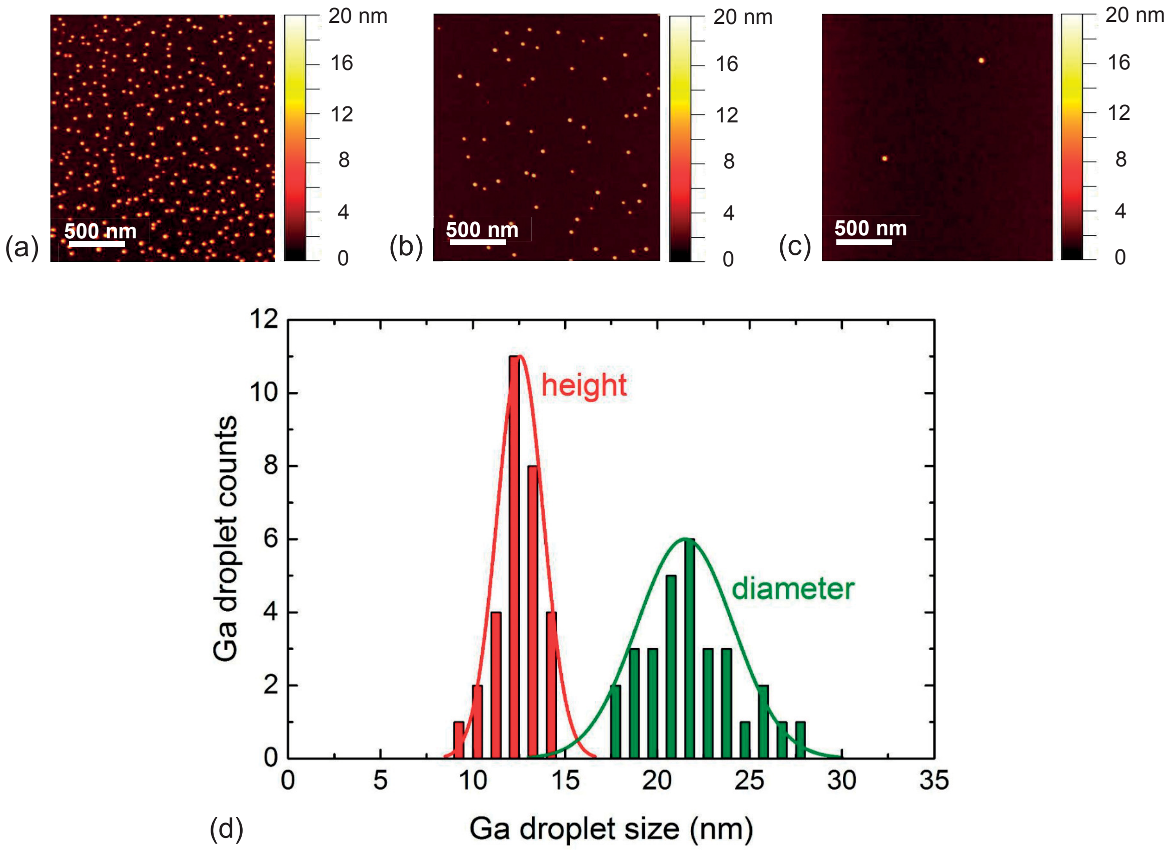

Fig. 4.9: 2×2 μm^2 AFM images of native-SiO$_x$/Si(111) substrates with Ga droplets deposited in SMP step-2 at (a) T_d=490 °C, (b) T_d=530 °C, and (c) T_d=590 °C (T_{a1}=770 °C in step-1). (d) Representative distribution of the corrected diameter d_c and height h_c of the Ga droplets shown in (a). Si(111) substrates with a 1.9 nm thin native-SiO$_x$ were employed. Figs. 4.9 (a)-(c) are adapted with permission from [47]. Copyright (2017) American Chemical Society.

Summarizing, both T_{a1} in SMP step-1 and T_d in SMP step-2 strongly influence the nucleation kinetics of Ga droplets on the native-SiO$_x$. The number density of Ga droplets can be varied deliberately within three orders of magnitude by changing T_{a1} in step-1 (i.e. 10^6-10^9 cm^{-2}) or T_d in step-2 (i.e. 10^7-10^{10} cm^{-2}). The difference in the ranges of the droplet densities of both sample series is attributed to the use of different substrate batches A and B with different mean thicknesses of the native-SiO$_x$ (i.e. 1.9 and 1.5 nm). In particular, the thicker SiO$_x$ yields a lower number density of Ga droplets of 1×10^8 cm^{-2} for T_{a1}=770 °C and T_d=570 °C, whereas the thinner SiO$_x$ produces a higher number density of Ga droplets of 6×10^8 cm^{-2} for the same T_{a1} and T_d. This is a reasonable result because an increased surface roughening in SMP step-1 is expected for the thinner SiO$_x$ layer.

4.2.3 Formation of Openings in the SiO$_x$ in SMP step-3

Finally, the full SMP was performed on Si(111) substrates from batch B with a native-SiO$_x$ thickness of 1.5 nm. Subsequent to the formation of Ga droplets in SMP step-2, a second thermal annealing of the substrate (SMP step-3) was carried out at T_{a2} (T_{a2} > T_d). In order to unravel the underlying physical processes that take place during SMP step-3, three samples were prepared using the same SMP parameters in step-1 (T_{a1}=770 °C) and step-2 (T_d=570 °C). Figures 4.10 (a)-(d) show the impact of SMP step-3 on the modification of the substrate surface.

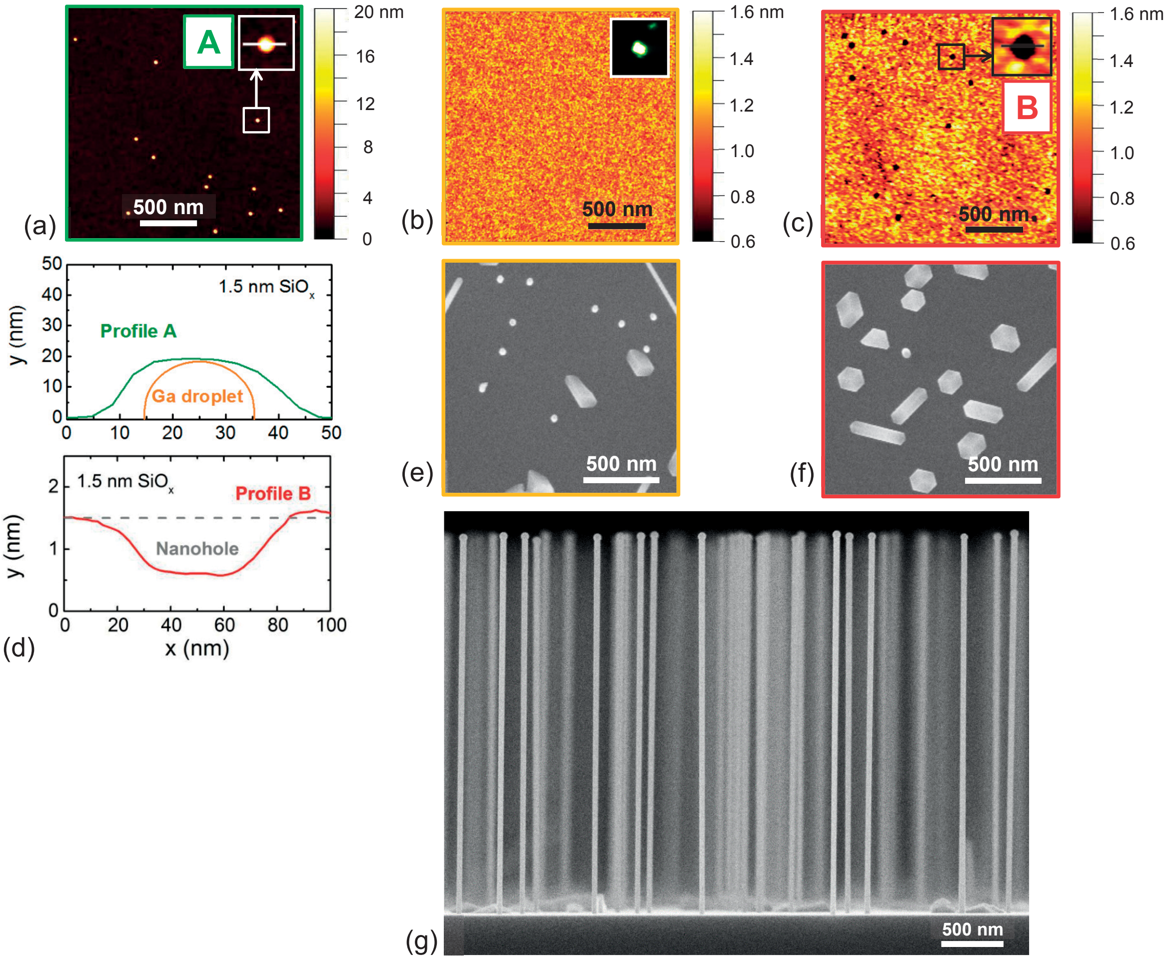

Fig. 4.10: Impact of t_{a2} in SMP step-3 on the size of SiO$_x$ holes and GaAs nucleation. Si(111) substrates with a 1.5 nm thin native-SiO$_x$ were used. (a) 2×2 μm^2 AFM image of the substrate surface after step-2 at T_d=570 °C (T_{a1}=770 °C). (b) 2×2 μm^2 AFM image of the substrate surface after performance of SMP step-3 at T_{a2}=760 °C for t_{a2}=5 min. The 15×15 nm^2 inset shows a conductive AFM image of a nanohole of the same sample. (c) 2×2 μm^2 AFM image of the substrate surface after performance of SMP step-3 at T_{a2}=760 °C for t_{a2}=20 min. The 100×100 nm^2 inset shows a close-up of a SiO$_x$ hole of the same sample. (d) Plot of a AFM line profile of a Ga droplet from (a) denoted as Profile A, and of a SiO$_x$ hole from (c) denoted as Profile B. (e) Plan-view and (g) side-view SEM image of GaAs structures grown on a substrate similar to (b). (f) Plan-view SEM image of GaAs structures grown on a substrate similar to (c). Adapted with permission from [47]. Copyright (2017) American Chemical Society.

Figure 4.10 (a) illustrates an AFM image of the native-SiO$_x$/Si(111) substrate with Ga droplets after performance of step-2. A representative AFM profile (denoted as profile A) through the center of a Ga droplet can be seen in the upper panel of Fig. 4.10 (d), where the measured profile is depicted in green color and the real droplet shape (extracted from the geometrical model presented in Chapter 4.2.1) is illustrated in orange color. After performance of SMP step-3 for 5 min at T_{a2}=760 °C, the Ga droplets were evaporated completely from the substrate surface as can be seen in Fig. 4.10 (b). Although no evidence of nano-sized holes in SiO$_x$ was found when conventional AFM in tapping mode was employed, small nanoholes of a size of ~5 nm were detected using conductive AFM as shown in the inset of Fig. 4.10 (b). Additionally, the number density of the SiO_x holes was found equal to the number density of Ga droplets after SMP step-2 (Fig. 4.10 (a)). Prolongation of the thermal annealing of the substrate in SMP step-3 from 5 to 20 min did not change the number density of SiO_x holes, but increased their size as evidenced from Fig. 4.10 (c). The diameter of the SiO_x holes was found approximately equal to 60 nm as indicated by profile B in the lower panel of Fig. 4.10 (d). It is important to note that it was not possible to detect any residual oxide at the bottom of the SiO_x holes by *ex situ* conductive AFM due to the small hole size compared to the tip radius and the fast oxidation of the exposed Si substrate inside the openings in atmosphere.

4.3 Effect of the SMP on the GaAs Nucleation

After detailed investigation of the physical mechanisms that take place during the SMP on native-SiO_x/Si(111) substrates, the advantages of the SMP in the self-catalyzed growth of GaAs nanowires on Si are elaborated. For this purpose, nucleation and growth of GaAs was always performed subsequent to the SMP at a substrate temperature T_{gr}=615 °C using fixed common growth conditions, i.e. a Ga flux of F_{Ga}=0.16 ML/s and an As_4 flux of F_{As_4}=1.8 ML/s (V/III flux ratio of 11). First, the As_4 shutter was opened to stabilize the As_4 flux for 10 min inside the growth chamber. Subsequently, growth was initiated by opening the Ga shutter. The background pressure during growth was 10^{-7} Torr. Finally, the growth was terminated after 15 min by interrupting the Ga and As_4 beams simultaneously, and by cooling down the substrate to 400 °C with a rate of 50 °C/min. The SMP provides an unprecedented level of control in the nucleation stage of GaAs nanowires on Si, which leads to growth of exceptionally uniform GaAs nanowire ensembles with high crystal quality and tunable number density and dimensions as will be demonstrated in the following sections.

4.3.1 Effect of the Size of SiO_x Openings on the GaAs Nucleation

First, the effect of the size of SiO_x holes on the nucleation and growth of GaAs is studied. For this purpose, growth of GaAs was performed on Si(111) substrates with previously created SiO_x holes of a size of ∼5 and ∼60 nm respectively (substrate treatment equal to Figs. 4.10 (b) and (c)). The corresponding plan-view SEM micrographs of the samples subsequent to growth of GaAs inside the SiO_x holes of different size are shown in Figs. 4.10 (e) and (f). As a result, it was found (i) that the number density of overall GaAs structures (including vertical and inclined GaAs nanowires as well as faceted GaAs islands) equals the number density of SiO_x holes, which clearly reveals that the droplet-induced openings accommodate all and every type of GaAs structures. This is deduced here for a certain number density of Ga droplets. The effect of the number density of Ga droplets on the number density of GaAs structures is discussed in section 4.3.2. (ii) The number yield of vertical GaAs nanowires, which is the ratio of the number densities of vertical GaAs nanowires and all GaAs structures (see Chapter 3.2.1 for details), depends on the size of the openings. All these findings are evidenced from comparison of Figs. 4.10 (b) and (e), and (c) and (f). Nanoholes with a diameter of 5 nm accommodate vertical GaAs nanowires with a number yield of ∼50%, but also inclined GaAs nanowires and faceted GaAs islands (parasitic growth) were grown as indicated in Fig. 4.10 (e). On the contrary, growth of GaAs inside ∼60 nm SiO$_x$ holes resulted mainly in faceted islands, and only a low number of vertical GaAs nanowires (number yield of ∼5%) was found on the substrate surface (Fig. 4.10 (f)). Unlike the VLS growth of nanowires, the growth of faceted GaAs islands takes place in the (droplet-free) vapor-solid selective area growth mode as discussed in Refs. [220, 221, 222]. A representative side-view SEM image of GaAs nanowires with a mean length of 2.910 ± 0.024 μm is shown in Fig. 4.10 (g). As indicated, a remarkable length uniformity, and thus, an exceptionally narrow distribution of nanowire lengths (standard deviation of less than 1%) was found, which is attributed to a highly synchronized nucleation of all nanowires inside the SiO$_x$ openings. This is discussed in detail in section 4.3.4.

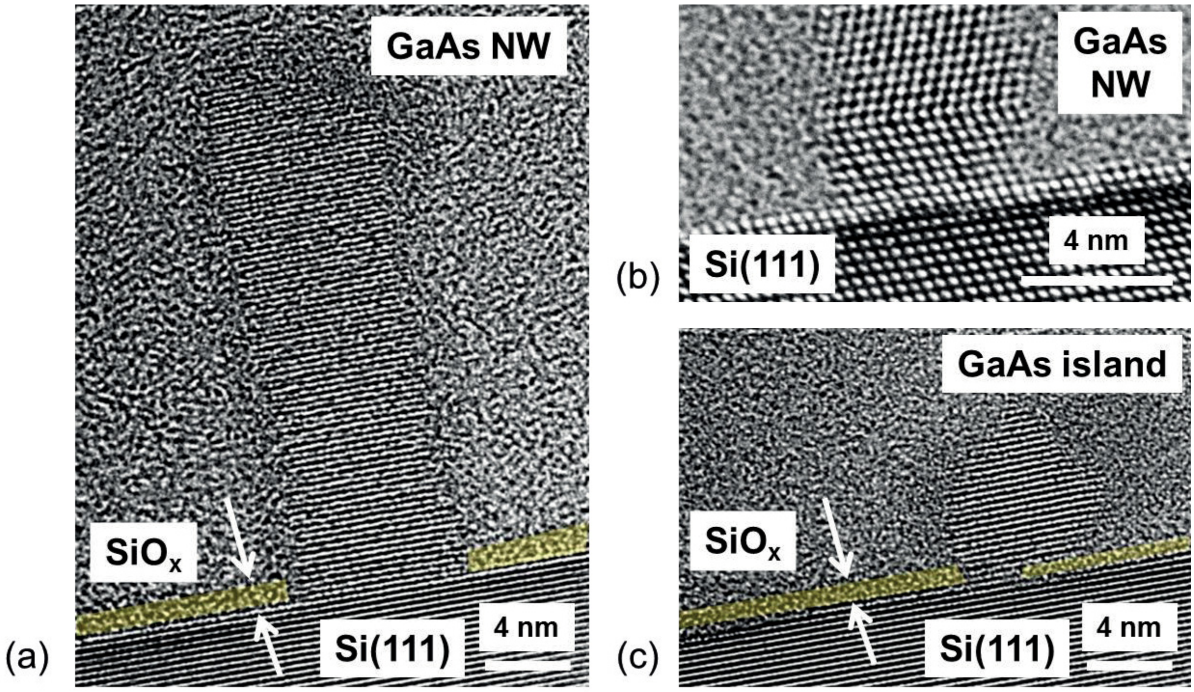

Fig. 4.11: Cross-sectional high-resolution TEM images of the GaAs/Si substrate interface of (a) a vertical GaAs nanowire (off-axis image), (b) another vertical GaAs nanowire (on-axis image), and (c) a GaAs island (off-axis image). The incident electron beam is not exactly aligned with the $[1\bar{1}0]$ zone axis in the off-axis images. These particular imaging conditions ensure a better visibility of the 1.5 nm thin native-SiO$_x$ layer, which is highlighted in yellow color (not the case for the on-axis image). Adapted with permission from [47]. Copyright (2017) American Chemical Society.

To further investigate how the size of SiO$_x$ holes affects the GaAs nucleation, cross-sectional high-resolution TEM analysis at the GaAs/Si interface has been carried out. For this purpose, a GaAs nanowire sample was prepared using exactly the same SMP parameters as employed for the sample shown in Fig. 4.10 (e), but the growth lasted only for 10 s (instead of 15 min). TEM samples were fabricated from selected positions of the as-grown nanowire sample by cutting TEM lamellae using Ga FIB. Figures 4.11 (a) and (b) depict the GaAs/Si substrate interface of a vertical GaAs nanowire and of a parasitic GaAs island, respectively. Both GaAs structures existed in the same TEM sample. As can be seen, the width of the nanowire/substrate interface and thus, the diameter of the SiO$_x$ holes was in the range of ~5-8 nm, which confirms the optimal size of the SiO$_x$ openings measured by conductive AFM (see inset of Fig. 4.10 (b)). As expected for such small diameters [38, 45], the on-axis image in Fig. 4.11 (b) shows that the GaAs nanowires grew free of misfit dislocations inside the SiO$_x$ openings. On the contrary, smaller holes in the native SiO$_x$ in the range of 2-3 nm accommodated GaAs islands rather than vertical GaAs nanowires as illustrated in Fig. 4.11 (c). Thus, it is unlikely to achieve a number yield of vertical GaAs nanowires of 100%, since the openings in the SiO$_x$ do not have identical sizes, but a rather broad distribution across the substrate surface. Therefore, all GaAs islands that grew next to the vertical GaAs nanowires in Fig. 4.10 (e) are attributed to smaller holes with a diameter of ~2 nm. These holes are located under one edge of the islands as shown for instance in Fig. 4.11 (c). Based on the study by Matteini *et al.* [70], it is speculated that the GaAs islands nucleated in the droplet-assisted VLS growth via asymmetric wetting of the Ga droplets with larger size compared to the hole size at the top of the openings.

After all, the size of the SiO$_x$ holes is an important parameter to control the number yield of vertical GaAs nanowires. In the sample series in Fig. 4.10, the size of the SiO$_x$ holes was tuned by varying t_{a2} at constant T_{a2} in SMP step-3. Alternatively, it is also possible to tune the size of the openings by varying T_{a2} for a fixed t_{a2} [217]. For this purpose, a new sample series was produced using T_{a1}=750 °C, T_d=560 °C, 2.4 ML of Ga, and t_{a2}=5 min, whereas T_{a2} was varied from 695 °C to 780 °C.

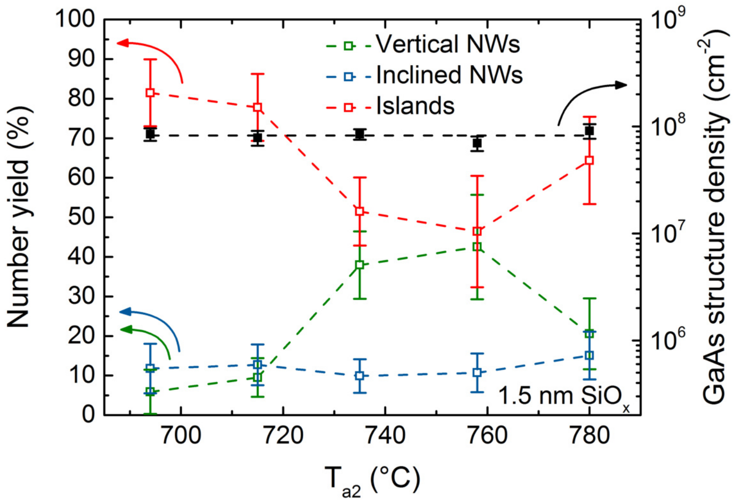

Fig. 4.12: Impact of T_{a2} in SMP step-3 (after step-1 and step-2 at T_{a1}=750 °C and T_d=560 °C) on the number yield of vertical GaAs nanowires, inclined GaAs nanowires and parasitic GaAs islands (left axis). Plot of the overall number density of GaAs structures as a function of T_{a2} (right axis). Si(111) substrates with a native-SiO$_x$ of a thickness of 1.5 nm were employed. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

Figure 4.12 clearly demonstrates the resulting dependence of the number yield of vertical GaAs nanowires on T_{a2}. The overall number density of GaAs structures at $\sim 9\times10^7$ cm^{-2} is independent of T_{a2} (it exclusively depends on T_d as will be discussed in the next section). According to

Fig. 4.12, only a narrow range of T_{a2} exists (i.e. 730 °C $< T_{a2} <$ 760 °C), in which the number density of vertical GaAs nanowires has increased (up to 43%). This result is attributed again to an optimal size of SiO$_x$ holes, which favors the growth of vertical GaAs nanowires rather than parasitic GaAs islands. On the contrary, for $T_{a2} <$ 730 °C, the number yield of vertical GaAs nanowires dropped below 10%, and the number yield of parasitic GaAs islands increased up to ~80% correspondingly, which is associated with too small holes in the SiO$_x$ with respect to the size of the Ga droplets in the nucleation phase, like in Fig. 4.11 (c). On the other hand, for $T_{a2} >$ 760 °C, the SiO$_x$ holes grew too large and favored again the nucleation of parasitic GaAs islands (number yield of 64%) similar to Fig. 4.10 (f). Besides, the number yield of inclined GaAs nanowires is always constant at ~12%, and thus, independent of T_{a2}.

It is important to note that all steps of the SMP are essential in order to prepare the native-SiO$_x$/Si(111) substrates for subsequent nanowire growth. If step-2 of the SMP is omitted, and only step-1 and step-3 are performed (i.e. at T_{a1}=770 °C and T_{a2}=760 °C), the nucleation and growth of GaAs nanowires hardly takes place and only a few GaAs structures (nanowires and islands) with an overall number density smaller than 1×10^6 cm^{-2} were found on the substrate as illustrated in Fig. 4.13 (a).

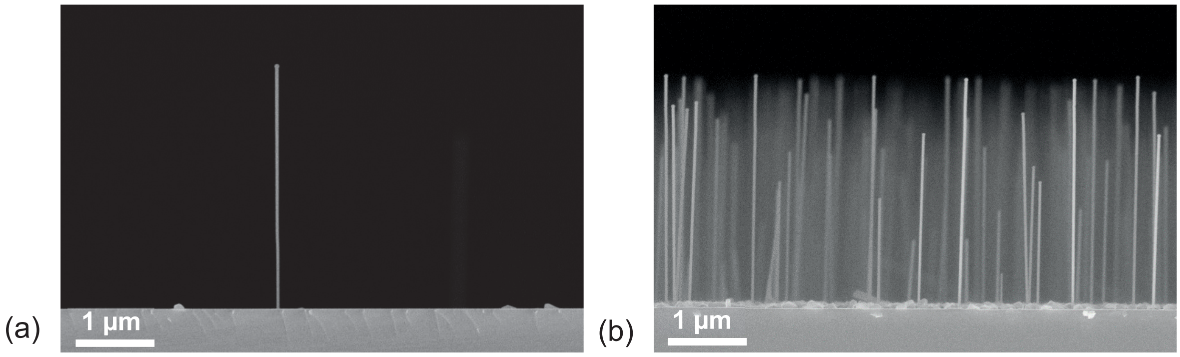

Fig. 4.13: Side-view SEM images of GaAs nanowires grown on native-SiO$_x$/Si(111) substrates after (a) omission of SMP step-2 (T_{a1}=770 °C in step-1 and T_{a2}=760 °C in step-3), and (b) omission of SMP step-3 (T_{a1}=770 °C in step-1 and T_d=490 °C in step-2). Si(111) substrates with a native-SiO$_x$ of a thickness of 1.9 nm were used. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

This is because an exceptionally low number of SiO$_x$ holes is initially present in the native-SiO$_x$ layer, and does not increase after SMP step-1 and step-3. If step-3 of the SMP is omitted, and only step-1 and step-2 are performed (i.e. at T_{a1}=770 °C and T_d=490 °C), GaAs nanowires and islands with an overall number density equal to the number density of Ga droplets in step-2 were obtained. However, the nanowires exhibit a broad spread in their lengths as shown in Fig. 4.13 (b) with a measured standard deviation of 20%. In addition, a low number yield of vertical GaAs nanowires of only 11% was achieved. At this point, it is speculated that both the broad length distribution and the low number yield of vertical GaAs nanowires are related to an inappropriate (too small) size of the openings in the native-SiO$_x$ when SMP step-3 is omitted.

In summary, all presented findings reveal (i) that the initial substrate annealing in step-1 roughens the SiO$_x$ surface, (ii) that the Ga droplets from step-2 modify the SiO$_x$ surface, and (iii) that these surface modifications evolve into nano-sized openings in the SiO$_x$ during step-3. Moreover, the results demonstrate (iv) that every Ga droplet creates one SiO$_x$ hole, where the nucleation of GaAs takes place, (v) that number yield of vertical GaAs nanowires against faceted islands depends on the size of SiO$_x$ holes, which can be controlled by the appropriate T_{a2}/t_{a2} combination in step-3, and (vi) that vertical GaAs nanowires can be successfully grown if all three SMP steps are performed, and if the SMP parameters, i.e. T_{a1}, T_{a2}, and t_{a2} are well-tuned.

4.3.2 Deliberate Control of the Number Density and the Dimensions of GaAs Nanowires

One of the results in section 4.3.1 was that all Ga-induced SiO$_x$ holes accommodate all and every type of GaAs structures. This result was deduced from the finding that the number density of overall GaAs structures equals the number density of Ga droplets from step-2 for a certain number density of $\sim5\times10^8$ cm^{-2} (Fig. 4.10). In this section, the dependence of the number density of all GaAs structures including vertical GaAs nanowires, inclined GaAs nanowires and parasitic GaAs islands on the number density of Ga droplets is discussed. For this purpose, a series of nanowire samples was grown using fixed SMP parameters (T_{a1}=770 °C, T_{a2}=760 °C, t_{a2}=5 min, 2.4 MLs of Ga) and growth conditions (T_{gr}=615 °C, V/III=11) except of T_d in SMP step-2, which was varied from 450 °C to 590 °C in order to produce various number densities of Ga droplets in the range from 3×10^{10} cm^{-2} to 2×10^7 cm^{-2} (Fig. 4.8 (a)).

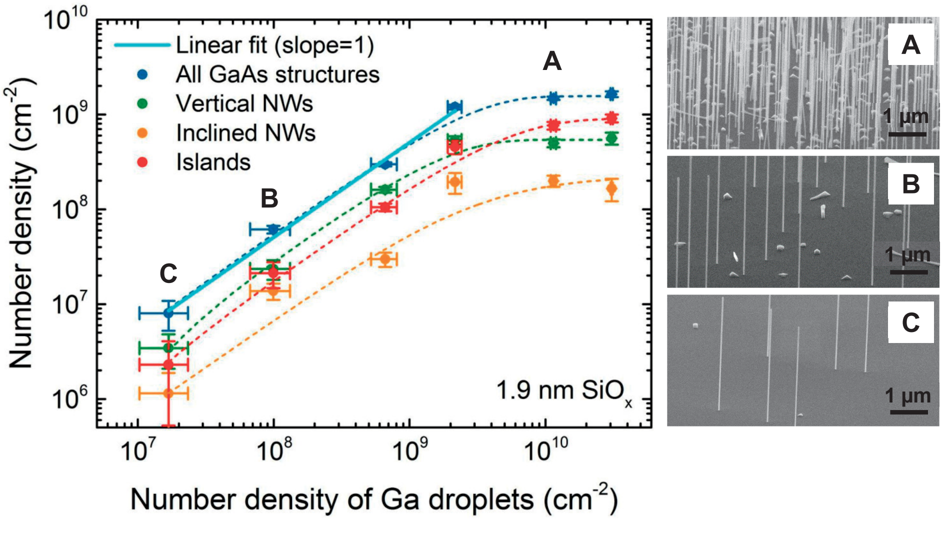

Fig. 4.14: Plot of the measured number density of overall GaAs structures, vertical GaAs nanowires, inclined GaAs nanowires, and parasitic GaAs islands in dependence of the number density of Ga droplets in SMP step-2. Corresponding tilt-view (65° from surface normal) SEM micrographs of samples A, B, and C are shown in the insets. Si(111) substrates with a native-SiO$_x$ of a thickness of 1.9 nm were used. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

In Figure 4.14, the resulting number density of all GaAs structures (nanowires and islands) is plotted as a function of the number density of Ga droplets in SMP step-2. Two regimes of the number density of GaAs structures can be identified. For number densities of Ga droplets smaller than 2×10^9 cm^{-2} ($T_d \geq 530$ °C), the number density of GaAs structures monotonically decreases from 1×10^9 cm^{-2} to 8×10^6 cm^{-2} with decreasing number density of Ga droplets from

$2{\times}10^9$ cm^{-2} to $2{\times}10^7$ cm^{-2}. Therefore, the number density of GaAs structures is equal to the number density of Ga droplets within a factor of ~2. In other words, the number density of GaAs structures is dictated by the number density of Ga droplets in SMP step-2. That means that all and every type of GaAs structures nucleated inside the SiO$_x$ holes at the same positions of the Ga droplets from SMP step-2 and only there. Moreover, each single contribution (nanowires and islands) to the overall number density of GaAs structures follows the same trend in this regime and is directly proportional to the number density of Ga droplets. Most importantly, the number density of vertical GaAs nanowires can be varied deliberately within three orders of magnitude by selecting T_d in SMP step-2 accordingly, in particular from $3{\times}10^6$ cm^{-2} for T_d=590 °C to $6{\times}10^8$ cm^{-2} for T_d=530 °C. Three representative examples denoted by A, B, and C are shown in the insets of Fig. 4.14. For number densities of Ga droplets larger than $2{\times}10^9$ cm^{-2} ($T_d <$ 530 °C), the number density of GaAs structures remained constant at $2{\times}10^9$ cm^{-2}, and thus is independent of T_d. This finding can be attributed to the surface diffusion length of Ga adatoms, which is larger than the mean distance (approximately 300 nm) between neighboring SiO$_x$ openings. In this range of number densities of Ga droplets, the number density of parasitic GaAs islands is larger than that of vertical GaAs nanowires. This finding implies a weak dependence of the number yield of vertical GaAs nanowires on their number density. This may be related to a larger number of SiO$_x$ holes with non-optimal (too small) size for number densities of Ga droplets larger than $2{\times}10^9$ cm^{-2}.

Figure 4.15 shows the dependence of the average lengths and diameters of GaAs nanowires on their number density (samples with $T_d \geq 530$ °C in Fig. 4.14). As indicated, both, the average length and diameter of the nanowires increased from 2.75 to 3.07 μm and from 43 to 52 nm, respectively, with decreasing nanowire number density from $5{\times}10^8$ cm^{-2} to $3{\times}10^6$ cm^{-2}.

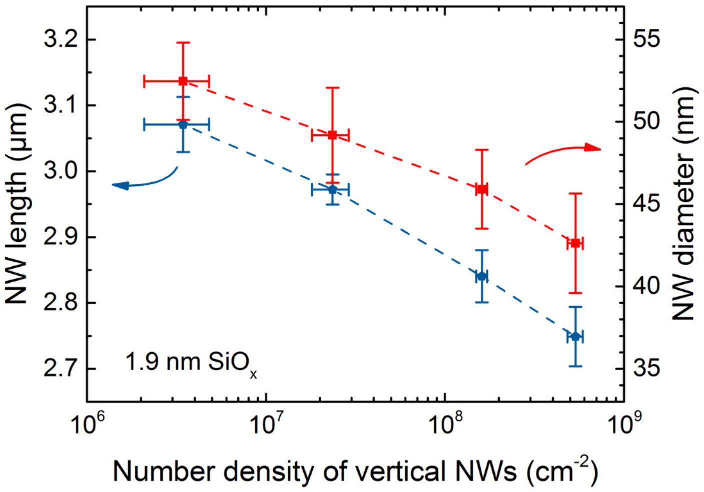

Fig. 4.15: Plot of the nanowire length (left axis) and nanowire diameter (right axis) as a function of the number density of vertical GaAs nanowires. Si(111) substrates with a native-SiO$_x$ of a thickness of 1.9 nm were used. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

The mean length of the nanowires produced within a fixed growth duration (corresponds to the axial growth rate GR_{ax}) is determined by the total flux of As$_4$ at the Ga droplet that contains both the direct and the rebound fluxes. The latter is the secondary beam flux of As$_4$ that feeds the Ga droplets at the nanowire tips after re-emission from the substrate and sidewalls of adjacent nanowires [76, 80]. The increase of the mean length of the nanowires with decreasing nanowire number density is attributed to a higher GR_{ax} as a result of an enhanced rebound As$_4$ flux due to reduced shadowing for low nanowire number densities [223]. The increase of the mean diameter of the nanowires with decreasing nanowire number density is attributed to the increased arrival rate of diffusing Ga adatoms from the substrate onto each droplet. Both, the length and diameter dependencies on the nanowire number density, are in agreement with findings reported for nanowire growth on pre-patterned thermally grown SiO$_2$/Si(111) substrates, where different hole pitches have been realized to cover a wide range of nanowire number densities [223].

The strength of the SMP is further highlighted by the possibility to control the diameter of the nanowires independent of their number density without *ex situ* substrate patterning of hole arrays with various number density and size. This was achieved by varying the V/III ratio (i.e. the Ga flux) intentionally before initiation of nanowire growth for a fixed nanowire number density. This is in contrast to the previous section (i.e. Fig. 4.15), which was subject to the study of the correlation of the diameter of the nanowires for various number densities at an identical Ga flux. For this purpose, a series of GaAs nanowire samples was grown for 10 min at T_{gr}=615 °C on native-SiO$_x$/Si(111) substrates subsequent to the SMP (T_{a1}=790 °C, T_d=580 °C, T_{a2}=770 °C). For nanowire growth, a fixed As$_4$ flux of F_{As_4}=1.8 ML/s and Ga fluxes F_{Ga} in the range from 0.16 to 0.11 ML/s were employed.

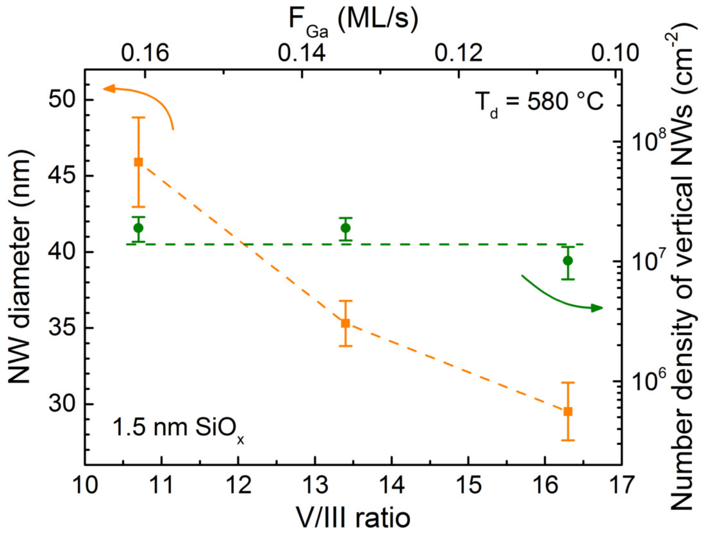

Fig. 4.16: Plot of the measured diameter (left axis) and number density (right axis) of vertical GaAs nanowires as a function of the V/III ratio (bottom axis) and the Ga flux respectively (top axis). Si(111) substrates with a native-SiO$_x$ of a thickness of 1.5 nm were used. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

The decrease of the Ga flux for a constant As$_4$ flux resulted in an increasing V/III ratio in the range from 11 to 16. The measured average diameters and number densities of the nanowires are plotted as a function of the V/III ratio and Ga flux F_{Ga} in Fig. 4.16. As indicated, the diameter of ~1.8 μm long nanowires (length that corresponds to t_{gr}=10 min) decreased from 46 to 30 nm with increasing V/III ratio from 11 to 16 independent of the number density of the nanowires, which remained constant at ∼2×10^7 cm^{-2}. This is because the nanowire nucleation takes place below Ga droplets of smaller size inside SiO$_x$ holes of similar number density and size, when a lower Ga flux (larger V/III ratio) is employed for growth. In other words, the nanowire dimensions (i.e. diameter and length) can be controlled by changing the growth conditions (i.e. Ga flux and t_{gr}), whereas the number density of the nanowires is exclusively controlled by the SMP parameters without the need of costly and time-consuming *ex situ* substrate patterning. Such a high level of growth control, in particular deliberate and independent control of all growth-related nanowire properties, has not yet been realized in the self-catalyzed growth of GaAs nanowires on native-SiO$_x$/Si(111) substrates.

4.3.3 High Growth Reproducibility

Finally, the capability of the SMP with respect to reproducibility of nanowire growth was tested. Growth reproducibility strongly depends on the properties of the native-SiO$_x$ layer that may differ when various substrate batches are used. Typically, serious problems exist in reproducing the same growth results on different native-SiO$_x$/Si substrates. In the following paragraph, the reproducibility of the number density and number yield of GaAs nanowires is investigated for two different native-SiO$_x$/Si(111) substrate batches. SE measurements revealed that only the thickness of the native-SiO$_x$ layer has changed from 1.9 nm (± 2%) in batch A to 1.5 nm (± 1.5%) in batch B. No compositional or morphological changes of the substrates of these two batches were detected by XPS and AFM. GaAs nanowires were grown on Si(111) substrates of batch A and B using the common growth conditions, but different SMP parameters (i.e. T_{a1}=770 °C and T_{a2}=760 °C for batch A, and T_{a1}=750 °C and T_{a2}=735 °C for batch B).

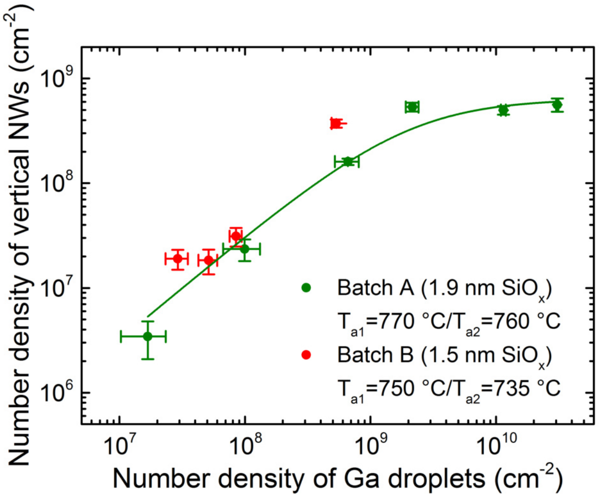

Fig. 4.17: Plot of the number density of vertical GaAs nanowires as a function of the number density of Ga droplets. GaAs nanowires were grown on native-SiO$_x$/Si(111) substrates with a SiO$_x$ thickness of 1.9 nm (batch A) and 1.5 nm (batch B) respectively after step-1 and step-3 at T_{a1}=770 °C and T_{a2}=760 °C (batch A), and T_{a1}=750 °C and T_{a2}=735 °C (batch B). Adapted with permission from [47]. Copyright (2017) American Chemical Society.

Figure 4.17 shows the plot of the number density of vertical GaAs nanowires as a function of the number density of Ga droplets from step-2 for both SiO$_x$ thicknesses. As indicated, it was possible to reproduce the dependence of the number density of vertical GaAs nanowires on the number density of Ga droplets of batch A with substrates of batch B. This was achieved either by fine-tuning of T_d in step-2 at fixed T_{a1} and T_{a2} (not shown for batch B, but demonstrated in Fig. 4.14 for batch A), or by reducing T_{a1} in step-1 and T_{a2} in step-3 as shown in Fig. 4.17. In particular, T_{a1}=750 °C and T_{a2}=735 °C are used for batch B in order to obtain similar number densities of vertical GaAs nanowires on substrates of batch B as compared to batch A. This is attributed to the dependence of the growth rate of voids in ultra-thin SiO$_x$ layers on the SiO$_x$ thickness and annealing temperature [217]. Following Ref. [217], it is assumed that a larger number of SiO$_x$ openings is produced (i) in thinner SiO$_x$ layers at fixed annealing temperatures T_{a1}/T_{a2}, or (ii) at higher annealing temperatures T_{a1}/T_{a2} at the same SiO$_x$ thickness. Consequently, a similar number density of SiO$_x$ openings is obtained in the thinner SiO$_x$ layer of batch B by lowering T_{a1} and T_{a2} as compared to the thicker SiO$_x$ layer of batch A.

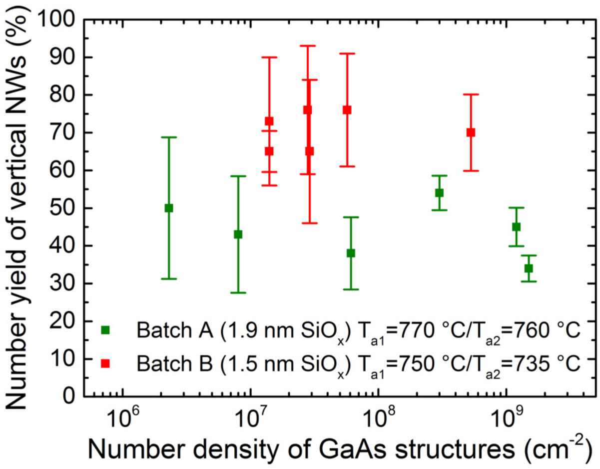

Fig. 4.18: Plot of the number yield of vertical GaAs nanowires as a function of the number density of GaAs structures. GaAs nanowires were grown on native-SiO$_x$/Si(111) substrates with a SiO$_x$ thickness of 1.9 nm (batch A) and 1.5 nm (batch B) respectively after step-1 and step-3 at T_{a1}=770 °C and T_{a2}=760 °C (batch A), and T_{a1}=750 °C and T_{a2}=735 °C (batch B). Adapted with permission from [47]. Copyright (2017) American Chemical Society.

In Figure 4.18, the number yield of vertical GaAs nanowires is plotted against the total number density of GaAs structures, again for both SiO$_x$ thicknesses. As can be seen in Fig. 4.18, the number yield of vertical GaAs nanowires is independent of their number density (or T_d), and similar yield values of ~50% for batch A and ~80% for batch B were realized over a wide range of number densities of GaAs structures. This is attributed to formation of SiO$_x$ holes of constant size on substrates of identical SiO$_x$ thickness (fixed T_{a1}/T_{a2} within each substrate batch). The lower number yield of vertical GaAs nanowires in batch A is related to non-optimal (too small) openings in the (thicker) SiO$_x$ layer as compared to batch B. It is assumed that the number yield of vertical GaAs nanowires may increase for batch A after optimizing the size of the SiO$_x$ openings. At this point it is speculated that most likely a higher T_{a2} and/or a longer t_{a2} are necessary in order to obtain the same size of SiO$_x$ holes on substrates of batch A as compared to batch B.

In summary, the number density of vertical GaAs nanowires can be simply reproduced on native-SiO$_x$/Si(111) substrates with different SiO$_x$ thickness by variation of T_d in SMP step-2 (at fixed T_{a1}/T_{a2}), or by fine-tuning of T_{a1} and T_{a2} (and T_d) in SMP steps 1 to 3. In contrast, the number yield of vertical GaAs nanowires depends only on the fine-tuning of the appropriate T_{a1}/T_{a2} (and t_{a2}) combination, but not on T_d. Although the number yield of vertical GaAs nanowires could not be reproduced on these two substrate batches, these original results demonstrate a high growth reproducibility of self-catalyzed GaAs nanowires on native-SiO$_x$/Si(111) substrates of various SiO$_x$ thicknesses.

4.3.4 Sub-Poissonian Length Distributions in GaAs Nanowire Ensembles

The achievement of a sub-Poissonian LD in VLS-grown III-V nanowire ensembles has been theoretically predicted by Glas and Dubrovskii in 2017 [93, 94]. It is attributed to the so-called nucleation antibunching [84, 93, 94, 95, 96], which is the temporal anti-correlation of discrete nucleation events at the droplet/nanowire interface owing to periodic droplet depletion and re-filling with As as outlined in detail in Chapter 2.4.1. Nucleation antibunching leads to self-narrowing of the LD in VLS-grown III-V nanowire ensembles [93, 94, 96], when broadening effects are absent or eliminated.

In practice, the achievement of a sub-Poissonian LD in self-catalyzed GaAs nanowire ensembles on Si substrates is very difficult. This is related to the thin native-SiO$_x$ layer, that is present even inside the openings of thermally grown and patterned SiO$_2$ layers on Si substrates [111, 205]. As a result, the nanowires typically suffer from a non-synchronized (delayed) nucleation on their substrate because multiple mechanisms take place simultaneously as already discussed (formation of Ga droplets, formation of openings in the SiO$_x$, and nucleation of GaAs nanowires inside those openings). Non-synchronized nanowire nucleation leads to broadening of their LD with a pronounced asymmetry towards shorter nanowire lengths. Elimination of asymmetric broadening (nucleation delay) and, thus, synchronization of nanowire nucleation requires (i) the formation of SiO$_x$ openings free of any residual oxide at the bottom of the openings, which can be only achieved by *in situ* preparation of the substrate, and (ii) the formation of uniform Ga droplets inside the openings. Furthermore, kinetic fluctuations, i.e. any temporal or spatial variations of the growth conditions, cannot be ruled out as an additional LD broadening factor. In other words, the same arrival rates of Ga and As at the Ga droplets and the same substrate temperature are required for every nanowire in the ensemble to avoid symmetric broadening of the nanowire LD by kinetic fluctuations.

The achievement of a sub-Poissonian LD of self-catalyzed GaAs nanowire ensembles on Si(111) substrates has been reported for the first time by Koivusalo *et al.* in 2017 [103]. Clearly, the measured variance of the LD of ∼600 nm^2 was much smaller compared to the Poissonian variance of ∼1000 nm^2 for a mean nanowire length of ∼3250 nm [103]. The sub-Poissonian narrowing of the LD was attributed to the nucleation antibunching as the dominant mechanism after minimization of nucleation delay (and thus synchronized nucleation) of the nanowires inside the SiO$_x$ openings [103]. The preparation of the SiO$_x$ openings was based on a complicated sequence of *in situ* and *ex situ* steps prior to nanowire nucleation and growth (i.e. *in situ* growth of GaAs islands on bare Si(111) substrate by droplet epitaxy, *ex situ* oxidation of the islands and the substrate surface, *in situ* removal of the oxidized islands by substrate annealing, and finally another *in situ* Ga deposition and evaporation step) [109, 212, 103].

In the following, it is demonstrated that the *in situ* SMP can be used to routinely achieve synchronized nanowire nucleation and thus, sub-Poissonian LDs, in self-catalyzed GaAs nanowire ensembles, without any *ex situ* process. Due to the unique control of the number density and size of SiO$_x$ openings, that SMP offers, it was possible to study (i) the impact of the number density of GaAs nanowires on their LD, and (ii) the effect of the size of the SiO$_x$ openings on the LD of GaAs nanowires. This chapter presents results that were obtained **in collaboration with Vladimir G. Dubrovskii and Yury Berdnikov** from ITMO University, St. Petersburg/Russia, who contributed to this work by developing a theoretical model in order to study LDs in GaAs nanowire ensembles. The model is presented in the following section.

For these studies, different GaAs nanowire samples were prepared. The lengths of more than 130 nanowires of each sample were analyzed by SEM and plotted in histograms. Then, the LD shapes were fitted with Eq. 4.8

$$f(s) = \frac{\alpha}{2} e^{\alpha(s-\tau)+\frac{\alpha^2 D}{2}} erfc[\frac{(s-\tau)+\alpha D}{\sqrt{2D}}], \tag{4.8}$$

which was obtained by replacing the Poissonian variance $\sigma_P^2 = \tau$ in Eq. 2.19 with $\tau = D$. Equal to Chapter 2.4.2, $s = L_{NW}/h_{GaAs}$ is the nanowire length measured in MLs with L_{NW} as the nanowire length in nm and h_{GaAs}=0.326 nm as the height of one ML of GaAs. Furthermore, τ is the mean nanowire length, D the variance of Green's function of the LD without nucleation delay, α describes the nucleation probability of the very first nanowire ML inside the SiO$_x$ openings of a certain number density with respect to the upper MLs (nucleation delay). $erfc(x)$ denotes the complementary error function. The overall variance σ^2 of the nanowire LD described by the function in Eq. 4.8 is given by Eq. 4.9

$$\sigma^2 = D + \frac{1}{\alpha^2}, \tag{4.9}$$

and takes into account two contributions. That is, (i) a symmetric contribution expressed by the term D, and (ii) an asymmetric contribution described by the term $1/\alpha^2$. The latter originates from nucleation delay. The symmetric contribution D to the overall variance of the LD further accounts for two effects. That is, symmetric narrowing due to nucleation antibunching described by the term $1/2\epsilon$, and symmetric broadening due to kinetic fluctuations, i.e. number density-dependent beam shadowing represented by the term $D_1(N)$. As already discussed with respect to Fig. 4.15, beam shadowing leads to a decrease of the mean length of the nanowires in denser nanowire ensembles. Thus, the role of beam shadowing as an additional broadening effect of the nanowire LD has to be considered in the model besides nucleation-induced broadening. Moreover, it has been shown that beam shadowing increases the variance of the LD in self-catalyzed GaAs nanowire ensembles [103]. Thus, the symmetric contribution D to the overall variance σ^2 of the LD is expressed by Eq. 4.10

$$D = \frac{1}{2\epsilon} + D_1(N). \tag{4.10}$$

In order to achieve a sub-Poissonian LD, $1/\alpha^2$ and $D_1(N)$ must be minimized. Minimization of $1/\alpha^2$ and $D_1(N)$ should be achieved if the nucleation of the nanowires on the substrate is synchronized and if kinetic fluctuations are eliminated. The analytical description of the nanowire LDs in this model is a refinement of the continuum-growth theoretical model described in Chapter 2.4.2. The refined model is now employed in this dissertation to fit the LDs of GaAs nanowire ensembles.

Tab. 4.1: SMP and statistical parameters of different GaAs nanowire samples. Tab. 4.1 is reproduced with permission from [201]. © 2018 IOP Publishing. All rights reserved.

Sample ID	SiO$_x$ thickness L_{ox} (nm)	SMP			NW number density (cm^{-2})	Measured mean NW length (MLs)	meas. σ (MLs)	fitted σ (MLs)	fitted $1/\alpha$ (MLs)	fitted $\sqrt{D}$ (MLs)
		T_{a1} (°C)	T_d (°C)	T_{a2} (°C)						
A (D0184)	1.9	770	490	760	5.0×10^{8}	8061	233	225	200	104
B (D0180)	1.9	770	570	760	2.4×10^{7}	8733	211	211	200	60
C (D0179)	1.9	770	590	760	3.4×10^{6}	8924	179	179	167	52
D (D0276)	1.5	750	570	735	1.8×10^{7}	9612	56	56	40	40
E (D0302)	1.5	770	580	760	2.7×10^{7}	9469	40	40	1	40
F (D0239)	1.5	750	570	735	4.4×10^{7}	9354	54	54	10	53
G (D0253)	1.5	750	570	735	8.9×10^{6}	9413	63	63	29	56

Three types of GaAs nanowire samples were involved in this study as listed in Tab. 4.1. The first type concerns samples A, B and C. The second type is represented by samples D and E. The third type concerns samples F and G. In all samples, different SMP parameters have been used for substrate preparation as will be described later in detail. Subsequent to the SMP, GaAs nanowires were always grown for 15 min using the usual growth conditions (T_{gr}=615°C, V/III=11).

Side-view SEM images of samples A to E are shown in Figs. 4.19 (a)-(e). The corresponding histograms are illustrated in Figs. 4.19 (f)-(i). The measured nanowire LDs of all samples are compared with their best fits by Eq. 4.8 (solid lines in Fig. 4.19). As shown representatively for samples A to E in the histograms of Fig. 4.19 (f)-(i), the measured LD shapes are reproduced very well by the fits using Eq. 4.8, which demonstrates a good agreement between experimental and fitted standard deviations σ. Statistical parameters obtained from the model fits are summarized for all samples in Tab. 4.1.

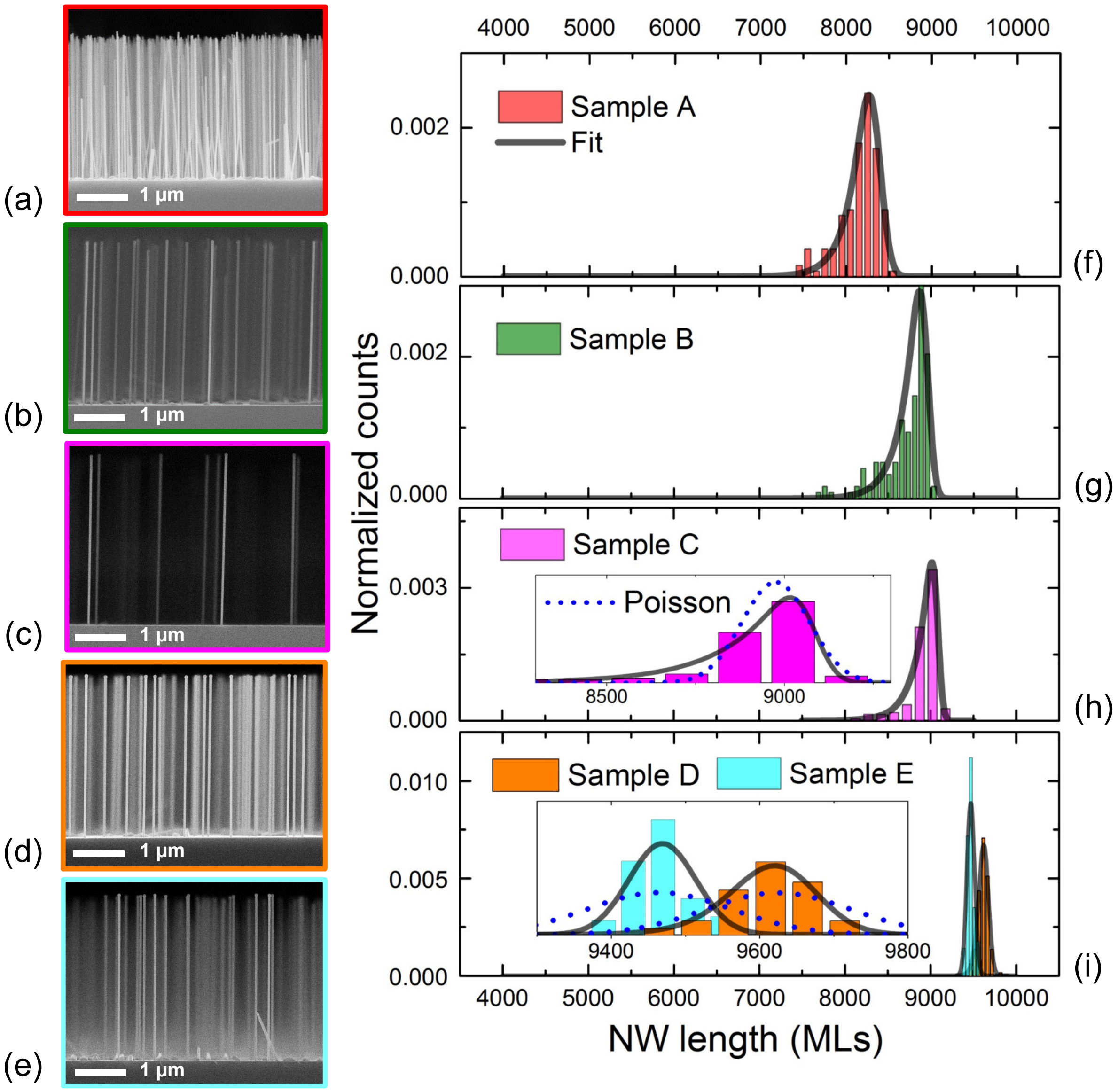

Fig. 4.19: Representative side-view SEM images of as-grown GaAs nanowire ensembles on native-SiO$_x$/Si(111) substrates of samples A (a), B (b), C (c), D (d), and E (e). Histograms of the measured nanowire lengths of samples A (f), B (g), C (h), D and E (i). The solid lines indicate the fits of the LDs according to Eq. 4.8. The insets in (h) and (i) show a close-up view of the LDs. The dotted lines represent the Poissonian LDs for the same mean length. Reproduced with permission from [201]. © 2018 IOP Publishing. All rights reserved.

For samples A to E, the measured and fitted overall variance σ^2 was normalized to the measured mean nanowire length $\langle s \rangle$, and plotted as a function of the nanowire number density N in Fig. 4.20 (black and blue symbols respectively). For a GaAs nanowire ensemble with a Poissonian LD, σ^2 should equal $\langle s \rangle$, which is indicated by the dashed line in Fig. 4.20. To provide a better insight into the single contributions to the broadening of the nanowire LDs, the overall normalized variance $\sigma^2 / \langle s \rangle$ was split into its symmetric and asymmetric parts D and $1/\alpha^2$, both again normalized to $\langle s \rangle$, and plotted as green and red symbols in Fig. 4.20, respectively.

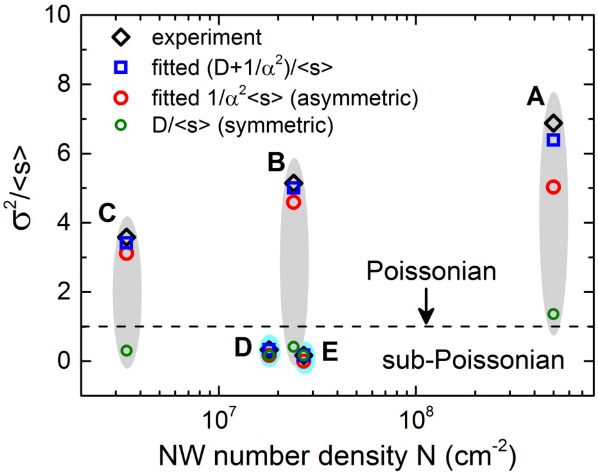

Fig. 4.20: Plot of the measured (black diamonds) and fitted (blue squares) overall variance normalized to the mean nanowire lengths as a function of the nanowire number density for samples A to E in Tab. 4.1. The individual normalized contributions of kinetic fluctuations $D/\langle s\rangle$ and nucleation delay $1/\alpha^2\langle s\rangle$ to the overall normalized variance $\sigma^2/\langle s\rangle$ are plotted as green and red circles respectively. The dashed line at $\sigma^2/\langle s\rangle = 1$ indicates the Poissonian variance and separates the nanowire LDs, which are broader and narrower (above and below the line) than Poissonian. All variance values of each sample are highlighted in gray and cyan color indicating broader and narrower LDs than Poissonian. Reproduced with permission from [201]. © 2018 IOP Publishing. All rights reserved.

The first part of the study concerns the investigation of the impact of the number density of GaAs nanowires on their LD, which is represented by samples A, B and C. In samples A, B and C, the number density of GaAs nanowires has been varied intentionally from 5.0×10^8 cm^{-2} in sample A to 3.4×10^6 cm^{-2} in sample C by appropriate selection of T_d in SMP step-2 (see Tab. 4.1). T_{a1} in SMP step-1 and T_{a2} in SMP step-3 were kept constant in order to produce a similar size of the SiO$_x$ openings. The employed Si substrates exhibit a thickness of the native-SiO$_x$ layer of 1.9 nm. As illustrated in the histograms in Figs. 4.19 (f)-(h), the LD width decreases (corresponding to a reduced σ^2), and the asymmetry decreases with decreasing nanowire number density from 5.0×10^8 cm^{-2} to 3.4×10^6 cm^{-2}. Nevertheless, the LDs of all three samples are clearly broader than Poissonian (i.e. $\sigma^2/\langle s\rangle > 1$) as shown in Fig. 4.20. The main contribution to the broadening of the nanowire LD originates from the asymmetric part. This means, that nucleation of the nanowires on their substrate takes long compared to the upper MLs, or in other words, the nucleation probability of the first nanowire ML inside the SiO$_x$ openings is lower than that of the subsequent MLs inside the same nanowire. This is represented by relatively small values of α in the range of 0.005 to 0.006 in Tab. 4.1. Two regimes of the monotonic increase of $\sigma^2/\langle s\rangle$ with N can be identified. For $N < 10^8$ cm^{-2}, the increase of $\sigma^2/\langle s\rangle$ with N is related to an effect of the number density on the formation of Ga droplets prior to nanowire nucleation. More specifically, the formation of Ga droplets inside the SiO$_x$ openings takes longer at higher N due to enhanced competition of the Ga droplets for collection of Ga adatoms from the diffusion Ga flux on the substrate when the same Ga flux is employed. The symmetric contribution to the broadening of the LD plays a minor role in this regime, but becomes dominant for $N > 10^8$ cm^{-2}, which is mainly related to beam shadowing of the As flux. Beam shadowing is random and as a result, some nanowires may receive more or less As than others on the same substrate.

Those findings suggest that the nanowire LD should be reduced down to the sub-Poissonian regime for $N < 10^8$ cm^{-2} if the nucleation delay is eliminated ($\alpha = 1$), and the nucleation of the first ML of all nanowires on the substrate is better synchronized. This is demonstrated with samples D and E in Tab. 4.1. In both samples, the SMP was performed on substrates with a 1.5 nm thin native-SiO$_x$ layer. T_d in SMP step-2 was selected to produce a similar, but low enough nanowire number density of $\sim 2.0\times 10^7$ cm^{-2} in order to minimize $D_1(N)$. Moreover, different annealing temperatures T_{a1} in SMP step-1 and T_{a2} SMP step-3 were used. As can be seen in the side-view SEM images in Fig. 4.19 (d) and (e) as well as in the histograms of Fig. 4.19 (i), the nanowire LDs of samples D and E are narrower and more symmetric compared to samples A, B and C. The values of the normalized variances $\sigma^2/\langle s\rangle$, including their individual normalized contributions $D/\langle s\rangle$ and $1/\alpha^2\langle s\rangle$, are additionally plotted for samples D and E in Fig. 4.20. As shown, the asymmetric contribution to the overall broadening of the nanowire LD has been minimized for samples D and E (i.e. shift of red data points down to the sub-Poissonian regime), and has become comparable to the symmetric contribution. In particular for sample E, a fitting parameter of $\alpha = 1$ was deduced, which reveals a negligible nucleation delay. As a result, GaAs nanowire ensembles with considerably narrow sub-Poissonian LDs were obtained, which is exclusively attributed to nucleation antibunching as the dominant mechanism in the nanowire ensembles, while broadening effects were successfully suppressed.

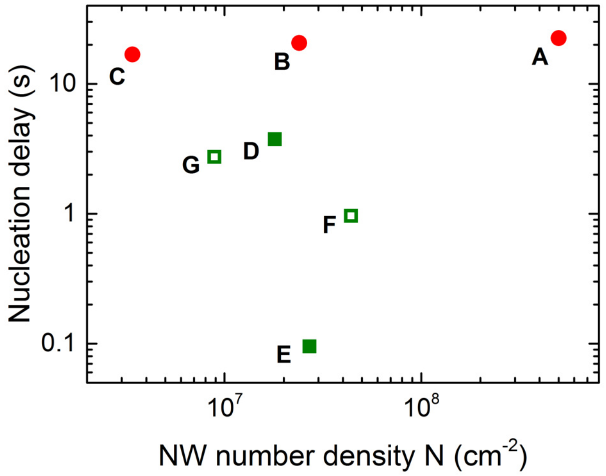

Fig. 4.21: Plot of the average nucleation delay time of GaAs nanowires as a function of their number density for all samples in Tab. 4.1. Red (green) symbols correspond to samples with a native-SiO$_x$ layer of L_{ox}=1.9 nm (1.5 nm), and nanowire LDs broader (narrower) than Poissonian. Reproduced with permission from [201]. © 2018 IOP Publishing. All rights reserved.

The nucleation delay time Δt was calculated with Eq. 4.11, that was obtained by solving Eq. 2.16 for Δt (Chapter 2.4.2), using the extracted fitting parameter α as listed in Tab. 4.1.

$$\Delta t = \frac{1}{\alpha \cdot GR_{ax}} = \frac{1}{\alpha} \cdot \frac{t_{gr}}{\tau} \tag{4.11}$$

GR_{ax} is the average growth rate in ML/s, τ the mean nanowire length, and t_{gr} the growth duration. The results for all samples are plotted in Fig. 4.21 as a function of the nanowire number density N. Samples A, B and C that were grown on substrates with a native-SiO$_x$ thickness of 1.9 nm (red symbols) exhibit nucleation delay times Δt in the range of 16 to 23 s. According to Fig. 4.20, all those samples possess nanowire LDs, which are broader than Poissonian. In contrast, all samples that were grown on substrates with a native-SiO$_x$ thickness of 1.5 nm (green symbols) reveal much shorter Δt, in the range of 0.1 to 4 s. These samples exhibit sub-Poissonian nanowire LDs. Shorter Δt in thinner SiO$_x$ layers are associated with a better synchronization of nanowire nucleation inside larger SiO$_x$ openings. This is evidenced from the comparison of samples B and E, where the same annealing temperature T_{a2} (i.e. 760 °C) employed on substrates with thicker (L_{ox}=1.9 nm in sample B) and thinner (L_{ox}=1.5 nm in sample E) native-SiO$_x$ layer should lead to smaller or larger openings respectively. This could not be confirmed by direct measurements of the size of the openings for the different SiO$_x$ thicknesses after the SMP and before nanowire growth because it is technically challenging to determine such small sizes (in the range of 5 nm for the 1.5 nm thin SiO$_x$ layer as shown in the inset of Fig. 4.10 (b)) with good enough resolution. Despite the lack of direct measurements of the size of the openings, it has been reported that the growth rate of voids in ultrathin SiO$_x$ layers depends on both the annealing temperature and the SiO$_x$ thickness, and increases at higher annealing temperatures, or for thinner SiO$_x$ layers [217]. Following Ref. [217], it is therefore assumed that the SMP has produced larger openings (i) in the thinner SiO$_x$ layer at same T_{a2} (comparison of samples B and E), and (ii) at higher T_{a2} for same SiO$_x$ thickness (comparison of samples D and E). Therefore, thinner SiO$_x$ layers or higher T_{a2} result in an improved synchronization of the nanowire nucleation inside larger SiO$_x$ openings, and thus in a remarkably short nucleation delay time Δt of ~100 ms as compared with Δt=21 s for sample B, and Δt=4 s for sample D.

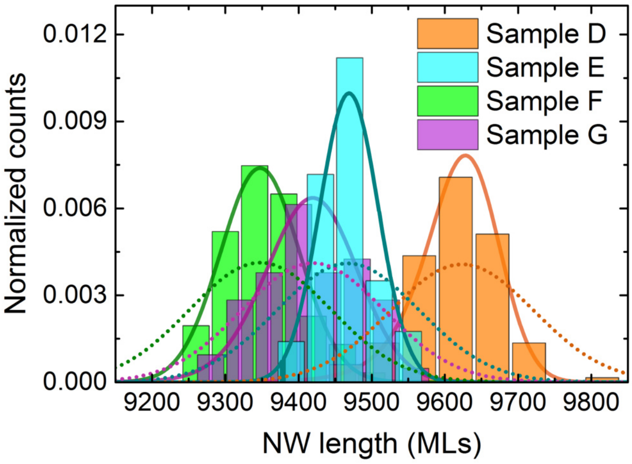

Fig. 4.22: Close-up view of histograms of the measured nanowire lengths of samples D, E, F, and G. The solid lines indicate the fits of the LDs according to Eq. 4.8. The dotted lines represent the Poissonian LDs for the same mean length. Reproduced with permission from [201]. © 2018 IOP Publishing. All rights reserved.

To test the reproducibility of growth of GaAs nanowire ensembles with sub-Poissonian LDs, a third type of samples, i.e. samples F and G, was prepared on substrates with the same SiO$_x$

thickness using the same SMP parameters as for sample D (see Tab. 4.1). Close-up views of the histograms of the measured nanowire lengths and their model fits by Eq. 4.8 are illustrated in Fig. 4.22 for samples F and G together with samples D and E. Samples F and G again exhibit nanowire LDs narrower than Poissonian. The nucleation delay times Δt are equal to 1 and 3 s respectively and have been plotted additionally in Fig. 4.21. Therefore, sub-Poissonian LDs in GaAs nanowire ensembles were reproducibly realized, when substrates of the same type (i.e. with the same SiO$_x$ thickness) and identical SMP parameters were employed. This result demonstrates the robustness and reliability of the developed SMP method. It is anticipated that sub-Poissonian LDs are possible also on substrates with different SiO$_x$ thicknesses after appropriate tuning of the SMP parameters.

4.3.5 GaAs Nanowires with High Crystal Quality

The crystal structure of GaAs nanowires, that were grown inside well-prepared SiO$_x$ openings produced by the SMP, has been investigated. For this purpose, sample D (Tab. 4.1) has been selected and six nanowires of this sample have been analyzed by HRTEM in order to obtain reliable statistics. Figure 4.23 shows an overview TEM image of a representative GaAs nanowire together with close-up HRTEM images and their FFT analysis. The nanowires are single crystals with ZB structure and only a few SFs. In particular, only a very short defective segment of ~50 nm was found at the nanowire base (region 1, magnified in Fig. 4.23 (b)) which contains only a few (less than 15) rotational TPs (special type of planar defect in nanowires, see Chapter 2.5.1 for detailed explanation). The formation of TPs in the lower nanowire segment is attributed to a transient in the size, and thus the contact angle, of the Ga droplets in the beginning of nanowire growth. As described in Chapter 2.5.2, contact angles of ~100° lead to the formation of WZ phase, whereas contact angles larger than ~130° result in the formation of ZB phase. Thus, the formation of twinned ZB GaAs at the nanowire base is related to a gradual increase of the contact angle in the range of ~110° to ~130° in the beginning of nanowire growth. Already after ~50 nm of growth, the Ga droplets must have reached a steady-state contact angle of ~130° and nanowire growth continues in stationary conditions. This resulted in a long defect-free nanowire section above the short defective segment. This finding is in clear contrast to the relatively long defective segments of ~400-800 nm at the base of the nanowires when no pre-growth treatment of the substrates is performed (see Fig. 2.18 in Chapter 2.5.3). Therefore, it is suspected that the well-prepared and large enough openings in the native-SiO$_x$ layer produced by the SMP appear not only advantageous for synchronized nanowire nucleation, but also for a high structural quality of the nanowires from the early stage of growth.

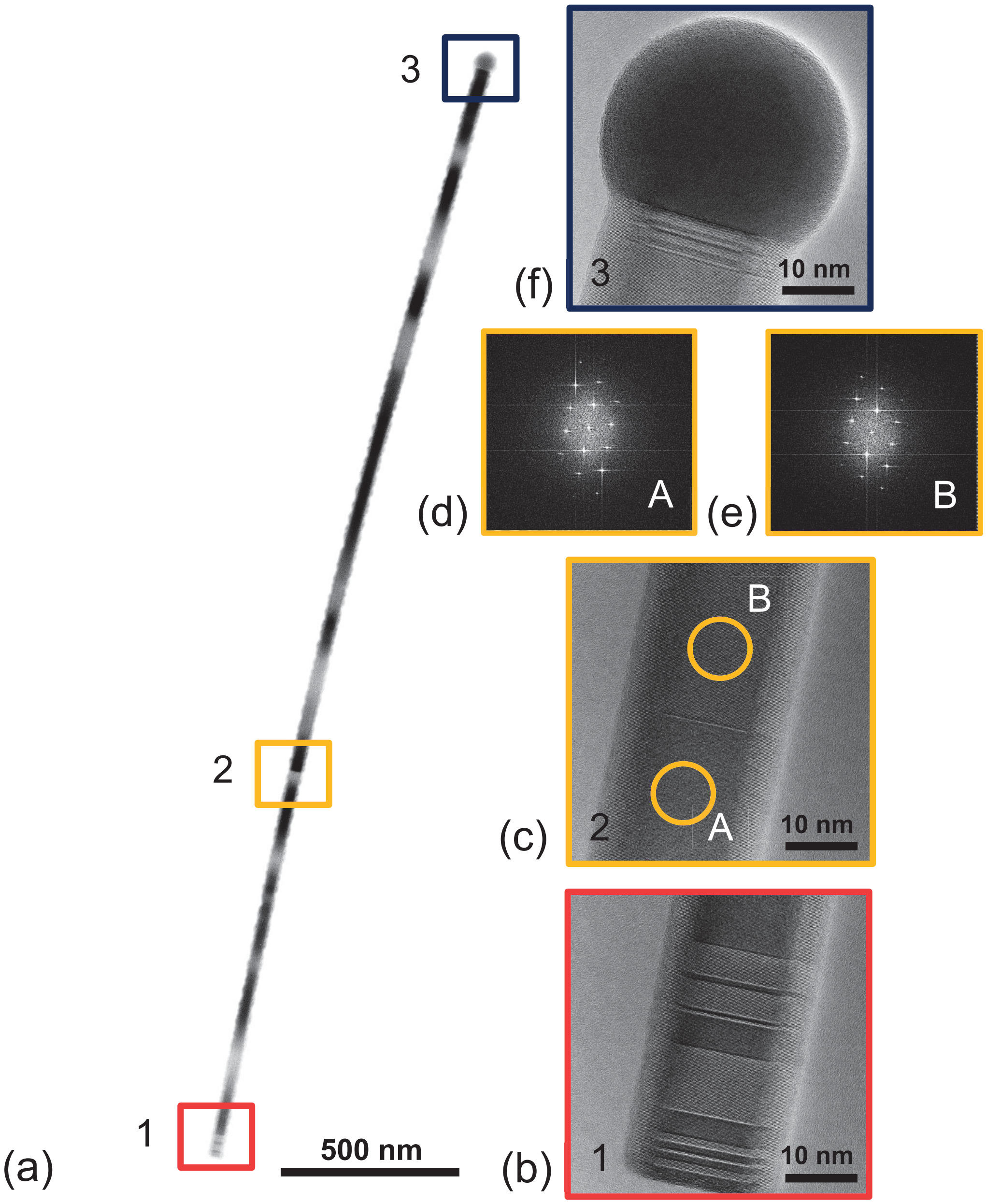

Fig. 4.23: (a) Side-view TEM image of a representative GaAs nanowire of sample D with marked nanowire segments denoted as region 1, 2 and 3. (b) Close-up TEM image of the lower defective segment of the nanowire (region 1). (c) Close-up TEM image of a selected portion of the middle segment of the nanowire (region 2) showing the only twin plane in the entire middle segment. (d), (e) Fast Fourier transform analysis of the regions denoted as A and B in (c) that indicate a pure zinc blende crystal phase aside from the twin plane in the middle segment. (f) Close-up TEM image of the nanowire tip (region 3), which illustrates a very short defective segment below the Ga droplet.

This is confirmed by Fig. 4.24, which shows the distribution of SFs (mostly TPs) along the axis of different GaAs nanowires for the case that SiO$_x$ openings were produced by the SMP prior to nanowire growth (in green color), or without formation of SiO$_x$ openings (omission of the SMP) prior to nanowire growth (in red color). As indicated in Fig. 4.24, the number of TPs in the lower defective segments of the nanowires was drastically reduced (by a factor of 4 to 6), and their average length was shortened (by a factor of 2 to 10) when SiO$_x$ openings were created by the SMP prior to nanowire growth. More specifically, the analysis of the number of TPs confirms that it does not increase significantly after growth of 50 to 100 nm long base segments for all investigated nanowires. This result implies that the Ga droplets must have grown already large enough inside the SMP-created SiO$_x$ openings when the nucleation of the first monolayer of GaAs takes place. In particular, the droplet contact angle must have exceeded already ~100° at the onset of nanowire nucleation on the substrate, since no evidence for WZ has been found, neither from *in situ* RHEED observations in the initial stage of growth as indicated in Fig. 4.24 (b), nor from *ex situ* HRTEM studies of the base segments. The formation of large enough Ga droplets is attributed to an enhanced sticking of Ga adatoms on the exposed Si substrate inside the well-prepared SiO$_x$ openings. Large enough Ga droplets, in turn, must be followed by a faster self-equilibration (shorter transition time) of their contact angles until steady-state values of ~130° were achieved (i.e. for a low number density of openings and the usual growth conditions). Furthermore, this finding indicates that all Ga droplets, that were formed inside the well-prepared openings, must also exhibit a high size uniformity because all investigated nanowires of sample D show similar short defective base segments.

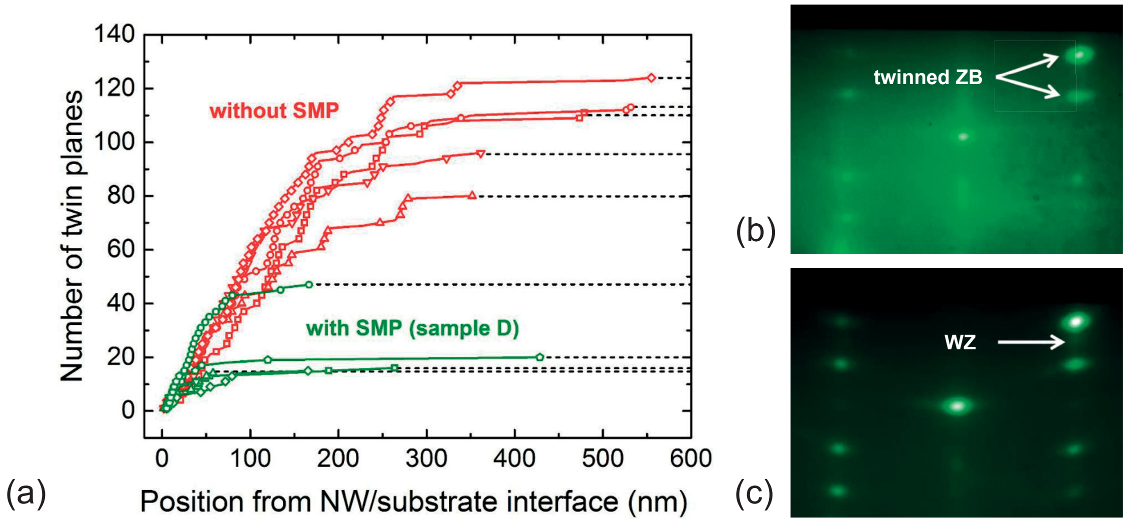

Fig. 4.24: (a) Plot of the total number of TPs as a function of the length of the base segments of GaAs nanowires, when the SMP has been performed (in green color) or omitted (in red color) prior to nanowire growth. (b), (c) *In situ* RHEED patterns of (b) twinned ZB GaAs after formation of SiO$_x$ openings by the SMP, and (c) additional weak WZ GaAs without prior formation of SiO$_x$ openings by the SMP. Both RHEED patterns were recorded in the initial stage of nanowire growth of the two samples shown in (a).

In contrast, without formation of SiO$_x$ openings of high quality (omission of the SMP), the Ga droplets must be smaller (contact angles in the range of ~100° to ~110°) when the nucleation of the first monolayer of GaAs takes place. This is concluded from *in situ* RHEED patterns, which additionally revealed a weak WZ spot between the two ZB spots in the initial stage of growth as shown in Fig. 4.24 (c). *Ex situ* HRTEM analysis of the base segments also revealed short WZ sections inside the twinned ZB GaAs base segments. Smaller Ga droplets at the onset of nanowire nucleation are attributed to a weak sticking and enhanced desorption of Ga adatoms from the SiO$_x$ due to lack of SiO$_x$ openings with the exposed Si surface or insufficient quality of

SiO$_x$ openings. Moreover, a weak dependence of the number density of SiO$_x$ openings on the size of the Ga droplets cannot be ruled out since the former one cannot be controlled when the SMP is omitted. The step-like evolution of the number of TPs in the nanowire base segments grown without prior formation of SiO$_x$ openings may imply that the contact angles of the droplets periodically increase to a new equilibrium. At this point, further investigations are necessary to confirm that. Interestingly, Koivusalo *et al.* also observed relatively short defective sections of ∼150 nm at the base of their GaAs nanowires, which were grown inside lithography-free nanohole templates [109]. Their findings further strengthen the presented observations that the high structural quality of the nanowire base sections correlates with the quality of the prepared SiO$_x$ openings, and thus nucleation synchronization.

The lower defective segment is followed by a ∼3 μm long section nearly free of TPs. Only one TP in the entire middle segment of the nanowire in region 2 (magnified in Fig. 4.23 (c)) was found, which demonstrates excellent crystal quality. FFT analysis of the nanowire crystal in region A and B in Fig. 4.23 (c) clearly reveals single ZB phase as can be seen in the corresponding FFT spectra in Figs. 4.23 (d) and (e). The nanowire tip in region 3 (magnified in Fig. 4.23 (f)) shows a ∼10 nm defective section that contains SF and WZ/ZB polytypes. Such polytypic segments are commonly observed [69, 123, 126, 146] and associated again with a local transient of the contact angle of the Ga droplets during growth termination as already described in detail in Chapter 2.5.3. Axial growth is prolonged unintentionally during droplet consumption under non-ideal conditions (i.e. high As background pressure in the growth chamber due to its long shut-off transient compared to the Ga flux despite simultaneous interruption), that produces SFs and short WZ insertions at the tip segments. By introducing a novel growth method in Chapter 5, it will be demonstrated how the defective segments in the nanowire crystals can be further minimized.

4.4 Conclusions

A simple *in situ* surface modification procedure of native-SiO$_x$/Si(111) substrates has been developed in order to prepare the substrate surface for self-catalyzed growth of GaAs nanowire ensembles. The SMP decouples the two roles of Ga droplets: the Ga-assisted formation of nano-sized openings in the SiO$_x$ from the Ga-assisted nucleation and growth of GaAs nanowires inside those openings. This was achieved by employing different Ga droplets for each purpose. Thus, Ga droplets employed for the formation of SiO$_x$ holes were removed before new Ga droplets drive the growth of GaAs nanowires therein. This is in clear contrast to self-catalyzed growth of GaAs nanowires without prior pre-growth treatment of the substrates, where both mechanisms take place underneath the same Ga droplets.

The SMP consists of three steps: (step-1) the first substrate annealing at high enough temperatures to roughen the SiO$_x$, (step-2) Ga deposition and droplet formation with controlled number density, which then create openings of equal number density in the SiO$_x$, and (step-3) the second substrate annealing at high enough temperatures to evaporate the Ga droplets and to increase the size of the openings in the SiO$_x$, where finally the nucleation of GaAs takes place. If all three steps of the SMP are performed under well-tuned conditions, vertical GaAs nanowires can be successfully grown. All individual steps of the SMP and their resulting surface modifications of the substrate are schematically illustrated in Fig. 4.25.

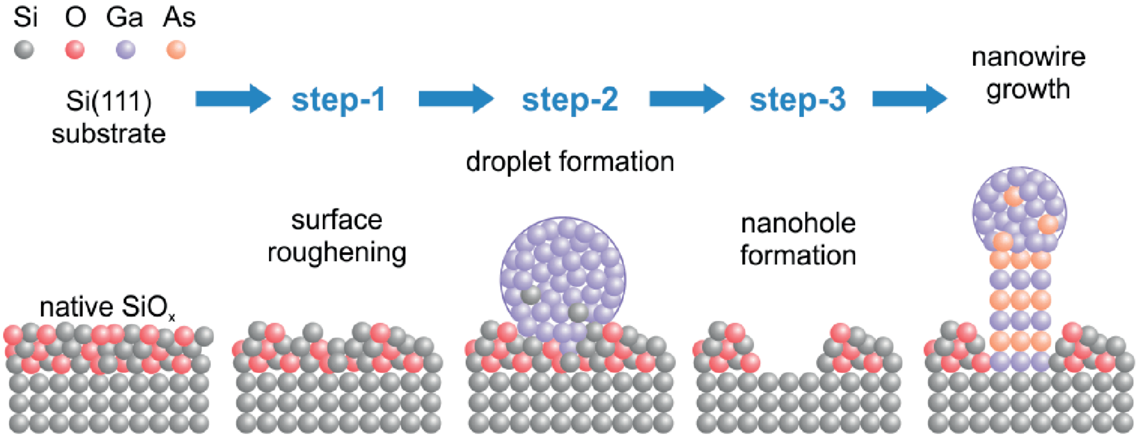

Fig. 4.25: Schematic illustration of the *in situ* SMP of native-SiO$_x$/Si(111) substrates. Adapted with permission from [47]. Copyright (2017) American Chemical Society.

The SMP enables independent control of the size and number density of SiO$_x$ openings, which provides unique advantages in the self-catalyzed growth of GaAs nanowire ensembles on native-SiO$_x$/Si(111) substrates. That is, (1) a high nucleation synchronization of the nanowires on their substrate inside well-prepared SiO$_x$ openings, which routinely produces exceptionally uniform GaAs nanowire ensembles with sub-Poissonian length distributions, and which proves theoretical predictions about nucleation antibunching, (2) excellent control of nanowire growth without time-consuming and costly *ex situ* substrate patterning, i.e. deliberate control of the number density of GaAs nanowires within three orders of magnitude without changing growth conditions, high number yields of vertical GaAs nanowires against parasitic GaAs islands (up to ∼80%), and independent control of the nanowire dimensions from their number density, (3) zinc blende GaAs nanowires with improved structural quality (less stacking faults) close to the interface with the substrate, and (4) high reproducibility of all growth results, which demonstrates the robustness and reliability of the SMP method.

5 Droplet-Confined Alternate Pulsed Epitaxy (DCAPE) of GaAs-Based Nanowires on Si

This chapter concerns a novel growth method for self-catalyzed GaAs-based nanowires on Si substrates. The new method is denoted as droplet-confined alternate-pulsed epitaxy. The main characteristics of DCAPE are the enhancement of the surface diffusivity of Ga as well as the precise control of the size of the Ga droplets. These enable self-catalyzed growth of GaAs nanowires and GaAs-based axial nanowire heterostructures with excellent structural quality at unconventional, low temperatures on Si, which is a pre-requisite for their monolithic integration on Si-CMOS platforms, and has not been demonstrated before. Part of the findings presented in this chapter has been published in the ACS Journal Nano Letters entitled as “Droplet-Confined Alternate Pulsed Epitaxy of GaAs Nanowires on Si Substrates down to CMOS-Compatible Temperatures” [224].

5.1 Inherent Challenges in the Self-Catalyzed Growth of GaAs-Based Nanowires at High Growth Temperatures

As presented in Chapter 4, free-standing vertical GaAs nanowire ensembles on native-$SiO_x/Si(111)$ substrates with predominant ZB structure, remarkable size uniformity and tunable nanowire number density and dimensions can be produced, when the SMP is employed. Despite those essential achievements, three main challenges still exist:

1. High growth temperatures (T_{gr}) in the range of 560 to 630 °C are always required to ensure a high surface diffusivity of Ga on the substrate and the nanowire sidewalls towards the Ga droplets at the nanowire tips in the presence of As (the dependence of the surface diffusion length of Ga on the temperature is discussed in Chapter 2.3.3); and high V/III ratios are necessary to compensate the high arrival rate of Ga atoms at the droplets [47, 68, 69]. However, such high growth temperatures are incompatible with the standard Si-CMOS platform due to the large thermal budget which is transferred to the wafer and a reduction of the growth temperature below 450 °C is necessary to prevent dopant redistribution or to enable integration of the nanowires in the back-end-of-line (subsequent to the metallization level) if relevant. To the best of my knowledge, only two attempts have been made so far to realize self-catalyzed growth of GaAs nanowires at unconventional, low substrate temperatures. For instance, Ermez *et al.* demonstrated self-catalyzed MOCVD growth of GaAs nanowires on GaAs(111)B substrates at temperatures in the range of 420 to 435 °C [225]. In another study by Yu *et al.*, self-catalyzed MBE growth of GaAs nanowires on Si(111) substrates has been achieved at temperatures in the range of 500 to 560 °C [226]. In both studies, a two-temperature procedure has been employed, in which the formation of Ga droplets and/or nucleation of nanowires was carried out at relatively high substrate temperatures (i.e. at T_{gr}=500-600 °C [225], and T_{gr}=620 °C [226]), and subsequently, growth or elongation of the nanowires was performed after cooling the substrates down to lower

temperatures. All as-grown GaAs nanowires exhibit a strong tapered shape and poor structural quality, i.e. existence of a high number of SFs perpendicular to the nanowire axis, independent of the growth technique (MOCVD or MBE) and the substrate type (GaAs or Si). Both the tapering and the planar defects were associated with a decreasing droplet size during nanowire growth, which was caused by limited surface diffusivity of Ga on the substrate and nanowire sidewalls at low growth temperatures [225, 226].

2. Poor control of the crystal structure of GaAs nanowires due to insufficient control of the contact angle of the Ga droplets during growth initiation and termination. This leads to relatively long defective segments at the bottom and the tip of the nanowires that consist of WZ/ZB polytypes, SFs and TPs as described in Chapter 2.5. Numerous efforts have already been made to tackle the challenge of obtaining satisfactory control of the crystal structure during the self-catalyzed growth of GaAs nanowires. In reality, a fairly good level of structural control has been demonstrated, where epitaxial growth was always performed under continuous beam supply [109, 124, 137, 138, 139, 227]. As an alternative solution, beam flux interruption and pulsing techniques appear very efficient for the reduction of the SF density and control of the crystal structure and phase purity as has been demonstrated for Au-catalyzed growth of InAs, GaP and GaP/GaAsP nanowires [141, 142, 143].

3. Growth of axial III-V nanowire heterostructures with atomically sharp interfaces is challenging due to compositional grading, which is attributed to undesirable phenomena, such as the reservoir effect [163, 165], atom interdiffusion [160, 169], and surface segregation [4, 170]. Those mechanisms are dominant at high growth temperatures, where kinetics cannot be suppressed. For Au-catalyzed growth of InAs/GaAs axial nanowire heterostructures, Dick *et al.* showed a weak dependence of the length of the interface gradient on the growth temperature, i.e. a shorter gradient at lower growth temperatures [163]. It has been furthermore demonstrated that sequential pulsing of the Ga source prior to growth of the GaAs segment reduces the reservoir effect by pushing In out from the Au catalyst, and thus produces significantly sharper interfaces [163]. To the best of my knowledge, only one study, that deals in detail with the self-catalyzed growth of GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ axial nanowire heterostructures, has been reported so far [167]. In this work, Priante *et al.* found that interruption of all beam fluxes and filling of the Ga droplets with Al prior to growth of $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ insertions, where As is supplied separately, is an efficient way to improve the abruptness of GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ interfaces (i.e. down to 2 MLs) [167]. Similarly, the same group demonstrated that beam flux interruptions appear beneficial in the self-catalyzed growth of GaP nanowires with short GaAs insertions in order to improve the sharpness of the GaP/GaAs interfaces [162].

Apparently, beam flux interruptions and pulsing methods (all demonstrated for conventional growth temperatures depending on the material to be grown) are promising in order to obtain control over both, the crystal structure of VLS-grown III-V nanowires, and their axial composition in heterostructures including the possibility for abrupt interfaces mainly due to efficient suppression of the reservoir effect. The reservoir effect and other unwanted phenomena can be prevented further, when nanowire growth is performed at lower temperatures, where kinetic processes are weak. Realization of nanowire growth at low temperatures would also pave the avenue towards CMOS-compatible integration of III-V nanowires on the industrial Si platform. Nevertheless, a high-enough surface diffusivity of growth species, i.e. Ga in the self-catalyzed growth of GaAs nanowires, has to be assured even at low temperatures.

In order to circumvent the inherent limitations in the self-catalyzed growth of GaAs-based nanowires, a novel growth method is presented and investigated systematically within this chapter. In particular, its capability with respect to Si-CMOS compatibility, structural control of the nanowires, and growth of axial nanowire heterostructures will be evaluated. This novel method uses sequential pulsing and interruptions of beam fluxes (as has been proposed being beneficial by various reports in the literature), and is performed at unconventional, low growth temperatures. In the following chapter, the method of droplet-confined alternate pulsed epitaxy (DCAPE) will be introduced and its technical realization elucidated. In Chapter 5.3, a detailed study of the basic growth parameters in DCAPE (i.e. T_{gr} and V/III ratio) will be presented. In specific, the effect of both T_{gr} and V/III ratio on the axial/radial growth rates, shape and crystal structure of short GaAs nanowire segments grown in DCAPE mode will be examined. In Chapter 5.4, the feasibility of DCAPE for direct nucleation and growth of GaAs nanowires on Si substrates will be tested. Furthermore, the impact of the type of the employed arsenic species on the shape and crystal structure of the nanowires will be studied. In Chapter 5.5, the applicability of DCAPE for growth of GaAs/$Al_xGa_{1-x}As$ axial heterostructure nanowires on Si substrates at low growth temperatures will be investigated.

5.2 DCAPE as a Novel Growth Approach for GaAs Nanowires

In clear contrast to conventional MBE of self-catalyzed GaAs nanowires, where all beam fluxes of the source elements are supplied simultaneously and continuously throughout the entire growth process, DCAPE uses short alternate pulses of Ga and As_4 beams. The introduction of DCAPE for self-catalyzed growth of GaAs nanowires on Si is inspired from the concept of migration-enhanced epitaxy (MEE). MEE has been developed for planar growth of uniform and atomically smooth GaAs-based heterostructures at low growth temperatures using pulsed beam supply [228]. The main advantage of MEE is the enhancement of the migration distance of Ga adatoms due to the fact that first, no As_4 molecules are present during Ga supply, and second, by a short substrate annealing at the growth temperature during beam interruption subsequent to Ga deposition [228]. The enhanced migration distance resulted in layer-by-layer growth of atomically flat GaAs on GaAs(001) surfaces with a roughness of maximal one monolayer, if the number of deposited Ga atoms per Ga pulse and unit area equals the number density of available surface sites [228]. In specific, two dangling bonds per As surface atom are available and should be fully covered with Ga atoms in each growth cycle on GaAs(001) surfaces. The enhancement of the migration distance in MEE can be compensated by reducing the growth temperature compared to conventional MBE of GaAs epilayers [228]. Another characteristic of MEE is the minimized planar growth of GaAs on GaAs(110) surfaces, which is exploited in selective area epitaxy of fine structures [228]. In contrast to MEE, the layer-by-layer growth mode is not intended in DCAPE, but rather the minimization of GaAs growth on GaAs(110) surfaces. To understand how DCAPE is expected to work, the atomic arrangement of surface atoms of the GaAs$\{1\bar{1}0\}$ nanowire sidewalls has to be considered as schematically illustrated in Fig. 5.1. Only one dangling bond per incorporated Ga or As surface atom is available for every incoming Ga or As atom. This results (i) in a low sticking and fast re-evaporation of incoming As_4 molecules from the nanowire sidewalls in absence of Ga adatoms (surface diffusion of As_4 is negligible [76]), and (ii) in a high diffusivity of Ga adatoms along the nanowire sidewalls in absence of As_4 molecules [229, 230]. Therefore, an enhanced and targeted delivery of Ga adatoms to the droplets at the nanowire tips should be possible by alternate pulsing of the beams at low temperatures, while planar growth on the nanowire sidewalls should be suppressed.

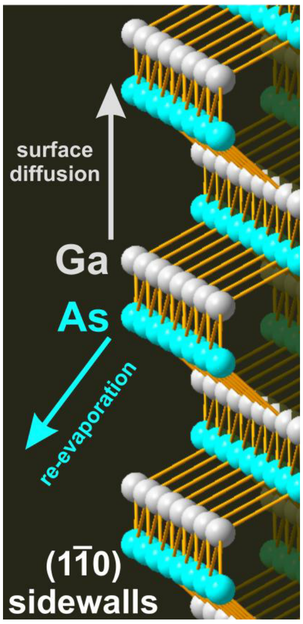

Fig. 5.1: Schematic illustration of the atomic arrangement of the surface atoms of the GaAs$\{1\bar{1}0\}$ nanowire sidewalls. Due to the incorporation of all three bonds per surface atom into the crystal lattice, only one dangling bond is available for creating new bonds with incoming Ga or As atoms.

To the best of my knowledge, only two growth studies of GaAs nanostructures under alternate pulsed beam supply have been presented so far. Iwai *et al.* showed selective-area vapor-solid growth of hexagonal GaAs disks on SiO_2/GaAs(111)B substrates at a relatively high temperature of T_{gr}=590 °C [231]. Self-catalyzed growth of GaAs nanowires on Si(111) substrates at intermediate temperatures in the range of 540-580 °C has been demonstrated by Kizu *et al.* [81]. These nanowires exhibit a high density of SFs. Despite the fundamental demonstration of growth, a detailed growth study is still lacking.

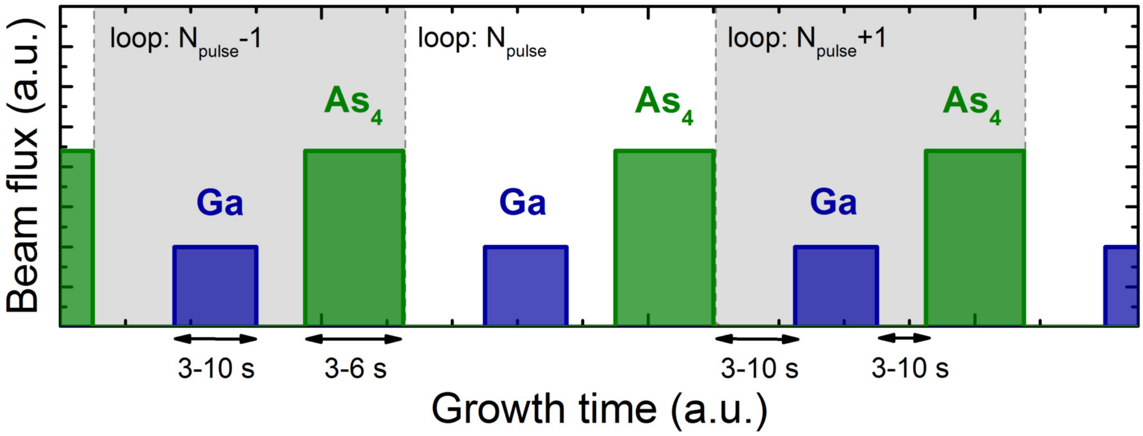

Fig. 5.2: Plot of the pulse sequence of Ga and As_4 beams during self-catalyzed growth of GaAs nanowires on Si(111) substrates in DCAPE mode.

A typical pulse sequence in DCAPE consists of an *interruption/Ga pulse/interruption/As_4 pulse*, which is repeated several times (loops). Figure 5.2 representatively illustrates three loops of a typical pulse sequence used in DCAPE. The beam pulses of Ga were generated by switching on and off the mechanical shutter of the Ga effusion cell. A motorized needle valve (part of the As cell) was employed for the creation of As_4 pulses in addition to the mechanical shutter of the As cell. The total amount of supplied Ga and As_4 per pulse is controlled by the beam fluxes (like in conventional MBE) or/and the duration of the beam pulses. DCAPE allows for supplying only a small number of growth species per pulse to the Ga droplets, which enables precise control of the growth processes. The amount of deposited Ga and As_4 in each pulse Θ_{Ga} and Θ_{As_4} given in equivalent thickness of planar GaAs is expressed by Eq. 5.1

$$\Theta_{Ga(As_4)} = F_{Ga(As_4)} \cdot t_{pulse(Ga(As_4))} \cdot S_{Ga(As_4)}, \tag{5.1}$$

where F_{Ga} and F_{As_4} are the Ga and As_4 beam fluxes given in equivalent growth rates on GaAs(001) substrates, $t_{pulse(Ga)}$ and $t_{pulse(As_4)}$ the durations of the Ga and As_4 pulses, and S_{Ga} and S_{As_4} the sticking coefficients of Ga and As_4. Θ_{Ga} and Θ_{As_4} have been varied in the range of 0.1-1.1 MLs and 0.7-1.4 MLs respectively. The corresponding V/III ratio is given by the ratio of the amount of deposited Ga and As_4 in each pulse according to Eq. 5.2

$$V/III = \frac{\Theta_{As_4}}{\Theta_{Ga}}. \tag{5.2}$$

The duration of the growth interruptions in between the Ga and As_4 pulses has been varied in the range of 3 to 10 s. The background pressure in DCAPE was typically in the range of $1\text{-}5{\cdot}10^{-9}$ Torr. All stated growth temperatures were measured before growth initiation with an optical pyrometer.

In the present growth study, DCAPE of GaAs nanowires or GaAs nanowire segments was performed at T_{gr} in the range of 450 to 550 °C. All DCAPE experiments were conducted on 3-inch n-type or p-type Si(111) substrates (Sb- or B-doped, 0.01-0.03 Ω·cm), which were uniformly covered by a native-SiO_x layer. Prior to DCAPE, the *in situ* SMP was always performed in order to create nano-sized openings of controlled number density and size in the native-SiO_x layer. The SMP was carried out as described in Chapter 4.2. Due to the use of new Si substrates, the SMP parameters had to be re-tuned. Thus, thermal annealing in SMP step-1 was performed for 1 h at T_{a1}=780 °C. T_d in SMP step-2 has been selected in the range of 530 to 570 °C, which resulted in an intermediate number density of GaAs nanowires in the range of 10^7 to 10^8 cm^{-2}. Thermal annealing of the substrates in SMP step-3 was carried out for 30 min at T_{a2}=740 °C.

5.3 Elongation of GaAs Template Nanowires in DCAPE Mode

The first part of the DCAPE study does not concern the nucleation stage of GaAs nanowires on Si substrates. It rather focuses on the elongation of conventionally grown GaAs nanowires. For this purpose, GaAs template nanowires were always grown under continuous supply of Ga and As_4 beams in conventional MBE using typical growth conditions (T_{gr}=615 °C, V/III=11). After template nanowires had grown 2 or 3 μm long, the growth in conventional MBE was interrupted by switching off all beam fluxes simultaneously and the substrate was cooled down for the following growth step in DCAPE mode. As a result of the interruption process, the Ga droplets at the tips of the template nanowires were not consumed, and thus, were used to resume the nanowire growth in DCAPE mode. For the growth study, several samples were prepared as listed in Tab. 5.1.

Tab. 5.1: Parameters for growth of short GaAs nanowire segments in DCAPE mode. F_{Ga} and F_{As_4} were calibrated for planar growth on GaAs(001) substrates. Θ_{Ga} and Θ_{As_4} are therefore given in equivalent thicknesses of planar GaAs(001). GR_{ax} has been determined from side-view length measurements of the nanowire segments.

Sample ID	T_{gr} (°C)	$t_{int.}$ (s)	$t_{pulse(Ga)}$ (s)	$t_{int.}$ (s)	$t_{pulse(As_4)}$ (s)	N_{pulse}	F_{Ga} (ML/s)	F_{As_4} (ML/s)	Θ_{Ga} (ML/pulse)	Θ_{As_4} (ML/pulse)	V/III	GR_{ax} (ML/s)
A (D0105)	550	3	6	3	6	300	0.12	0.23	0.72	1.38	1.9	2.07
B (D0109)	550	3	3	3	6	200	0.12	0.23	0.36	1.38	3.8	2.67
C (D0111)	550	3	3	3	6	200	0.06	0.23	0.18	1.38	7.7	2.52
D (D0114)	550	3	3	3	6	200	0.04	0.23	0.12	1.38	11.5	2.24
E (D0155)	500	10	5	5	4	420	0.06	0.24	0.30	0.96	3.2	1.69
F (D0157)	450	10	4	5	3	525	0.06	0.25	0.24	0.75	3.1	1.36
G (D0139)	450	-	-	-	-	-	0.28	0.25	-	-	0.9	1.81
H (D0167)	500	10	5	5	12	420	0.06	0.06	0.30	0.72	2.4	0.56
I (D0164)	500	10	5	5	12	420	0.06	0.08	0.30	0.96	3.2	0.58
J (D0163)	450	10	4	5	3	262	0.06	0.25	0.24	0.75	3.1	1.43
K (D0165)	450	10	4	5	3	131	0.06	0.25	0.24	0.75	3.1	0.66

5.3.1 Methodology of Growth Study Using Template Nanowires

As can be seen from the comparison of Figs. 5.3 (a) (template) and (b) (template+DCAPE), DCAPE produces short GaAs nanowire segments on top of the template nanowires.

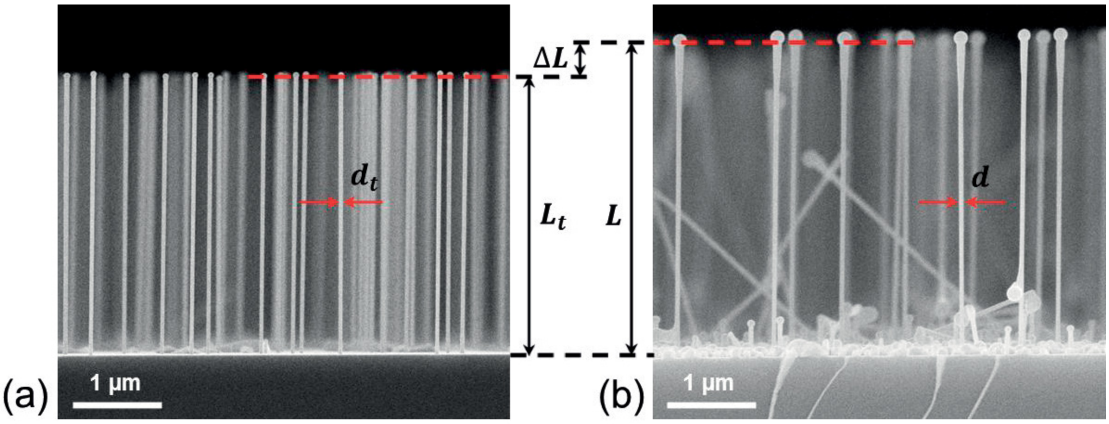

Fig. 5.3: Side-view SEM images of (a) GaAs template nanowires grown on native-SiO$_x$/Si(111) substrates at 615 °C using conventional MBE, and (b) GaAs template nanowires after elongation in DCAPE mode at 500 °C.

In order to determine the axial growth rate of the nanowire segment grown in DCAPE mode, statistical length measurements of 40 to 80 nanowires of each sample were carried out by SEM. The average length of the short nanowire segment ΔL is obtained by subtracting the average length of the template nanowires L_t from the average length of the elongated template nanowires L as depicted in Fig. 5.3. The axial growth rate GR_{ax} of the short nanowire segment is then obtained by dividing its average length ΔL by the total time of As$_4$ supply t_{As_4}, since the axial growth rate is limited by As$_4$. Thus, GR_{ax} is expressed by Eq. 5.3

$$GR_{ax} = \frac{\Delta L}{t_{As_4}} = \frac{L - L_t}{N_{pulse(As_4)} \cdot t_{pulse(As_4)}}, \tag{5.3}$$

where $N_{pulse(As_4)}$ is the number of As$_4$ pulses, and $t_{pulse(As_4)}$ the duration of each As$_4$ pulse. For determination of the radial growth rate GR_{rad} of the nanowires in DCAPE, the average diameter of the template nanowires d_t is subtracted from the mean diameter of the template nanowires d after their elongation in DCAPE mode. The diameters d_t and d were measured in the middle of 40 to 80 nanowires of each sample as indicated in Fig. 5.3. GR_{rad} is given by Eq. 5.4

$$GR_{rad} = \frac{d - d_t}{N_{pulse(As_4)} \cdot t_{pulse(As_4)}}. \tag{5.4}$$

The nanowire diameter of the DCAPE segments above the template nanowires is directly defined by the diameter of the Ga droplets, which can increase as indicated in Fig. 5.3 (b), or decrease during DCAPE depending on the local V/III ratio. This, in turn, leads to local thickening or thinning of the short nanowire segments.

5.3.2 Impact of Growth Parameters on Ga Surface Diffusivity and Nanowire Shape

The following section aims at discussing the impact of basic growth parameters, when DCAPE is employed for self-catalyzed growth of short GaAs nanowire segments. More specifically, the roles of the V/III ratio and the growth temperature are examined during growth of short GaAs nanowire segments.

First, the effect of the V/III ratio on the surface diffusivity of Ga adatoms, and shape of the nanowire segments is studied. In specially designed growth experiments, samples A to D as listed in Tab. 5.1 were fabricated, in which the amount of supplied Ga was varied (in particular, the duration of the Ga pulse in samples A and B, or the Ga flux in samples C and D), whereas the As_4 flux was always fixed. The change in the Ga supply during nanowire growth should affect the droplet size, and thus, the nanowire diameter, but not the axial growth rate GR_{ax}, which is controlled by the amount of supplied As_4 (As_4 was kept constant). Thus, GR_{ax} is approximately constant and only varies slightly in a range of 2.1 to 2.7 ML/s as can be seen in Tab. 5.1. Growth of GaAs nanowire segments was performed in DCAPE mode first at T_{gr}=615 °C, which is the typical substrate temperature for conventional MBE of GaAs nanowires. At T_{gr}=615 °C, elongation of 2 μm long template nanowires in DCAPE mode was not possible, which is associated with thermal decomposition of the template nanowires below the Ga droplets because of growth interruptions in DCAPE, during which the delivery of growth species to the droplets was cut off periodically. Lowering T_{gr} down to 550 °C prevented thermal decomposition of the template nanowires, and thus, enabled growth of short GaAs nanowire segments in DCAPE mode. Thus, all DCAPE experiments were performed at T_{gr}=550 °C in order to study the effect of the V/III ratio on the surface diffusivity of Ga adatoms and the shape of the nanowire segments. Side-view SEM images of GaAs nanowires of samples A to D are shown above the dashed line (MBE/DCAPE interface) in the corresponding insets A to D of Fig. 5.4. As can be seen, an increase in the V/III ratio from 1.9 in sample A to 11.5 in sample D, results in an improved shape of the DCAPE segment. More specifically, an optimal V/III ratio of 11.5 (sample D) was found to produce straight and non-tapered GaAs nanowire segments with equal diameters compared to the template nanowires. In contrast, nanowire segments grown under $V/III < 11.5$ (samples A to C) reveal inverse tapering (thickening). For $V/III > 11.5$, the Ga droplets at the nanowire tips were entirely consumed, which resulted in the cease of axial growth. These findings show that the Ga and As_4 beam fluxes at the nanowire tips need to match in order to maintain a constant size of the Ga droplets, and thus, to obtain a uniform diameter of the nanowire segments grown in DCAPE mode. Matching of the Ga and As_4 beam fluxes at the nanowire tips means that the local V/III ratio at the droplet/nanowire interface is equal to one. Thus, good matching requires well-tuned arrival rates of the growth species from both the direct and indirect (diffusion Ga and rebound As_4) beams at the growth interface. This is achieved by precise adjustment of $\Theta_{As_4}/\Theta_{Ga}$ (=V/III ratio) at a given T_{gr} in DCAPE mode.

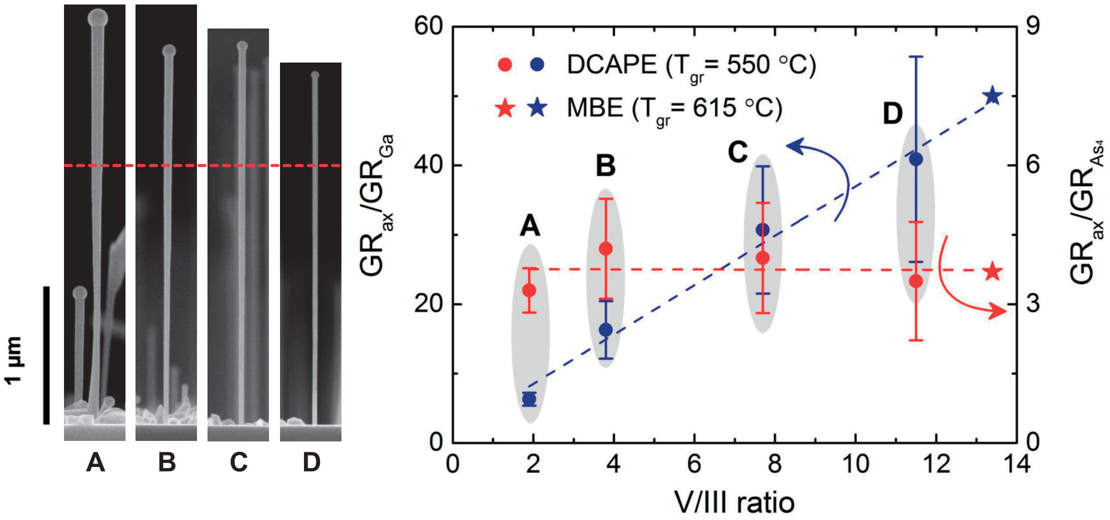

Fig. 5.4: Plot of the normalized growth rates GR_{ax}/GR_{Ga} (left axis) and GR_{ax}/GR_{As_4} (right axis) as a function of the V/III ratio during DCAPE of GaAs nanowire segments at 550 °C (circles) in comparison with conventional MBE at 615 °C (stars). The shape of the nanowire segments obtained for different V/III ratios is shown in the insets A to D. The dashed line indicates the MBE/DCAPE interface. Adapted with permission from [224]. Copyright (2016) American Chemical Society.

In order to study the dependence of Ga adatom surface diffusivity on the V/III ratio in DCAPE mode, the measured axial growth rate GR_{ax} of the nanowire segments was compared to the growth rates GR_{Ga} and GR_{As_4}, which would have been obtained if only the contributions of the direct Ga and As$_4$ beams to the nanowire growth were considered. GR_{Ga} and GR_{As_4} were calculated according to a theoretical growth model presented in Ref. [76]. The dependencies of GR_{ax}/GR_{Ga} and GR_{ax}/GR_{As_4} on the V/III ratio are shown in the plot of Fig. 5.4. As expected, the axial growth rate is insensitive to changes in the amount of incoming Ga atoms at the droplets, which is confirmed by the invariance of GR_{ax}/GR_{As_4} to the V/III ratio. Moreover, GR_{ax}/GR_{As_4} is larger than 1, which implies that the Ga droplets efficiently collect As$_4$ molecules from the rebound As$_4$ flux as suggested by Ramdani *et al.* [80]. On the contrary, the increase of GR_{ax}/GR_{Ga} with increasing V/III ratio reveals that Ga was incorporated more efficiently into the nanowire crystal, when the amount of supplied Ga was reduced. This is related to approaching local matching of arriving Ga and As$_4$ at the droplet/nanowire interface in DCAPE mode, when the V/III ratio has been optimized for a certain T_{gr}. The normalized ratios of the growth rates for an optimal V/III ratio of 11.5 at T_{gr}=550 °C (sample D) are similar to those obtained in conventional MBE at T_{gr}=615 °C (star symbols). Thus, axial growth of straight non-tapered GaAs nanowire segments, that follow the shape of the template nanowires, was achieved in DCAPE mode at T_{gr} lower by 65 °C compared to conventional MBE due to enhanced delivery of Ga adatoms to the droplets at the nanowire tips. Moreover, DCAPE also results in a minimized radial growth compared to conventional MBE, since both Ga adatoms and As$_4$ molecules do not arrive simultaneously at the nanowire sidewalls.

Second, the dependence of the surface diffusivity of Ga adatoms on the growth temperature is studied. For this purpose, growth of short GaAs nanowire segments was performed in DCAPE mode at $T_{gr} < 550$ °C, in particular at T_{gr}=500 °C and 450 °C. The corresponding two nanowire samples are denoted as samples E and F, and their growth parameters are listed in Tab. 5.1. For the preparation of both samples, 3 μm long GaAs template nanowires were previously grown in conventional MBE. A V/III ratio of ∼3 had to be used for both samples in order to achieve local matching of the beam fluxes at the droplet/nanowire interface, and thus, elongation of template nanowires with uniform diameters as shown by the corresponding side-view SEM insets of Fig. 5.5. V/III ratios much lower or larger than ∼3 produced non-uniform nanowire segments with inversely tapered or tapered shape (thickening or thinning respectively). Compared to sample D at T_{gr}=550 °C, a lower optimal V/III ratio (or an increased amount of supplied Ga) is necessary to achieve beam flux matching. Furthermore, for lower growth temperatures, the formation of secondary Ga droplets at the bottom of the template nanowires was found in samples E and F as indicated by the arrows. Moreover, an increase in the amount of parasitic growth on the substrate surface was found. Both findings imply a reduced surface diffusivity of Ga adatoms on the substrate and nanowire sidewalls at T_{gr}=500 °C and 450 °C. Thus, a smaller arrival rate of Ga adatoms at the droplets requires an increased amount of supplied Ga (i.e. a higher Ga flux, and thus a lower V/III ratio) in order to compensate for the shorter diffusion lengths of Ga adatoms on the nanowire sidewalls at low T_{gr}. In fact, secondary Ga droplets are formed because the diffusion lengths of Ga adatoms on the nanowire sidewalls are shorter than the total nanowire lengths. Thus, Ga adatoms from the substrate do not contribute to nanowire growth since their delivery path, which is given by the distinct length of the template nanowires (here 3 μm), up to the droplets at the nanowire tips is too long.

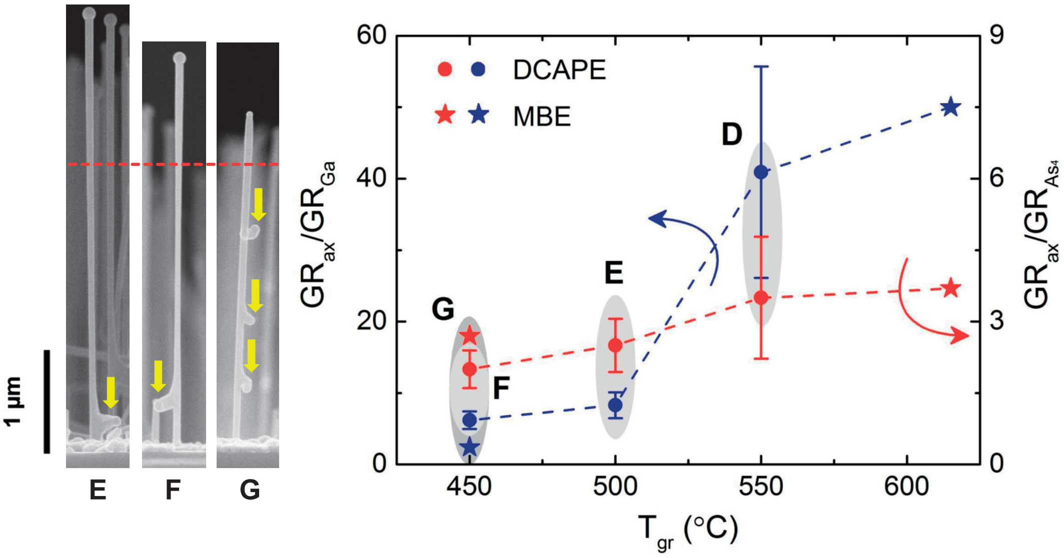

Fig. 5.5: Plot of the normalized growth rates GR_{ax}/GR_{Ga} (left axis) and GR_{ax}/GR_{As_4} (right axis) as a function of T_{gr} during DCAPE of GaAs nanowire segments under optimal V/III ratios (circles) in comparison with conventional MBE at 615 °C and 450 °C (stars). The shape of the nanowire segments grown in DCAPE mode at different T_{gr} is shown in the insets D to F, while it is presented for conventional MBE at 450 °C in inset G. The dashed line indicates the MBE/DCAPE interface. The yellow arrows indicate secondary Ga droplets on the nanowire sidewalls. Adapted with permission from [224]. Copyright (2016) American Chemical Society.

Equivalent to Fig. 5.4, the measured axial growth rate GR_{ax} of the nanowire segments was normalized to the growth rates of the direct Ga and As_4 beam fluxes GR_{Ga} and GR_{As_4}, and their dependencies on the growth temperature are illustrated in the plot in Fig. 5.5. As indicated, GR_{ax}/GR_{As_4} slightly drops with decreasing growth temperature, which is related to a reduction of the rebound As_4 flux at lower growth temperatures as evidenced from the larger substrate area covered by parasitic GaAs islands. Similarly, the decrease of GR_{ax}/GR_{Ga} with decreasing growth temperature again emphasizes a reduced surface diffusivity of Ga adatoms on the nanowire sidewalls at lower growth temperatures.

At low growth temperatures, radial growth on the nanowire sidewalls becomes more pronounced. This is evidenced from a decrease of the ratio of the axial and radial growth rates from GR_{ax}/GR_{rad}=185 at T_{gr}=615 °C in conventional MBE to GR_{ax}/GR_{rad}=60 at T_{gr}=450 °C in DCAPE mode. In other words, the axial growth at T_{gr}=450 °C is 60 times faster than the radial one, which still leads to a fairly unidirectional elongation of the template nanowires.

Finally, elongation of GaAs template nanowires was carried out at T_{gr}=450 °C in conventional MBE using continuous beam supply. The corresponding nanowire sample is denoted as sample G, and its growth parameters are additionally listed in Tab. 5.1. The purpose of this sample was to compare the surface diffusivity of Ga adatoms in conventional MBE and DCAPE mode at T_{gr}=450 °C. A very low V/III ratio of ∼1 in combination with reduced Ga and As_4 beam fluxes had to be employed in order to maintain a constant droplet size at the nanowire tips. The reduction of the beam fluxes was necessary to enhance the surface diffusivity of Ga adatoms in conventional MBE. As shown by the corresponding SEM inset of sample G in Fig. 5.5, a short tapered GaAs nanowire segment was obtained, and additionally, three secondary Ga droplets with equidistant spacing were found on the sidewalls of the template nanowires as marked by the arrows. The very low V/III ratio, the tapered segment shape and the secondary Ga droplets imply a very low arrival rate of Ga adatoms at the droplets at the nanowire tips. Moreover, radial growth of the template nanowires was further enhanced in conventional MBE as evidenced by the decrease of GR_{ax}/GR_{rad} to 25 in clear contrast to DCAPE at T_{gr}=450 °C. All those findings render elongation of GaAs template nanowires in conventional MBE at 450 °C impossible because of the restricted Ga adatom surface diffusivity.

5.3.3 Surface Diffusion Lengths of Ga Adatoms

Secondary Ga droplets only were created in samples E and F, in which the surface diffusion lengths are shorter than the total nanowire lengths (see corresponding SEM insets in Fig. 5.5). By measuring the distances between the Ga droplets at the nanowire tips and the secondary droplets on the nanowire sidewalls, the surface diffusion lengths of Ga adatoms were estimated. Figure 5.6 shows the measured average surface diffusion length λ_{Ga} of Ga adatoms obtained in DCAPE mode (circles) and conventional MBE (stars) in comparison with calculated λ_{Ga} for planar growth of GaAs epilayers on GaAs($1\bar{1}0$) facets (squares, taken from Ref. [230]) as a function of $1/kT_{gr}$ and T_{gr} respectively. For samples grown at $T_{gr} \geq 550$ °C, in which no secondary droplets were found due to longer λ_{Ga} compared to the total nanowire lengths, λ_{Ga} could not be measured directly, but was rather estimated (framed symbols). To deduce λ_{Ga} at T_{gr}=550 °C and 615 °C, the measured value of λ_{Ga} at T_{gr}=500 °C was multiplied by a factor of 5 and 6 respectively. These factors were obtained from the ratios of GR_{ax}/GR_{Ga} at T_{gr}=550 °C and 500 °C (factor of 5) and T_{gr}=615 °C and 500 °C (factor of 6) in the plot of Fig. 5.5. Estimated values of λ_{Ga} at $T_{gr} \geq 550$ °C include the contributions from the substrate as well as from the nanowire sidewalls, whereas measured values of λ_{Ga} at $T_{gr} < 550$ °C solely contain the contribution from the nanowire sidewalls.

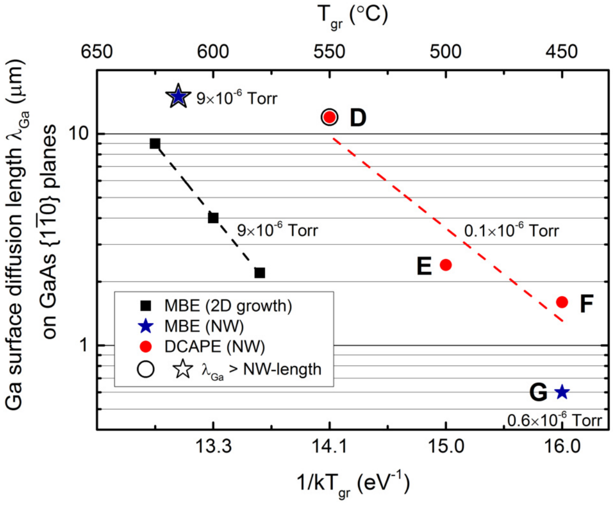

Fig. 5.6: Plot of the surface diffusion length λ_{Ga} of Ga adatoms on GaAs$\{1\bar{1}0\}$ planes of the nanowire sidewalls as a function of $1/kT_{gr}$ (bottom axis) or T_{gr} (top axis) in DCAPE mode (circles) and conventional MBE (stars) in comparison with planar MBE of GaAs epilayers (squares). Data points depicted by squares were taken from Ref. [230].

As indicated in Fig. 5.6, similar λ_{Ga} in the range of ∼1.6 to 12 μm were obtained in DCAPE mode compared to planar growth of GaAs epilayers (for similar As_4 BEP), but at much lower T_{gr} in the range of 450 to 550 °C. A further reduction of λ_{Ga} at T_{gr}=450 °C by a factor of 3 was measured when elongation of GaAs template nanowires was performed in conventional MBE at 450 °C (sample G). All those findings manifest that DCAPE provides an enhanced Ga adatom surface diffusivity at low growth temperatures. Therefore, a targeted delivery of Ga adatoms to the droplets at the nanowire tips cannot only be realized in conventional MBE under continuous beam supply at high-enough growth temperatures, but also by pulsing and interrupting the beams in DCAPE mode in combination with lower growth temperatures. All results highlight the enormous potential of the novel growth technique for low-temperature and CMOS-compatible integration of GaAs-based nanowires on the industrial Si platform.

5.3.4 Crystal Structure of GaAs Nanowires

In the following section, the crystal structure of GaAs nanowire segments grown in DCAPE mode is evaluated. For this purpose, a detailed TEM study was performed on various nanowire samples. As presented in Chapter 5.3.2, local matching of arriving Ga and As_4 at the nanowire tips is necessary in order to maintain a constant size of the Ga droplets and to obtain GaAs nanowire segments with a uniform diameter. On the other hand, deviation from local beam flux matching at the droplets results in non-uniform (inversely) tapered nanowire segments. This TEM study concerns the investigation of the effect of the size and contact angle of the Ga droplets on the crystal structure of the nanowire segments. This is achieved by deliberate variation of the arrival rates of Ga and As_4 at the droplets in DCAPE. For this purpose, two nanowire samples denoted as samples H and I were grown at T_{gr}=500 °C under almost identical conditions. Only the amount of offered As_4 per pulse was increased slightly from Θ_{As_4}=0.06 ML/pulse in sample H to 0.08 ML/pulse in sample I as indicated in Tab. 5.1. The purpose of sample I was to reduce the size and contact angle of the Ga droplets intentionally compared to sample H, while keeping GR_{ax} fairly constant, which required a minor imbalance of the arriving Ga and As_4 at the droplets. Thus, a larger Θ_{As_4} (or equivalently, V/III ratio) should lead to an increased incorporation of Ga atoms into the nanowire crystal, and consequently, to a smaller size and contact angle of the Ga droplet at the nanowire tip. In both samples, the size and contact angles of Ga droplets present at the nanowire tips were analyzed from side-view HRTEM images, and then correlated with the crystal structure of the nanowire segments. Side-view HRTEM images of representative GaAs nanowires of both samples are depicted in Figs. 5.7 (a)-(c). Only the DCAPE segments are shown.

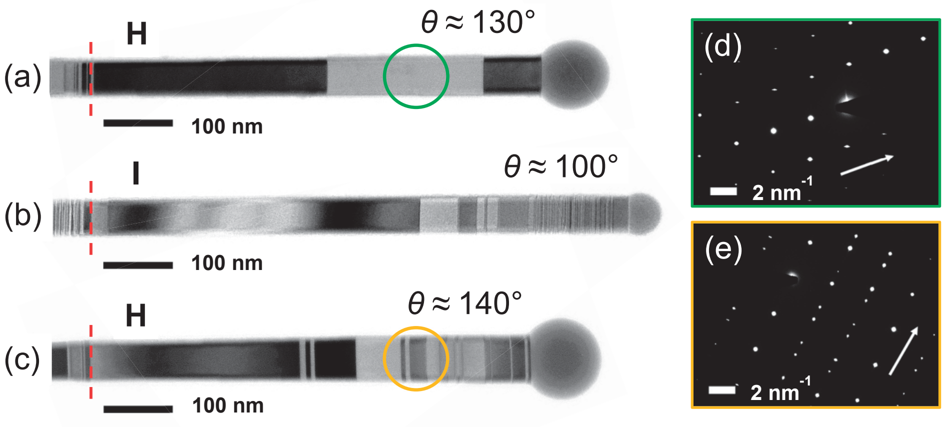

Fig. 5.7: Impact of the size and contact angle of the Ga droplet on the crystal structure of GaAs nanowire segments grown in DCAPE mode at 500 °C. (a)-(c) Side-view TEM images of representative GaAs nanowire segments of sample H (a), (c) and sample I (b). A contact angle θ of the Ga droplet of ~130° was measured in (a), ~100° in (b) and ~140° in (c). (d), (e) SAED patterns of (d) single and (e) twinned ZB crystal structure of GaAs nanowire segments in (a) and (c). Both patterns were acquired along the [111] zone axis, which is indicated by the corresponding arrows.

In all samples, a ~50 nm defective segment was found in the middle region of the nanowires (template+DCAPE). This defective segment serves as a marker in the TEM study and its top end was defined as the position of the MBE/DCAPE interface, which is indicated by the dashed red lines in Figs. 5.7 (a)-(c). The origin of the defective segment is associated with a decreasing contact angle of the Ga droplets due to local changes in the effective V/III ratio at the nanowire tips, when conventional MBE was interrupted at the end of template growth. As demonstrated by Fig. 2.18 (d) in Chapter 2.5.3 or Fig. 4.23 (f) in Chapter 4.3.5, the length of the defective segment at the end of template growth is equal to ~10 nm. Thus, it must have increased by

∼40 nm, when growth in DCAPE mode was resumed. This is related to an increase in the contact angle of the droplets until a critical value for defect-free growth has been reached again. The ∼40 nm defective segment in the beginning of DCAPE was neglected in the analysis of the lengths and growth rates of the DCAPE segments. A detailed description of the crystal structure of the template nanowires is provided in Chapter 4.3.5.

The crystal structure of two representative DCAPE segments of sample H is shown in the side-view TEM images of Figs. 5.7 (a) and (c). Both types of nanowires were found in the same sample. The DCAPE segment shown in Fig. 5.7 (a) exhibits a pure ZB phase and only two rotational TPs are present along the axis of the nanowire segment as evidenced from the corresponding SAED pattern shown in Fig. 5.7 (d) and the contrast changes in the TEM image. The Ga droplet at the nanowire tip exhibits a contact angle of ∼130°. The low formation rate of TPs is attributed to a fast stabilization of the contact angle above a critical value after nanowire growth was resumed in DCAPE. A constant contact angle could be maintained throughout the entire DCAPE process because the effective incoming flux of Ga at the droplet matched very well with that of As_4. This finding clearly demonstrates the possibility for SF-free growth of GaAs nanowire segments in DCAPE under well-matched conditions at the growth interface at a certain T_{gr} (beam flux matching depends on the growth temperature due to different contributions of the direct Ga/As_4 and the diffusion Ga/rebound As_4 beams to axial growth at various T_{gr}). In particular, this was achieved by a V/III ratio of 2.4 at T_{gr}=500 °C. For the first time, nearly twin-free growth of GaAs nanowire segments is demonstrated at growth temperatures as low as 500 °C. Thus, the value of $\theta = 130°$ is interpreted as an optimal contact angle for steady-state growth of defect-free GaAs nanowires. For well-matched arrival rates of Ga and As_4, the DCAPE segment does not exhibit a higher number of TPs at its tip underneath the Ga droplet, which further demonstrates the unique possibility to interrupt or terminate nanowire growth without formation of planar defects. This finding is in clear contrast to nanowire growth in conventional MBE and attributed to the fact that the background pressure of As_4 in DCAPE is significantly lower than that in conventional MBE, i.e. by two orders of magnitude. As a result, pumping of residual As_4 out of the growth chamber upon closing the As shutter and valve is much faster in DCAPE and no defective GaAs is formed at the nanowire tips.

In contrast, the DCAPE segments shown in Figs. 5.7 (b) and (c) reveal contact angles θ of the droplets at the nanowire tips smaller or larger than ∼130°. The DCAPE segment of sample I in Fig. 5.7 (b) exhibits a large number of planar defects in the upper part and a contact angle of the droplet of $\theta \approx 100°$ was measured at the nanowire tip. It is worth to note that Θ_{As_4} has been slightly increased prior to growth of the segments in order to reduce the size and contact angle of the droplet at the nanowire tip on purpose compared to sample H (deviation from local matching of Ga and As_4 at the droplet was intended). Due to a larger incorporation rate of Ga atoms in the nanowire crystal at a constant arrival rate of Ga at the droplet by increased amount of supplied As_4, the size and contact angle of the droplet must have decreased gradually from $\theta \approx 130°$ for twin-free growth of the lower part of the segment (as shown in Fig. 5.7 (a)) to $\theta \approx 100°$ during growth of the upper part. The continuous decrease of the contact angle resulted in the formation of numerous TPs, SFs and short sections of ZB/WZ polytypes. The smaller the contact angle of the droplet within this range, the higher is the number density of planar defects inserted along the nanowire axis. As a side effect, the axial growth rate slightly increased from GR_{ax}=0.56 ML/s in sample H to GR_{ax}=0.58 ML/s in sample I since Θ_{As_4} is the basic parameter that determines the axial growth rate at a fixed growth temperature. Despite the decrease of the contact angle, the diameter did not change along the nanowire axis. This is in good agreement with findings reported in Ref. [124]. Following Ref. [124], the nanowire diameter should decrease for contact angles $\theta \approx 90°$.

The second type of DCAPE segments found in sample H (Fig. 5.7 (c)) exhibits a twinned ZB crystal structure with an increasing number of TPs along the growth direction as demonstrated by the corresponding SAED pattern shown in Fig. 5.7 (e) and the contrast changes in the TEM image. The first ~300 nm of the segment grew without formation of TPs (like the segment shown in Fig. 5.7 (a)), whereas TPs were created in the residual ~300 nm long segment. The Ga droplet at the nanowire tip provides a contact angle of $\theta \approx 140°$. Although both nanowires originate from the same sample, local fluctuations of the effective V/III ratio at the droplet took place, which affected its size and contact angle. Consequently, the arrival rate of Ga at the droplet must have increased continuously at the droplet starting in the center of the segment compared to As$_4$ due to an increasing contact angle from $\theta \approx 130°$ (as determined for twin-free growth in Fig. 5.7 (a)) to $\theta \approx 140°$ at the nanowire tip. Within this small range of contact angles, the number density of TPs has increased significantly, which indicates a high sensitivity of the crystal structure of the nanowires to minor changes of the contact angle. This finding implies a slight deviation from excellent matching of arriving Ga and As$_4$ at the droplet (i.e. more Ga arrives at the droplets compared to As$_4$). To the best of my knowledge, this is the first experimental demonstration of TP formation in GaAs nanowires for contact angles $\theta > 130°$, which is in excellent agreement with theoretical explanations reported in Ref. [124]. An increasing droplet size and contact angle with time are further evidenced from an increased diameter of the nanowire segment at the tip. A slightly increasing droplet size and, thus, nanowire diameter for $\theta \gtrsim 130°$ has been also reported in Refs. [91] and [124].

Similar results were obtained for DCAPE of GaAs nanowire segments at T_{gr}=450 °C (sample F). A corresponding side-view TEM image of a DCAPE segment of sample F is depicted in Fig. 5.8 (a). For a detailed study the TP formation for contact angles $\theta > 130°$, the number of TPs was analyzed as a function of the length of the nanowire segments, and plotted in Fig. 5.8 (b) (left y-axis). For increasing imbalance of Ga and As$_4$ at the droplets (i.e. more Ga arrives at the droplets than As$_4$), two regimes are identified: the number of TPs increased with a low rate during the initial ~300 nm, and subsequently with a much faster rate (two different slopes). This finding implies a local variation of the growth conditions and thus, the axial growth rate. To reveal a dependence of the latter on the length of the nanowire segments, two more samples with shorter DCAPE segments denoted as samples J and K were grown at T_{gr}=450 °C, in which the number of pulses was reduced to N_{pulse}=262 in sample J, and to N_{pulse}=131 in sample K compared to sample F (N_{pulse}=525) under otherwise constant growth parameters (see Tab. 5.1).

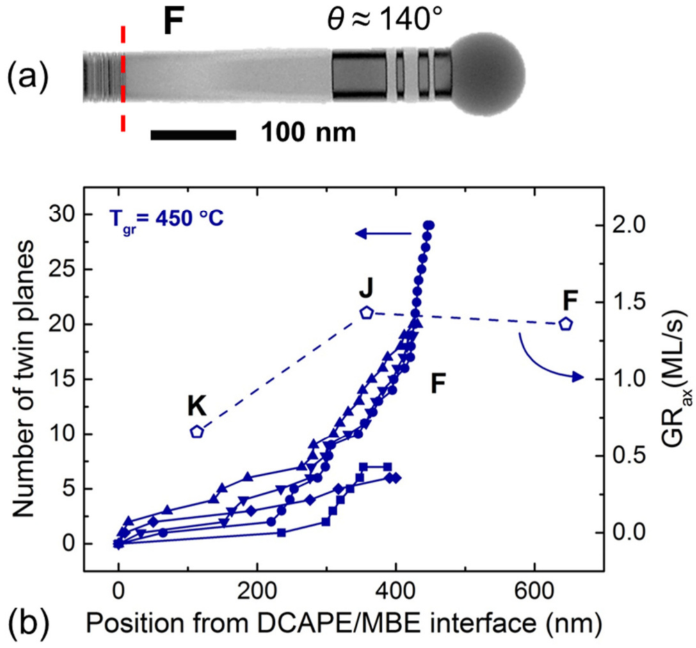

Fig. 5.8: (a) Close-up side-view TEM image of a representative GaAs nanowire segment grown in DCAPE mode at 450 °C. (b) Plot of the number of twin planes (left y-axis) and axial growth rate GR_{ax} (right y-axis) as a function of the length of the nanowire segments grown at 450 °C. Fig. 5.8 (b) is adapted with permission from [224]. Copyright (2016) American Chemical Society.

It was found that the axial growth rate increases with the length (or growth duration) of the nanowire segments in two modes as depicted in Fig. 5.8 (b) (right y-axis). That is, a low axial growth rate of GR_{ax}=0.7 ML/s corresponds to a smaller formation rate of TPs, whereas a high axial growth rate of GR_{ax}=1.4 ML/s is consistent with a higher formation rate of TPs. Hence, the evolution of the formation rate of TPs in two stages is correlated with the increase of the axial growth rate, which may arise from the increasing droplet diameter and contact angle and/or from an increasing arrival rate of As_4 provided by the rebound As_4 flux as a result of the increase of the surface collection area of the droplets [87, 90]. It should be possible to suppress TP formation even at T_{gr}=450 °C, if the effective arrival rates of Ga and As_4 at the droplets are well-tuned via beam fluxes and/or pulse durations in DCAPE.

Summarizing, it is concluded that the formation of TPs and SFs in the nanowire segments clearly correlates with the evolution of the contact angle of the droplets during nanowire growth. It has been further shown that local changes in the size and contact angles of the droplets also affect the axial growth rate. Finally, it is demonstrated that DCAPE is a very suitable growth technique to precisely control the contact angle of the droplets, and thus the crystal structure of the nanowires.

5.4 DCAPE of GaAs Nanowires Directly on Si

The second part of the DCAPE study concerns the nucleation stage of GaAs nanowires on Si substrates. For the growth study, the following samples were produced using the parameters as listed in Tab. 5.2. Prior to DCAPE, the *in situ* SMP was performed as described in Chapter 5.2 to create openings of controlled number density and size in the native-SiO$_x$ layer of the Si substrates. Subsequently, growth of GaAs nanowires was initiated by alternate beam pulsing of Ga and As in DCAPE mode. It is important to note that neither pre-deposition of Ga, nor growth of GaAs template nanowires in conventional MBE was performed prior to DCAPE.

Tab. 5.2: Parameters for growth of GaAs nanowires in DCAPE mode. F_{Ga} and F_{As} were calibrated for planar growth on GaAs(001) substrates. Θ_{Ga} and Θ_{As} are therefore given in equivalent thicknesses of planar GaAs(001). GR_{ax} has been determined from side-view length measurements of the nanowires.

Sample ID	As type	T_{gr} (°C)	$t_{int.}$ (s)	$t_{pulse(Ga)}$ (s)	$t_{int.}$ (s)	$t_{pulse(As)}$ (s)	N_{pulse}	F_{Ga} (ML/s)	F_{As} (ML/s)	Θ_{Ga} (ML/pulse)	Θ_{As} (ML/pulse)	V/III	GR_{ax} (ML/s)
L (D0429)	As_4	550	5	5	3	6	300	0.10	0.22	0.50	1.32	2.6	1.95
M (D0437)	As_2	550	5	5	3	6	300	0.10	0.22	0.50	1.32	2.6	1.84
N (D0212)	As_4	550	5	3	3	6	300	0.10	0.22	0.30	1.32	4.2	1.52

5.4.1 Impact of As Species on Ga Surface Diffusivity and Nanowire Shape

In this section, the feasibility of DCAPE for direct nucleation and growth of GaAs nanowires on Si substrates is tested. Moreover, the role of the employed arsenic species, in particular As_4 or As_2, on the surface diffusivity of Ga adatoms and shape of the nanowires is investigated. For this purpose, three nanowire samples denoted as samples L, M and N were grown in DCAPE mode on native-SiO$_x$/Si(111) substrates at T_{gr}=550 °C using the parameters summarized in Tab. 5.2. Samples L and M were prepared under exactly identical conditions, but a different type of arsenic species, i.e. As_4 in sample L and As_2 in sample M, was employed. Sample N was grown under supply of As_4 using almost identical parameters as compared to sample L. Only the amount of supplied Ga was lowered from Θ_{Ga}=0.5 ML/pulse in sample L to Θ_{Ga}=0.3 ML/pulse in sample N. This has been achieved by shortening the duration of the Ga pulse from 5 to 3 s. The purpose of sample N was the fine-tuning of Ga and As_4 beam fluxes for perfect matching of the effective arrival rates of Ga and As_4 at the droplets. Side-view SEM images of GaAs nanowire ensembles of the three samples are shown in Figs. 5.9 (a)-(c), respectively.

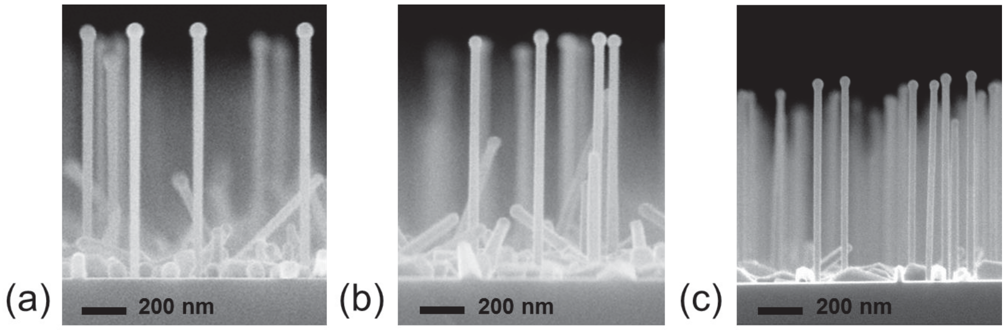

Fig. 5.9: Side-view SEM images of GaAs nanowire ensembles grown directly on native-SiO$_x$/Si(111) substrates at 550 °C in DCAPE mode under supply of As_4 in sample L (a) and N (c), and As_2 in sample M (b).

As can be seen, nucleation and growth of GaAs nanowires on native-SiO$_x$/Si(111) substrates in DCAPE mode was successful without the need for prior nucleation of GaAs template nanowires.

Direct nucleation and growth of GaAs nanowires at T_{gr}=550 °C required a V/III ratio of 2.6 in samples L and M and 4.2 in sample N. Therefore, an increased amount of Ga was necessary for direct nucleation of the nanowires on their substrate, since Ga droplets had to be created first on the substrate surface. This is unlike the simple elongation of pre-existing template nanowires in DCAPE mode (i.e. sample D), where a lower amount of Ga had to be employed (optimal V/III=11.5), since Ga droplets were already present at the tips of the template nanowires.

The comparison of samples L (As_4) and M (As_2) in Figs. 5.9 (a) and (b) reveals that the nanowire shape is the only difference between the two samples. More specifically, the nanowires of sample L exhibit a slight inversely tapered shape (average base and tip diameters of ∼40 nm and ∼50 nm) compared to the straight non-tapered shape in sample M (average diameter of ∼45 nm). This is a strong evidence that the size and contact angle of the droplets gradually increased during growth of the nanowires in sample L, which is attributed to not perfectly matching beam fluxes, i.e. a higher arrival rate of Ga at the droplets compared to As_4. Furthermore, this also explains why the Ga droplets in sample L are larger by 20% compared to sample M. On the other hand, the nanowires exhibit almost identical average lengths of 1.14 μm (GR_{ax}=1.95 ML/s) in sample L and 1.08 μm (GR_{ax}=1.84 ML/s) in sample M. It is worth to note that the variations in the nanowire shape between the two samples are exclusively attributed to the type of the employed arsenic species rather than the growth conditions, since both samples were prepared with the same amount of Ga and As per loop (i.e. Θ_{Ga}, Θ_{As_4}), and the same number of DCAPE loops (i.e. N_{pulse}). Moreover, the substrate surface area covered by parasitic GaAs islands has increased by 10% in sample M compared to sample L. Due to the enhanced parasitic growth of GaAs islands, the number density of vertical GaAs nanowires was difficult to determine, but estimated by one order of magnitude lower in sample M compared to sample L. All these findings imply that (i) the surface diffusivity of Ga adatoms on the substrate and the nanowire sidewalls is affected by the type of the employed arsenic species, i.e. a lower diffusivity for As_2, and (ii) the axial growth rate is independent of the type of the employed arsenic species. The lower surface diffusivity of Ga adatoms for As_2 may be attributed to an increased sticking of As_2 on the substrate and nanowire sidewalls compared to As_4. From vapor-solid growth of GaAs thin films on GaAs(001) substrates (Ga-rich conditions), it is known that the sticking coefficient of As_2 can reach unity ($S_{As2(max)}$=1), whereas that one of As_4 cannot exceed 0.5 ($S_{As4(max)}$=0.5) [78, 79]. On the other hand, the independence of the axial growth rate on the type of the employed arsenic species in the self-catalyzed VLS growth of GaAs nanowires is in clear contrast to vapor-solid growth of planar GaAs, where the larger sticking coefficient of As_2 on the substrate results in an increased (or doubled) growth rate of GaAs compared to As_4. This does not apply to self-catalyzed VLS growth of GaAs nanowires. Thus, it is suspected that the growth mechanism of self-catalyzed GaAs nanowires is independent and decoupled from the type of the employed arsenic species.

Finally, after fine-tuning of the Ga and As_4 beam fluxes in sample N for a perfect matching of the effective arrival rates of Ga and As_4 at the droplets, the inverse tapering of the nanowires in sample L could be fully eliminated and a uniform diameter across the length of the nanowires was obtained as shown in Fig. 5.9 (c). In fact, thinner and shorter nanowires with an average diameter of ~35 nm and an average length of 0.89 μm were grown compared to the nanowires in sample L, which is attributed to the lower axial growth rate of GR_{ax}=1.52 ML/s as a result of smaller Ga droplets (decreased amount of supplied Ga per pulse).

5.4.2 Crystal Structure of GaAs Nanowires

The following section presents the structural analysis of GaAs nanowires of samples L (As_4), M (As_2) and N (As_4), respectively. More specifically, it is investigated, whether the type of the employed arsenic species has an effect on the crystal structure of the nanowires. For this purpose, the crystal structure of several nanowires of samples L, M and N was analyzed by TEM, and overview TEM images of representative nanowires are shown in Figs. 5.10 (a)-(c), respectively. Close-up HRTEM images of selected sections of the nanowires in Figs. 5.10 (a)-(c) denoted as regions 1 to 6 are presented in Figs. 5.10 (d)-(i), respectively.

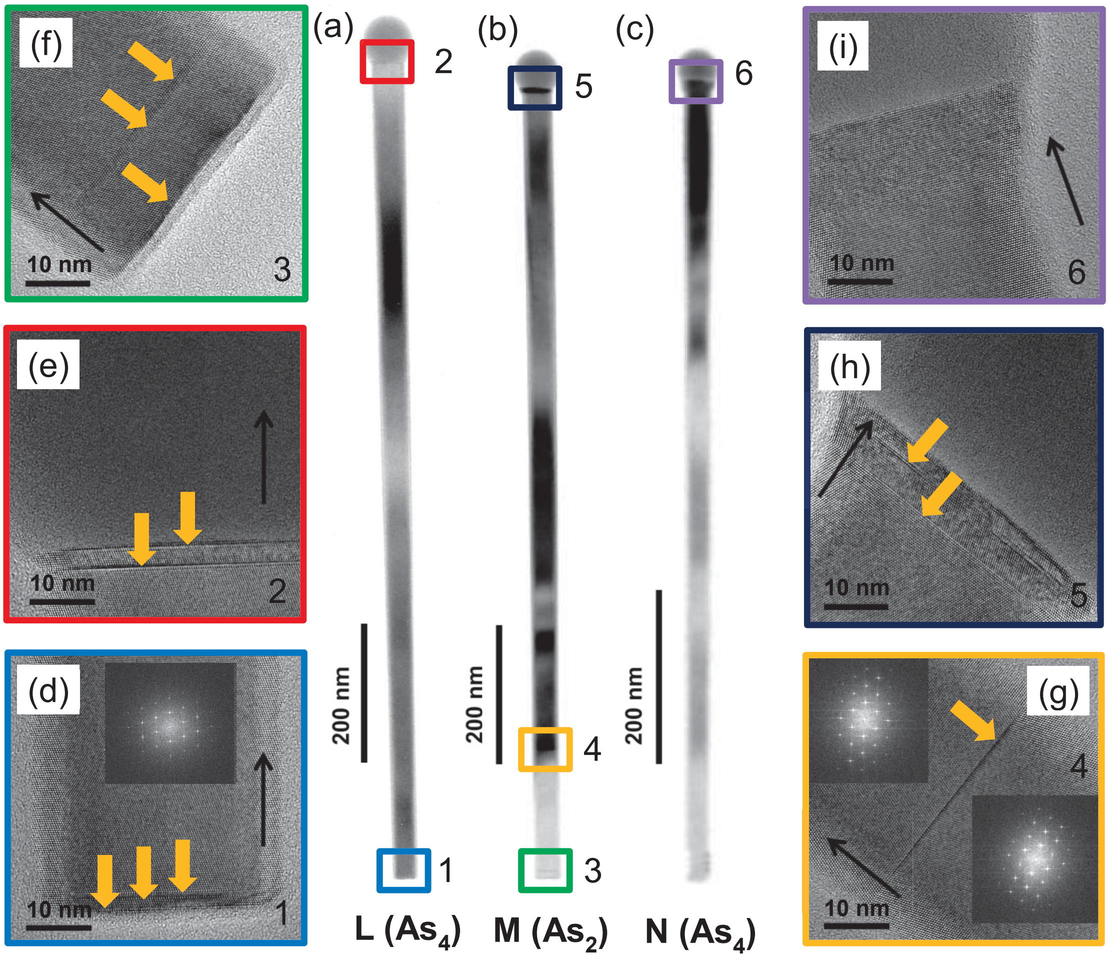

Fig. 5.10: Side-view TEM images of GaAs nanowires of samples L (a), M (b) and N (c) grown in DCAPE mode at 550 °C under supply of As_4 in (a) and (c), and As_2 in (b). Selected nanowire sections are denoted as regions 1 and 2 in (a), regions 3, 4 and 5 in (b), and region 6 in (c). (d), (e) Close-up HRTEM images of the base and tip (regions 1 and 2) of the nanowire shown in (a). (f), (g), (h) Close-up HRTEM images of the base, middle and tip (regions 3 to 5) of the nanowire presented in (b). (i) Close-up HRTEM image of the tip (region 6) of the nanowire shown in (c). Fast Fourier transform analysis of the defect-free part of region 1 and region 4 is shown in (d) and (g), respectively that reveals single zinc blende phase. All stacking faults are indicated by yellow arrows. The growth direction is indicated by the black arrow.

As indicated in Figs. 5.10 (a)-(c), all nanowires reveal a superior structural quality independent of the type of the employed arsenic species. More specifically, the nanowires exhibit a pure ZB phase with only very few rotational TPs as revealed by HRTEM and FFT analysis. Those TPs, which were marked by yellow arrows, are mainly located at the base and the tip of the nanowires as shown in the close-up HRTEM images of regions 1, 2 and 3, 5 in Figs. 5.10 (d), (e) and (f), (h), respectively. The bases of the nanowires in Fig. 5.10 contain remarkably short defective sections in the range of 3 to 40 nm. In particular, only three TPs were found in the lower sections of the nanowires in Figs. 5.10 (a) and (b) as pointed out by the arrows in Figs. 5.10 (d) and (f). The nearly defect-free nucleation of the nanowires on their substrate in DCAPE mode leads to a remarkable improvement of the crystal structure of the lower sections of the nanowires compared to conventional MBE. For detailed investigations, the number of TPs was analyzed for several nanowires of samples L and M, and is plotted as a function of their lengths in Fig. 5.11. For comparison, the number of TPs found in GaAs nanowires grown in conventional MBE (nanowires were taken from sample D of Chapter 4, see Tab. 4.1) is additionally plotted in Fig. 5.11. It is important to recall that SiO_x openings were created in all three samples by the *in situ* SMP prior to nanowire nucleation and growth on Si substrates.

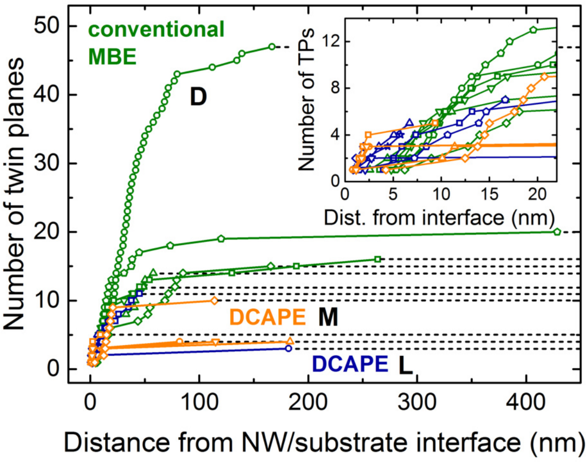

Fig. 5.11: Dependence of the number of twin planes in the base sections of GaAs nanowires on the growth method. Plot of the number of twin planes as a function of the length of the base sections of GaAs nanowires of sample D (Tab. 4.1) grown in conventional MBE, and of samples L and M grown in DCAPE under As_4 and As_2, respectively.

As indicated in Fig. 5.11, the number of TPs in the lower defective nanowire sections decreased significantly by a factor of ∼2 to 4, and the average length of the defective sections was reduced by a factor of at least ∼2, when growth was performed in DCAPE mode. More specifically, the number of TPs in the lower defective sections does not exceed 11 in all analyzed nanowires of samples L and M grown in DCAPE. On the contrary, nucleation and growth of GaAs nanowires in conventional MBE resulted in a larger number of TPs and longer defective base sections as shown in Fig. 5.11. This finding implies that the growth method must have a critical impact on the formation of Ga droplets, i.e. on their size and contact angle, in the nucleation stage of the nanowires on the substrate. A close-up view of the dependence of the number of TPs on the length of the lower defective parts is presented in the inset of Fig. 5.11. As shown, the onset of TP formation during growth of the first monolayers of GaAs in samples L and M is earlier, and their formation rates of TPs (i.e. slopes) are larger before they rapidly drop to zero, whereas the onset of TP formation is delayed in sample D, and its formation rate of TPs is slightly smaller and drops to zero in a later stage of the growth. Those findings imply that the Ga droplets, which were formed in DCAPE mode in the nucleation stage of the nanowires, grew already large enough in samples L and M prior to nanowire nucleation (in particular close to the critical value of the contact angle of $\theta \approx 130°$ for defect-free growth) to initiate nanowire nucleation on the substrate with such a low number of TPs. In other words, self-equilibration of the contact angle of the droplets during growth of the first monolayers of GaAs must be exceptionally fast, or the transition time/number of pulses, during which the critical contact angle for defect-free growth was achieved, is very short/small. For instance, already after three As_4 pulses, that correspond to the growth of a ~10 nm long defective section (GR_{ax}=3.6 nm/pulse) as shown in Fig. 5.10 (f), the Ga droplets must have reached a contact angle of $\theta \approx 130°$, and then drive the growth in stationary conditions without creating new TPs above the short base section. The formation of large enough Ga droplets at the onset of nanowire nucleation in DCAPE mode is further evidenced from the relatively large diameters of the nanowires, i.e. ~45 nm for a mean length of ~1 μm compared to ~50 nm thin and ~3 μm long nanowires obtained in conventional MBE, and may be attributed to the kinetics of droplet formation in DCAPE mode. It is suspected that larger droplets are formed prior to nanowire nucleation due to enhanced surface diffusivity of Ga adatoms in absence of As_4. However, further investigations are necessary to confirm that. The lower defective parts of the nanowires in Fig. 5.10 are followed by ~1 μm long defect-free sections. Only the nanowire in Fig. 5.10 (b) reveals one TP in the entire middle segment, which is shown in the close-up HRTEM image of region 4 in Fig. 5.10 (g). Fast Fourier transform analysis of selected areas of the HRTEM image below and above the individual TP clearly reveals single ZB phase as demonstrated in the corresponding FFT spectra in the insets of Fig. 5.10 (g). All described findings also are true for the majority of the investigated nanowires within each sample. The tips of the nanowires in Figs. 5.10 (a)-(c) exhibit very small defective parts, that contain only a few TPs, or a completely twin-free upper section with slightly larger diameter as shown in the close-up HRTEM images of Figs. 5.10 (e), (h) and (i). This is again a clear improvement of the crystal structure of the tip section compared to nanowires, which were grown in conventional MBE (see Figs. 2.18 (g), 4.23 (f), respectively). This finding is again attributed to a negligible continuation of the nanowire growth after closing the As valve and shutter as a result of the lower background pressure of As in DCAPE compared to conventional MBE. This is the first demonstration of nucleation and growth of self-catalyzed GaAs nanowires with excellent structural quality and high size uniformity directly on Si at unconventional, low growth temperatures.

5.5 DCAPE of Complex Nanowire Heterostructures on Si

The third part of the DCAPE study deals with self-catalyzed growth of axial nanowire heterostructures. Synthesis of axial nanowire heterostructures requires a modulation of the III-V material along the nanowire axis. In the present study, this is realized by inserting a group-III ternary alloy, in particular $Al_xGa_{1-x}As$, into the established GaAs binary system in order to grow axial GaAs/$Al_xGa_{1-x}As$ nanowire heterostructures. Aluminium has been chosen since the two end-point binary alloys AlAs and GaAs exhibit a negligible small lattice mismatch, which is suitable for growth of III-III-V ternary nanowire sections without accommodation of lattice strain at the binary/ternary interface.

The aim of this section is to study the axial growth of $Al_xGa_{1-x}As$ ternary alloys in free-standing GaAs nanowires using DCAPE. Moreover, the focus is on the investigation of the composition, interface sharpness and crystal structure of the binary/ternary nanowire heterostructures. As a first example, a thin $Al_xGa_{1-x}As$/GaAs/$Al_xGa_{1-x}As$ sequence is grown along the axis of an otherwise GaAs binary nanowire to form an axial quantum well (QW) structure. The short GaAs section with a lower band gap, that acts as the quantum well is sandwiched between two short $Al_xGa_{1-x}As$ sections with a higher band gap, that form the barriers perpendicular to the nanowire axis. If the GaAs/$Al_xGa_{1-x}As$ axial QW structure is embedded in a III-V material of a higher band gap, it forms a quantum dot-(QD-)in-a-wire structure. The concept of a QD-in-a-wire has been proposed for applications such as on-demand sources of single photons or polarization-entangled photons in quantum technology systems [12, 13, 14]. Another motive is the tuning of the optical properties of the QD by strain engineering. This can be realized by embedding the GaAs/$Al_xGa_{1-x}As$ axial QW structure in core-shell nanowires via radial overgrowth of the axial QW (core nanowire) with lattice-mismatched shells, such as $In_xGa_{1-x}As$ or $In_xAl_{1-x}As$. Recently, it has been shown that for thin-enough GaAs core nanowires (20-25 nm) and thick $In_xGa_{1-x}As$ or $In_xAl_{1-x}As$ shells (80 nm), the large misfit strain is fully accommodated in the core, producing a hydrostatic tensile-strained core, whereas the lattice-mismatched shells are fully relaxed [232]. The strain in the core can be engineered by variation of the shell thickness and composition, which is not possible in thin film growth. This approach allows one to reduce the band gap of GaAs up to 40%, and to shift the emission towards larger wavelength (i.e. the telecommunication range) [232].

To the best of my knowledge, only one detailed growth study has been reported so far that deals with self-catalyzed growth of GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures as outlined in Chapter 5.1 [167]. In this study, it has been demonstrated that interruption of all beam fluxes and filling of the Ga droplets with Al prior to growth of $Al_xGa_{1-x}As$ sections, where As is supplied separately, is an efficient approach to improve the abruptness of GaAs/$Al_xGa_{1-x}As$ interfaces (i.e. down to 2 MLs) [167]. Nevertheless, the $Al_xGa_{1-x}As$/GaAs interface with a gradient of approximately 10 MLs is still broad [167]. Sharp GaAs/$Al_xGa_{1-x}As$ interfaces are attributed to a higher bonding rate of Al with As (at least by two orders of magnitude) compared to the bonding rate of Ga with As [233], which leads to an energetically favored incorporation of Al from the droplet into the nanowire crystal as soon as Al and As are simultaneously present inside the droplets. In contrast, broad $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$/GaAs interfaces are the result of a local gradient in the Al-content until the main fraction of Al is consumed from the droplets after pre-filling. The thickness of the gradient depends on the equilibrium concentration of Al in the liquid, which is a function of the growth temperature [82]. The smaller the growth temperature, the smaller is the equilibrium concentration of Al in the droplet [82]. Thus, smaller equilibrium concentrations of Al in the liquid should enable growth of $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$/GaAs heterostructures with smaller Al gradients and sharper interfaces. Growth temperatures in the range of 590-610 °C have been used in this growth study [167]. In addition, Ga may be always incorporated into the nanowire crystal due to excess of Ga in the form of pure Ga catalyst droplets [82]. The incorporation of Ga into the crystal depends on the Al/As ratio and the phase diagram [82, 167]. Despite the sharpening of the GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ interface, the nanowires contain multiple SFs (i.e. TPs), that have been created most likely during growth interruptions in conventional MBE prior to filling of the Ga droplets with Al. Furthermore, we observe variations in the composition and thickness of the $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ insertions. The latter may be attributed to an unprecise control of the axial growth rate.

DCAPE appears very suitable to circumvent these issues in the growth of GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ axial nanowire heterostructures due to (i) the accurate control of the axial growth rate, allowing for the precise adjustment of the thickness of the heterostructure insertions, (ii) suppression of SF formation during growth interruptions, which enables defect-free growth, and (iii) the possibility for both sharp GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ and $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$/GaAs heterointerfaces due to beam flux interruptions and growth at lower temperatures, at which the equilibrium concentration of Al in the Ga droplets is smaller, and thus, the reservoir effect weak. On the other hand, self-catalyzed growth of $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ sections (barriers) with homogeneous Al distribution is expected to be challenging in DCAPE owing to the nature of the beam supply (short pulses). Instead, the $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ barrier is expected to be grown as a digital alloy that consists of short periodically alternating sections of Al-rich and Al-poor (Ga-rich) $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ alloys, where the number of periods is given by the number of Al pulses. Growth of short Al-rich $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ alloys inside the barrier is attributed to the higher bonding rate of Al with As compared to Ga with As as already discussed.

5.5.1 Axial GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ Quantum Wells

Droplet-confined alternate pulsed epitaxy of GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ axial nanowire heterostructures was performed directly on Si substrates at T_{gr}=550 °C. First, 500 nm long GaAs nanowires were grown in DCAPE as presented in Chapter 5.4 using T_{gr}=550 °C, V/III=2.6, GR_{ax}=1.95 ML/s, N_{pulse}=150 (similar to sample L in Tab. 5.2). The short length of the nanowires has been aimed for minimization of lateral growth on the nanowire sidewalls, and thus realization of thin enough nanowires for a radial confinement of the electrons. The GaAs nanowires are denoted as GaAs stems.

Subsequent to preparation of the nanowire stems, growth of an $Al_xGa_{1-x}As/GaAs/Al_xGa_{1-x}As$ axial QW structure was carried out. The pulse sequence of Ga, Al and As_4 beams for axial growth of the $Al_xGa_{1-x}As/GaAs/Al_xGa_{1-x}As$ QW structure is shown qualitatively in Fig. 5.12.

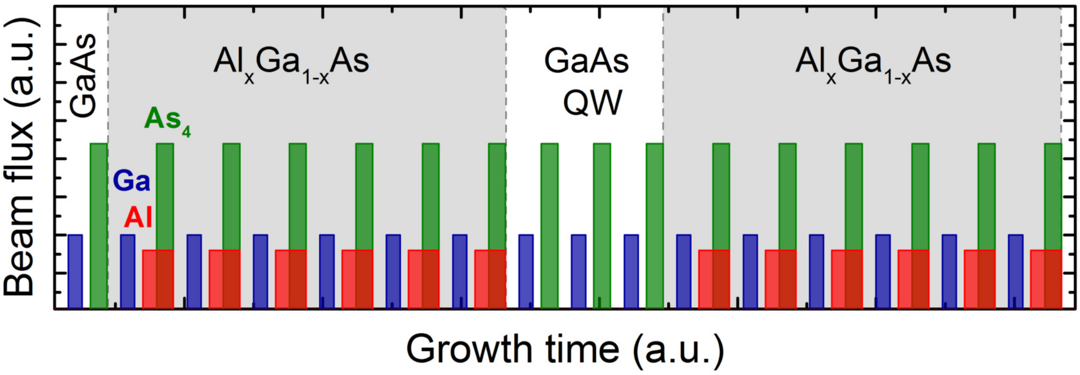

Fig. 5.12: Plot of the pulse sequence of Ga, Al and As_4 beams during self-catalyzed growth of $GaAs/Al_xGa_{1-x}As$ axial quantum wells in DCAPE mode.

For the first barrier, a 20 nm long $Al_xGa_{1-x}As$ section is grown by supplying Al pulses to the droplets in addition to Ga and As_4 pulses. All pulse parameters are given in Tab. 5.3. The Ga droplets are first pre-filled with Al by supplying Al alone, and then As_4 is supplied together with Al in order to incorporate the Al atoms from the Ga droplets into the nanowire crystals. The Al-content x_{Al} inside the $Al_xGa_{1-x}As$ sections depends on both the Al and the As_4 pulses (given the abundance of Ga), and is expressed by Eq. 5.5

$$x_{Al} = \frac{F_{Al} \cdot t_{pulse(Al)}}{GR_{ax} \cdot 1\ pulse}, \tag{5.5}$$

where F_{Al} is the Al flux, $t_{pulse(Al)}$ the duration of one Al pulse and GR_{ax} the axial growth rate. The latter is given by the product of the As_4 flux F_{As_4} and the duration of one As_4 pulse $t_{pulse(As_4)}$. One As_4 pulse with $t_{pulse(As_4)}$=6 s and F_{As_4}=0.22 ML/s results in an axial growth rate of GR_{ax}=3.3 nm/pulse or 10 ML/pulse as measured from side-view HRTEM images. The amount of supplied Ga in each Ga pulse (i.e. the duration of the Ga pulse $t_{pulse(Ga)}$) is doubled during growth of the $Al_xGa_{1-x}As$ section compared to the amount of Ga offered per pulse for growth of the nanowire stems. This is necessary in order to maintain the size and contact angle of the Ga droplets during growth of the barrier since Al provides an increased sticking and a lower surface diffusivity compared to Ga, and its presence on the substrate and nanowire sidewalls therefore leads to a decrease of the surface diffusion length λ_{Ga} of Ga adatoms [233]. The decrease of λ_{Ga} results in a lower arrival rate of Ga at the droplets, which was compensated by supplying more Ga in every Ga pulse. After the first barrier, a 10 nm long GaAs section (QW) is grown using identical pulse sequence and parameters as employed for the nanowire stems and N_{pulse}=3 for a 10 nm thin section. A second 20 nm long $Al_xGa_{1-x}As$ barrier is grown in order to complete the QW structure using the same pulse sequence and parameters as employed for the first barrier. After the second barrier, growth is terminated by rapid cooling of the substrate down to 400 °C.

Thus, the QW structure is located close to the tip of the nanowires. Axial QW nanowire samples denoted as samples O, P, Q, R and S with different thicknesses of the $Al_xGa_{1-x}As$ and GaAs sections d_{AlGaAs} and d_{GaAs}, respectively, and Al-content x_{Al} were prepared as summarized in Tab. 5.3. As-grown axial QW nanowires of sample O are depicted in the side-view SEM image in Fig. 5.13 (a). The nanowires reveal an average length of approximately 600 nm and diameter of approximately 50 nm as well as an excellent size uniformity due to highly synchronized nucleation of the nanowires on the substrates prepared by the SMP.

Tab. 5.3: Selected parameters for growth of the $Al_xGa_{1-x}As$ sections and measured properties of the QW structure grown in DCAPE mode. An As_4 flux of F_{As_4}=0.22 ML/s was used. A Ga flux of F_{Ga}=0.10 ML/s was used in samples O and P, and F_{Ga}=0.09 ML/s in samples Q, R, and S. All beam fluxes were calibrated for planar growth on GaAs(001) substrates. The Al-content x_{Al} has been determined by EDX element analysis in STEM mode. The axial growth rate GR_{ax}, the nanowire diameter d_{NW} and the thicknesses of the $Al_xGa_{1-x}As$ and GaAs sections d_{AlGaAs} and d_{GaAs}, respectively, were determined from side-view length measurements of the QW structure in HRTEM images.

Sample ID	F_{Al} (ML/s)	$t_{pulse(Al)}$ (s)	$t_{pulse(Ga)}$ (s)	$t_{pulse(Al+As_4)}$ (s)	$t_{pulse(As_4)}$ (s)	N_{pulse}	Al-content x_{Al}	GR_{ax} (nm/pulse)	d_{NW} (nm)	d_{AlGaAs} (nm)	d_{GaAs} (nm)	d_{AlGaAs} (nm)
O (D0454)	0.08	5	10	6	–	6	0.30 ±0.03	3.3	53	19	11	15
P (D0455)	0.05	5	10	6	–	6	0.16 ±0.03	3.3	54	21	10	17
Q (D0478)	0.11	6	2	–	3	10	0.38 ±0.03	1.7	54	18	5	13
R (D0485)	0.11	6	1.5	–	4	10	0.29 (nominal)	2.2	40	24	5	20
S (D0487)	0.11	6	2	–	4	10	0.29 (nominal)	2.2	–	–	–	–

In order to evaluate the composition and interface sharpness of the GaAs/$Al_xGa_{1-x}As$ axial QWs, HAADF-STEM and EDX analysis were performed. For those investigations, the nanowires were transferred from their substrate onto a carbon-coated TEM copper grid. All TEM studies were then carried out on selected nanowires. An overview HAADF-STEM image of a representative nanowire of sample O is shown in Fig. 5.13 (b). The contrast change in the tip region (marked region) clearly reveals a compositional change along the nanowire axis. Detailed compositional information of the tip region is provided by the close-up HAADF-STEM image in Fig. 5.13 (c) in combination with EDX element analysis in Fig. 5.13 (d).

As shown, a pure ∼10 nm thick GaAs QW and two $Al_xGa_{1-x}As$ barriers with thicknesses of ∼20 nm (lower barrier) and ∼15 nm (upper barrier) were grown in fairly good agreement with the target dimensions. Clearly, this is a result of the precise adjustment of the amount of supplied As_4 per pulse, when DCAPE is used.

The high-resolution HAADF-STEM image in Fig. 5.13 (c) indicates a fluctuation of the Al-content across the $Al_xGa_{1-x}As$ sections. As shown, the contrast within each $Al_xGa_{1-x}As$ section changes periodically and the number of periods is equal to the number of Al pulses (N_{pulse}=6). Al-rich $Al_xGa_{1-x}As$ corresponds to the darker contrast lines. As expected, the barriers were grown as a digital alloy, where the Al-rich $Al_xGa_{1-x}As$ segments form a superlattice inside the barriers. The modulation of the chemical composition along the growth axis in each barrier cannot be resolved in EDX element maps. Instead, only the average composition of the barriers can be measured. Thus, an overall Al-content of x_{Al}=0.30 ± 0.03 in both sections was determined by EDX spectroscopy as shown in Fig. 5.13 (d), which indicates a high uniformity of the average Al-content in both barriers.

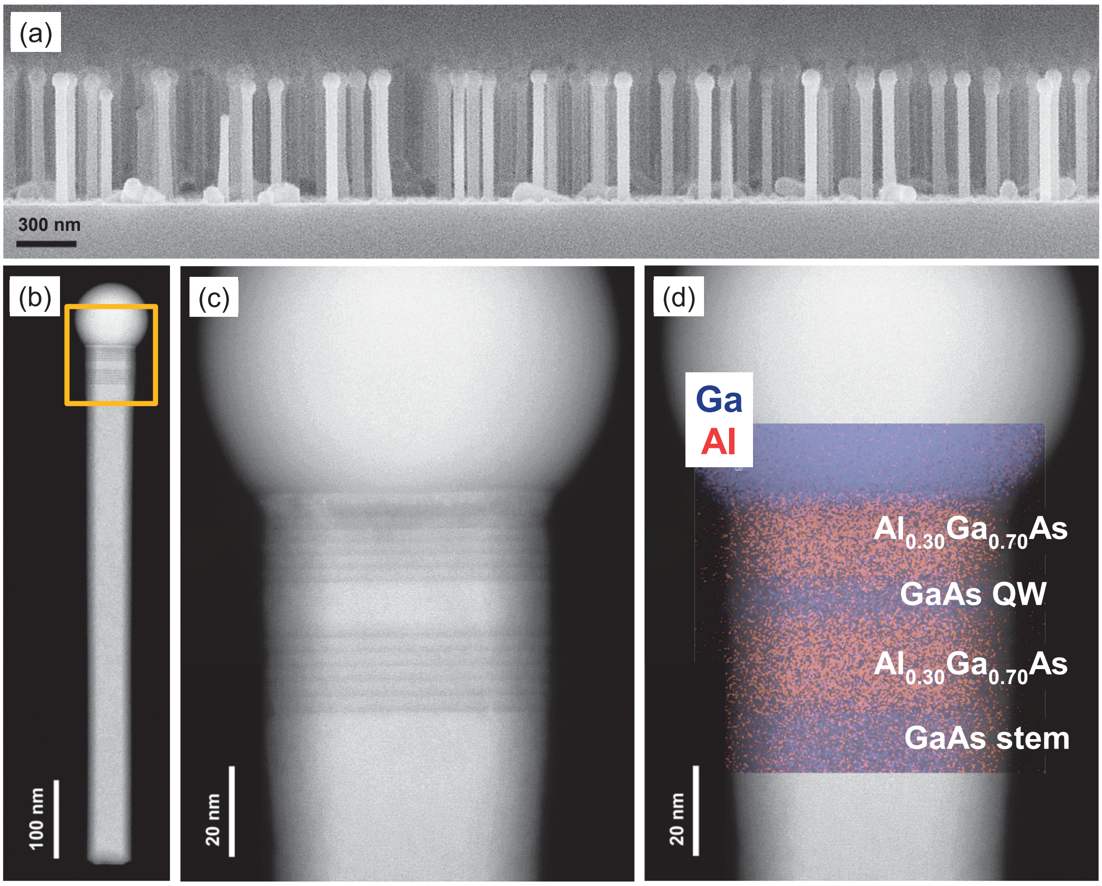

Fig. 5.13: Composition of GaAs/$Al_xGa_{1-x}As$ axial QW nanowires of sample O grown in DCAPE mode at 550 °C. (a) Side-view SEM image of the as-grown nanowires of sample O on native-SiO_x/Si(111) substrates. (b) Overview HAADF-STEM image of a representative nanowire with a GaAs/$Al_xGa_{1-x}As$ axial QW at the nanowire tip. (c) Close-up HAADF-STEM image of the tip region of the GaAs/$Al_xGa_{1-x}As$ QW nanowire. (d) EDX element map of the tip region of the GaAs/$Al_xGa_{1-x}As$ QW nanowire depicting the distribution of Ga and Al, respectively.

Although the growth of the two $Al_xGa_{1-x}As$ barriers was performed under identical conditions in all samples, they exhibit a small difference in thickness (see Tab. 5.3). It is speculated that this happened because of a continuous slight decrease of the droplet size and, thus, of the corresponding axial growth rate during the growth of the QW structure as a result of the decreased surface diffusivity of Ga after Al has been offered. Thus, the amount of supplied Ga per pulse (i.e. F_{Ga}) would have to be tuned continuously during growth of the QW structure in order to compensate for the reduced surface diffusivity of Ga in presence of Al, which is rather challenging. Nevertheless, DCAPE appears very suitable for growth of axial nanowire heterostructures due to fairly accurate control of the thicknesses of the heterostructure insertions. In order to examine the sharpness of the GaAs/$Al_xGa_{1-x}As$ and $Al_xGa_{1-x}As$/GaAs interfaces quantitatively, HAADF intensity measurements across the length of the QW structure would be necessary. Nevertheless, the GaAs/$Al_xGa_{1-x}As$ interface appears sharper compared to the $Al_xGa_{1-x}As$/GaAs interface, and the composition gradient across the interfaces is supposed to be less than 10 MLs (~3 nm) for both interfaces. The sharp interfaces are attributed first, to beam flux interruptions and filling of the droplets with Al prior to the As_4 pulse, and second, to growth at lower temperatures, at which the equilibrium concentration of Al in the liquid droplets is smaller, and the reservoir effect weak.

One way to control the average composition x_{Al} of the $Al_xGa_{1-x}As$ barrier is by changing the Al flux F_{Al} according to Eq. 5.5. This is demonstrated by sample P (see Tab. 5.3), in which a lower Al flux of F_{Al}=0.05 ML/s was employed compared to sample O under otherwise fixed pulse parameters. EDX spectroscopy of sample P reveals an average Al-content of the $Al_xGa_{1-x}As$ sections of x_{Al}=0.16 ± 0.03. A second possibility to control the average composition x_{Al} of the digital alloy is by varying the duration of the As_4 pulse $t_{pulse(As_4)}$. This results in a change of the axial growth rate GR_{ax} (see Eq. 5.5), and thus, a smaller or larger period of the superlattice. This is shown by sample Q (see Tab. 5.3), in which the axial growth rate was cut to half by shortening the duration of the As_4 pulse from $t_{pulse(As_4)}$=6 s in samples O and P to 3 s in sample Q. In order to maintain the target thickness of the barriers of d_{AlGaAs}=20 nm, the number of pulses was increased from N_{pulse}=6 to 10. Furthermore, the duration of the Ga pulse was reduced from $t_{pulse(Ga)}$=10 s in samples O and P to 2 s in sample Q in order to eliminate a slight inverse tapering of the nanowires during the growth of the GaAs/$Al_xGa_{1-x}As$ segments as observed in samples O and P. The tip region of a representative nanowire of sample Q is shown in the close-up HAADF-STEM image in Fig. 5.14 (a) together with EDX element analysis in Fig. 5.14 (b).

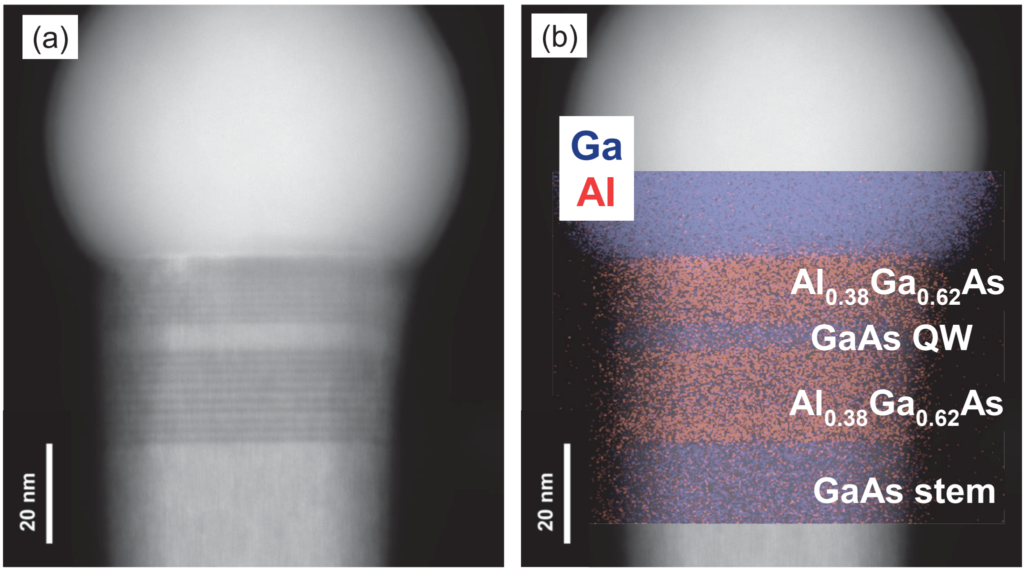

Fig. 5.14: Composition of the GaAs/$Al_xGa_{1-x}As$ axial QW nanowires of sample Q grown in DCAPE mode under reduced growth rate of 1.7 nm/pulse at 550 °C. (a) Close-up HAADF-STEM image of the tip region of the GaAs/$Al_xGa_{1-x}As$ QW nanowire. (b) EDX element map of the tip region of the GaAs/$Al_xGa_{1-x}As$ QW nanowire showing the distribution of Ga and Al, respectively.

As seen, a lower axial growth rate produces a shorter period of the Al-rich $Al_xGa_{1-x}As$ alloys with an average Al-content of the barrier of x_{Al}=0.38 ± 0.03. The increase of the overall Al-content from x_{Al}=0.16 in sample P to 0.38 in sample Q is not only attributed to the reduction of the axial growth rate, but also to the simultaneous increase of the Al flux from F_{Al}=0.5 ML/s in sample P to 0.11 ML/s in sample Q. As further shown, the thickness of the QW decreased from d_{GaAs}=10 nm in sample P to 5 nm in sample Q due to continuing the growth under reduced axial growth rate (N_{pulse}=3 at GR_{ax}=1.7 nm/pulse). For preparation of sample Q, the Ga droplets were pre-filled with Al for 6 s, and then As_4 alone was supplied for 3 s (i.e. $t_{pulse(Al+As_4)}$=0 s). This approach for growth of $Al_xGa_{1-x}As$ alloys is similar to what has been proposed by Priante *et al.* [167], and also produces remarkably sharp interfaces.

In order to evaluate the crystal structure of the GaAs/$Al_xGa_{1-x}As$ QW nanowires, HRTEM analysis was performed. An overview TEM image of a representative nanowire of sample O is depicted in Fig. 5.15 (a). In agreement with results presented in Chapter 5.4, the QW nanowire exhibits high crystal quality, and only a small number of TPs was found at the base of the nanowires. The origin of the short defective section is related to fast stabilization of the contact angle of already large enough Ga droplets during nanowire nucleation as described in Chapter 5.4.

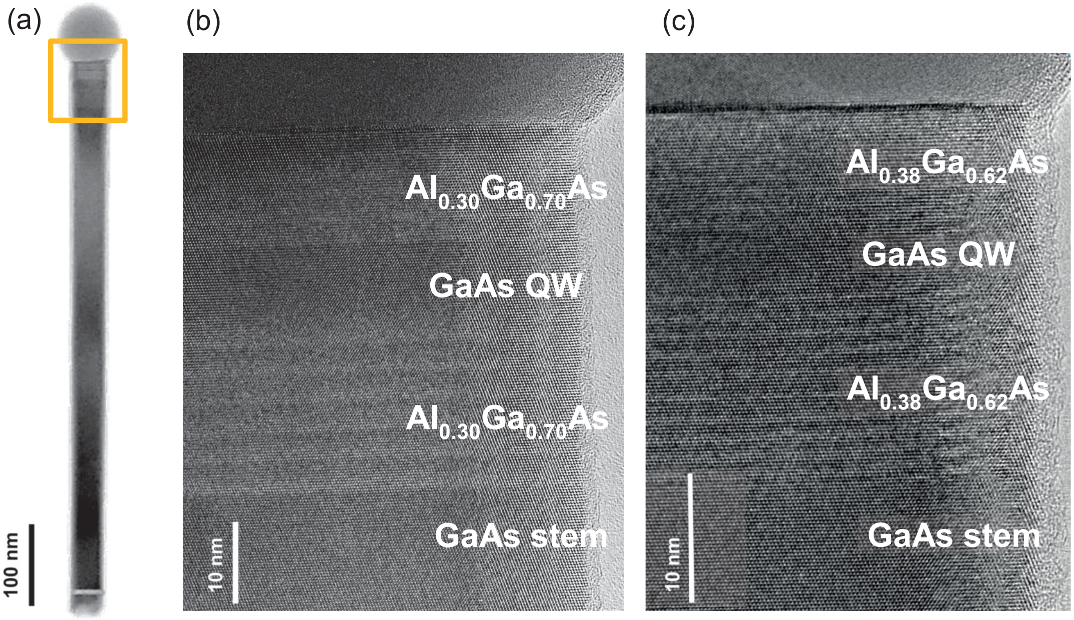

Fig. 5.15: Crystal structure of the GaAs/$Al_xGa_{1-x}As$ axial QW nanowires of samples O and Q grown in DCAPE mode at 550 °C. (a) Overview TEM image of a representative nanowire of sample O with a GaAs/$Al_xGa_{1-x}As$ axial QW at the nanowire tip. (b), (c) Close-up HRTEM images of the GaAs/$Al_xGa_{1-x}As$ QW structure at the tip region of the nanowires of samples O and Q, respectively.

Structural information of the axial QW at the tip region of the nanowires of samples O and Q is provided by the close-up HRTEM images in Figs. 5.15 (b) and (c), respectively. As shown, a perfect crystal structure free of any SFs and TPs is found at the tip regions of the nanowires. The $Al_xGa_{1-x}As$ barriers exhibit a crystal phase equivalent to the GaAs stem. Consequently, pure ZB phase and twin-free GaAs/$Al_xGa_{1-x}As$ QWs were successfully grown along the axis of GaAs nanowires at T_{gr}=550 °C. Twin-free growth of QW structures at the nanowire tips is again attributed to precise tuning of the contact angle of the Ga droplets, and thus, structural control in DCAPE mode. This is the first demonstration of self-catalyzed growth of pure ZB GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures without defects.

5.5.2 GaAs/Al$_x$Ga$_{1-x}$As Quantum Dots in In$_x$Al$_{1-x}$As Core-Shell Nanowires

Finally, the GaAs/Al$_x$Ga$_{1-x}$As axial QW nanowires are embedded as cores into core-shell nanowires to create QD-in-a-wire structures. The motivation is to tune the optical properties of the GaAs (QW) by application of strain to the core. As discussed in the introduction of Chapter 5.5, strain in GaAs core nanowires can be engineered by variation of the thickness and composition of thick lattice-mismatched In$_x$Ga$_{1-x}$As or In$_x$Al$_{1-x}$As shells that were grown on the sidewalls of the core nanowires [232].

Growth of core-shell nanowires was demonstrated with sample R. First, GaAs/Al$_x$Ga$_{1-x}$As axial QW nanowires were grown using identical DCAPE parameters as compared to sample Q (see Tab. 5.3). Only the duration of the As$_4$ pulse was increased from $t_{pulse(As_4)}$=3 s in sample Q to 4 s in sample R to reduce the average Al-content in the Al$_x$Ga$_{1-x}$As barriers by increasing the axial growth rate (see Eq. 5.5). The QW structure was grown as described in detail in Chapter 5.5.1. Second, a thick lattice-mismatched In$_x$Al$_{1-x}$As layer was conformally grown around the core to strain the GaAs QW. In$_x$Al$_{1-x}$As with a higher band gap than GaAs has been selected as shell material instead of In$_x$Ga$_{1-x}$As to avoid an overlap of emission lines in the PL spectrum since the band gaps of In$_x$Ga$_{1-x}$As and tensile-strained GaAs (QW) may exhibit a similar value (see Fig. 2.2).

The shell growth was performed as follows. After the second Al$_x$Ga$_{1-x}$As barrier, growth was interrupted by cooling of the substrate down to 370 °C with opened As shutter. This leads to prolonged axial growth of the core nanowires until the Ga droplets at their tips were consumed. After stabilizing the substrate temperature for 20 min, an In$_x$Al$_{1-x}$As shell with a target thickness of 40 nm and composition of x_{In}=0.40 was grown for 11.5 min by opening the In and Al shutters in addition to the As shutter. To avoid oxidation of the In$_x$Al$_{1-x}$As shell in atmosphere, a thin In$_x$Ga$_{1-x}$As capping layer was grown for 1.5 min to passivate the In$_x$Al$_{1-x}$As shell. In, Al, Ga and As fluxes of F_{In}=0.30 ML/s, F_{Al}=0.47 ML/s, F_{Ga}=0.45 ML/s and F_{As_4}=2.45 ML/s were used for shell growth. All beam fluxes were calibrated for planar growth on GaAs(001) substrates. The shell growth was terminated by closing the shutters. A representative core-shell nanowire with a GaAs/Al$_x$Ga$_{1-x}$As QD at the nanowire tip (marked region) is depicted in the overview HAADF-STEM image of Fig. 5.16 (a). The diameter of the QD is determined by the width of the nanowire core.

EDX analysis is performed in order to reveal the composition of the core-shell nanowires. EDX element maps of Ga and Al as well as In are shown in Figs. 5.16 (b) and (c), respectively. As indicated, the axial QW nanowires were successfully overgrown with a ∼50 nm thick In$_x$Al$_{1-x}$As layer with an average In-content of x_{In}=0.34 ± 0.03, and form a QD-in-a-wire structure. The In$_x$Al$_{1-x}$As shell is capped with a ∼6 nm thick In$_x$Ga$_{1-x}$As layer with an average In-content of x_{In}=0.34 ± 0.03. The average Al-content of the Al$_x$Ga$_{1-x}$As barriers was not possible to determine in this sample due to the shell growth, but is expected to be lower compared to sample Q (nominal value of x_{Al}=0.29) due to the larger axial growth rate. In addition, SFs were found close to the tip of the nanowires as indicated by the compositional fluctuations of In (i.e. In-poor lines perpendicular to the nanowire axis) in Fig. 5.16 (c). These SFs are attributed to a smaller droplet contact angle as a result of the slightly lower amount of Ga ($t_{pulse(Ga)}$=1.5 s) and increased amount of As_4 ($t_{pulse(Ga)}$=4 s) used for growth of the GaAs/$Al_xGa_{1-x}As$ QW in sample R compared to sample Q. It should be possible to suppress the formation of SFs during growth of the GaAs/$Al_xGa_{1-x}As$ QW by fine-tuning of the Ga and As_4 beam fluxes (V/III ratio) at the nanowire tips.

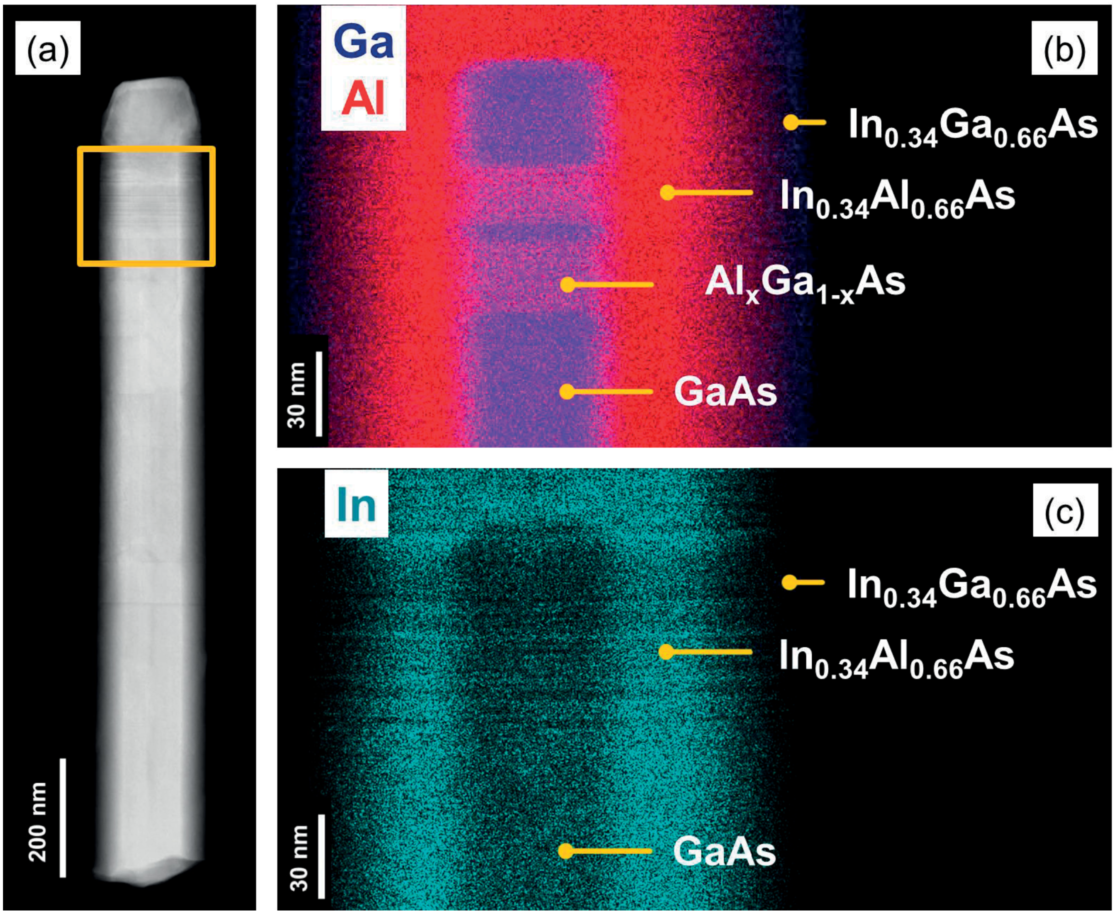

Fig. 5.16: Composition of GaAs/$Al_xGa_{1-x}As$ core-$In_xAl_{1-x}As$ shell nanowires of sample R. (a) Overview HAADF-STEM image of a representative core-shell nanowire with a GaAs/$Al_xGa_{1-x}As$ QD at the nanowire tip. (b), (c) EDX element maps of the tip region of the core-shell nanowire showing the distribution of Ga and Al in (b), and In in (c).

Photoluminescence spectroscopy was performed **in collaboration with Nikos T. Pelekanos and Nikos G. Chatzarakis** at the University of Crete, Heraklion, Greece to study the emission of the GaAs/$Al_xGa_{1-x}As$ QDs in the core-shell nanowires. For this purpose, sample S was grown using identical DCAPE parameters as compared to sample R. Only the duration of the Ga pulse was increased from $t_{pulse(Ga)}$=1.5 s in sample R to 2 s in sample S to suppress the formation of SFs during growth of the GaAs/$Al_xGa_{1-x}As$ QW. Consequently, it is assumed that the $Al_xGa_{1-x}As$ barriers and the $In_xAl_{1-x}As$ shell exhibit the same Al-content of x_{Al}=0.29 (nominal value) and In-content of x_{In}=0.34, respectively, as well as the same dimensions of the QW structure and shell thickness.

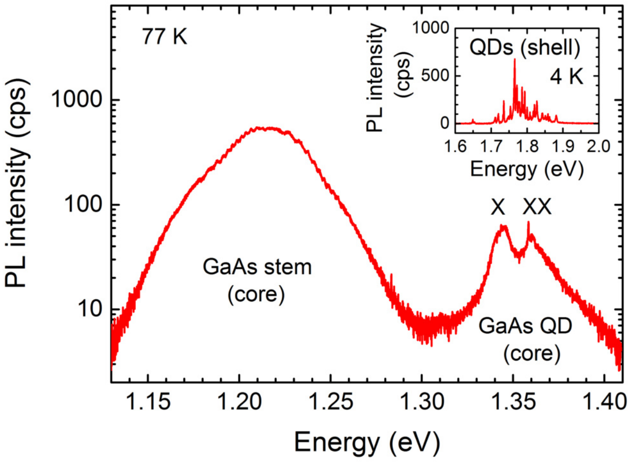

Fig. 5.17: Micro-PL spectrum of a single GaAs/Al_xGa_{1-x}As core–In_xAl_{1-x}As shell nanowire measured at 77 K showing emission at energies in the range of 1.13 to 1.41 eV. The inset shows additional PL emission at larger energies within a range of 1.6 to 2.0 eV measured at 10 K. The PL signal in the inset is plotted on a linear y-axis for a better visibility.

A representative micro-PL spectrum of a single GaAs/Al_xGa_{1-x}As core–In_xAl_{1-x}As shell nanowire of sample S measured at 77 K is shown in Fig. 5.17. As seen, the nanowire reveals emission at different energies. A relatively broad PL signal was measured at a photon energy of 1.22 eV, whose origin is attributed to recombination of excitons in the GaAs stem of the core nanowires. Furthermore, two relatively sharp emission features were detected at photon energies of 1.345 eV and 1.360 eV, respectively. Their origin is attributed to distinct biexciton (XX) and exciton (X) transitions in the 3D-confined GaAs QD embedded in the core-shell nanowire. In contrast, no PL signal was found at larger photon energies of approximately 1.52 eV, where emission from strain-free bulk GaAs at cryogenic temperatures is expected [117, 118]. These findings clearly demonstrate that the emission of GaAs was red-shifted by approximately 0.18 eV as compared to bulk GaAs. As a result, the emission of GaAs can be tuned in a wide range of wavelengths by application of strain to the GaAs/Al_xGa_{1-x}As QW nanowires. As additionally depicted in the inset of Fig. 5.17, multiple narrow PL lines were measured at photon energies in the range from 1.65 to 1.90 eV (the corresponding PL measurements were performed at Helmholtz-Zentrum Dresden-Rossendorf). These PL lines most likely originate from QD-like structures formed during the shell growth as a result of unintentional compositional fluctuations. Similar observations have been reported for Al_xGa_{1-x}As and $In_xAl_yGa_{1-x-y}$As shells [234, 235]. However, further investigations are necessary to confirm that.

5.6 Conclusions

A novel growth method based on alternate beam pulses of Ga and As_4 or As_2 has been developed for the self-catalyzed growth of GaAs nanowires and GaAs/Al_xGa_{1-x}As axial nanowire heterostructures on the Si platform. Droplet-confined alternate pulsed epitaxy is possible due to the atomic arrangement of the $\{1\bar{1}0\}$ nanowire sidewalls, which facilitates a low sticking of As in absence of Ga and a high surface diffusivity of Ga on the nanowire sidewalls in absence of

As. Perfect matching of Ga and As at the nanowire tips, that is achieved by fine-tuning of the beam fluxes and/or pulse durations, produces stable sizes of the Ga droplets and enables growth of GaAs-based nanowires with uniform diameters, while radial growth is strongly suppressed. DCAPE provides unique possibilities in the self-catalyzed growth of GaAs nanowires and GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ axial nanowire heterostructures compared to conventional MBE: (1) low growth temperatures in the range of 450 to 550 °C owing to the enhanced surface diffusivity of Ga and targeted delivery of Ga adatoms to the droplets, (2) compatibility with the Si-CMOS technology due to the low thermal budget, which enables monolithic integration of III-V nanowire-based devices on the industrial Si platform, (3) high structural quality even at low temperatures owing to the precise control of the droplet contact angle already from the early stage of growth, which allows nearly twin-free nucleation of the nanowires on their substrate, (4) accurate control of the axial growth rate due to the precise adjustment of the amount of supplied As in each pulse, which enables very low growth rates down to one monolayer per pulse, and thus, precisely controlled thicknesses of GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ segments in axial heterostructures, (5) stacking-fault-free growth terminations and interruptions, which lead to a high structural quality of the nanowires in the final stage of growth, and enable growth of digital alloys with controlled average Al-content after filling of the Ga droplets with Al, (6) relatively sharp GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ and $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$/GaAs interfaces owing to the weak reservoir effect at low growth temperatures, and (7) growth of complex nanowire heterostructures, i.e. highly strained GaAs/$\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ QDs in core-shell nanowires with tunable photon emission in a wide range of wavelengths.

6 Summary and Outlook

This dissertation has been focused on the bottom-up synthesis of free-standing GaAs-based nanowires on Si(111) substrates as potential building blocks for future (opto)electronic devices. Epitaxial growth of the nanowires on the substrate has been realized in the self-catalyzed vapor-liquid-solid mode using solid-source molecular beam epitaxy. In this work, Si(111) substrates covered by a thin native-SiO$_x$ layer were employed for nanowire growth. The two main goals of this dissertation were first, to overcome the existing challenges in the conventional growth processes by developing new methods for substrate preparation and nanowire growth, and second, to provide a fundamental understanding of the physical mechanisms involved in the self-catalyzed nucleation and growth of GaAs-based nanowires on the Si platform.

In Chapter 4, a novel method called surface modification procedure (SMP) has been introduced for the *in situ* preparation of the native-SiO$_x$/Si(111) substrates. Surface modification of the substrate was achieved by employing a pre-growth treatment of the substrate, that consists of three steps: (step-1) the first substrate annealing at high enough temperatures, (step-2) Ga deposition and droplet formation, (step-3) the second substrate annealing at high enough temperatures. The *in situ* SMP decouples the two roles of Ga droplets in the self-catalyzed growth of GaAs nanowires, which has not been demonstrated before. Decoupling was achieved by using different Ga droplets for each purpose. The first set of Ga droplets initiates the formation of nano-sized openings in the SiO$_x$ with controllable number density, while the second one assists the nucleation of GaAs nanowires inside these openings. A key step is the second substrate annealing to evaporate the first Ga droplets and to increase the size of the SiO$_x$ openings prior to nanowire growth. As a result, the number density and size of the SiO$_x$ openings can be controlled independently.

The SMP offers unprecedented possibilities in the self-catalyzed growth of GaAs nanowires on native-SiO$_x$/Si(111) substrates without *ex situ* substrate patterning or change of the growth conditions: (i) high synchronization of nucleation of the nanowires on their substrate, which in turn, produces highly uniform GaAs nanowire ensembles with a narrow (sub-Poissonian) length distribution, (ii) improved structural quality of the nanowires close to the interface with the substrate, (iii) high yields of vertical GaAs nanowires up to 80% owing to minimized parasitic growth of faceted GaAs islands, (iv) deliberate control of the number density of GaAs nanowires within three orders of magnitude, (v) independent control of the nanowire dimensions from their number density, and (vi) a high growth reproducibility. For the development of the SMP, we studied the nucleation kinetics of Ga droplets on SiO$_x$, the interaction between the Ga droplets and the SiO$_x$, and the growth of SiO$_x$ openings at high temperatures. The high synchronization of nanowire nucleation on the substrate allowed us to observe the effect of the so-called nucleation antibunching on the length distribution of GaAs nanowires. Our findings validate theoretical considerations about temporally anti-correlated nucleation events in VLS-grown III-V nanowires. For all these reasons, we propose the *in situ* SMP as a promising method for low-cost fabrication of GaAs nanowire-based devices on Si substrates. It is anticipated that the procedure is also applicable for growth of other types of nanostructures or III-V materials.

One constraint of the SMP is the incompatibility with the standard Si-CMOS platform owing to the thermal substrate annealing at high temperatures (approximately 780 °C) in SMP step-1 and step-3. For instance, substrate annealing may activate diffusion and redistribution of dopants in the substrate and built-in devices, which finally leads to device degradation or failure. An approach to increase the size of the SiO_x openings at lower annealing temperatures in step-3 may be the use of multiple sets of Ga droplets and/or a larger Ga droplets (higher Ga flux) in step-2. It has been reported that evaporation of Ga from SiO_x is already possible at temperatures of approximately 600 °C [221].

In Chapter 5, a novel growth method called droplet-confined alternate pulsed epitaxy (DCAPE) has been introduced for the self-catalyzed growth of GaAs nanowires and GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures on Si substrates. In contrast to conventional growth processes, nanowire growth was realized by alternate pulsing of the Ga and As beams. Due to the fact that the surface diffusivity of Ga adatoms on the nanowire sidewalls is enhanced in absence of As, axial growth is possible at lower temperatures (in the range of 450 to 550 °C), while radial growth on the nanowire sidewalls is not significant. Using DCAPE, for the first time, defect-free growth of pure zinc blende GaAs nanowires and embedded GaAs/$Al_xGa_{1-x}As$ quantum wells has been demonstrated.

DCAPE offers unique advantages in the self-catalyzed growth of GaAs-based nanowires compared to conventional growth processes: (i) CMOS-compatibility due to growth at unconventional, low substrate temperatures, (ii) accurate control of the axial growth rate down to one monolayer per As-pulse, (iii) precise control of the droplet size and contact angle from the early growth stage, which in turn, leads to an accurate control of the crystal structure for phase-pure and stacking-fault-free nanowires, (iv) defect-free growth interruptions are possible and lead to GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures with a perfect crystal structure, tunable Al-content in the $Al_xGa_{1-x}As$ segments and minimal interface gradients. In DCAPE, the $Al_xGa_{1-x}As$ segments can only be grown as digital alloys. The average Al-content could be precisely controlled via the period of the digital alloy. As a first example for axial nanowire heterostructures, growth of single $Al_xGa_{1-x}As$/GaAs/$Al_xGa_{1-x}As$ quantum wells at the tips of GaAs nanowires has been demonstrated. Finally, the quantum well nanowires had been overgrown with thick conformal $In_xAl_{1-x}As$ layers in a core-shell fashion to create complex quantum dot-in-a-wire structures. The thin core develops hydrostatic tensile strain owing to the large lattice-mismatch with the shell, and a significant red-shift of the emission of the GaAs quantum dot by 180 meV compared to a strain-free GaAs quantum well has been obtained. Strain-induced tuning of the band gap of GaAs is particularly interesting for telecommuncation photonics.

All results presented in Chapter 5 highlight the great potential of the pulsed epitaxy method for low-temperature and Si-CMOS-compatible growth of GaAs-based nanowires with excellent crystal quality. Therefore, we propose DCAPE as a promising approach for fabrication of GaAs-based (opto)electronic nanowire devices on the industrially well-established Si platform. This work provides a significant contribution towards CMOS-compatible monolithic integration of defect-free III-V semiconductors on the lattice-mismatched mature Si platform.

Future work could focus on the further development of DCAPE for growth of complex nanowire heterostructures. Various challenges still exist as described in the following. First, for quantitative analysis of the sharpness of the GaAs/$Al_xGa_{1-x}As$ and $Al_xGa_{1-x}As$/GaAs interfaces, atomically resolved measurements of composition profiles along the axis of the nanowire heterostructure are necessary. This requires acquisition of STEM-HAADF images with monolayer resolution and quantification of the image contrast (HAADF-intensity). Pre-requisites are a very clean sample and a microscope with a high lateral resolution. It is assumed that the growth of GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures at substrate temperatures lower than 550 °C should further improve the abruptness of the heterointerfaces. Second, the axial quantum wells can only be embedded at the tips of the nanowires as opposed to other positions along the nanowire axis, since elongation of the nanowires by subsequent growth of GaAs would also lead to an unintentional radial growth of GaAs on the nanowire sidewalls. This prevents the possibility to form a quantum dot-in-a-wire structure, and to tune the optical properties of GaAs in the core by strain engineering via lattice-mismatched shells. Third, the GaAs/$Al_xGa_{1-x}As$ axial nanowire heterostructures exhibited relatively large diameters in the range of 40 to 50 nm although the wires were already grown very short with an average length of 600 nm, and growth of thinner nanowires with diameters below 25 nm would be necessary for a better radial confinement of the electrons in the GaAs quantum dot nanowires. Fourth, micro-PL measurements revealed a relatively broad signal of high intensity from the GaAs stem of the core as well as multiple sharp lines from quantum dot-like structures most likely present in the shell. Their photon emission is not desired for application of the core-shell nanowires as single photon sources in (opto)electronic devices. It has been demonstrated that a reduction of the shell growth temperature leads to the suppression of compositional fluctuations, and thus, quantum dot-like structures in the shell [234]. Moreover, the GaAs stem in the core may be replaced by a thin $Al_xGa_{1-x}As$ stem, but its growth is very challenging due to a lower surface diffusivity of Al compared to Ga, which leads to strongly tapered $Al_xGa_{1-x}As$ nanowires with a Ga-rich core and an Al-rich shell [233]. Finally, the growth of a tapered nanowire tip acting as a waveguide would be necessary to increase the extraction efficiency of the photons emitted from the quantum dot [14]. This could be realized by growth of a slightly tapered $Al_xGa_{1-x}As$ tip at the nanowire core.

A Appendix

Derivation of Formula for the Calculation of the Real Droplet Radius from the Measured AFM Profiles

Formula 4.1 in Chapter 4, which describes the influence of the geometry of the AFM tip on the droplet shape, has been obtained by the derivation as follows.

Two different center positions of the AFM tip with respect to the center position of the Ga droplet are distinguished:
If the center position of the tip is higher than the center of the Ga droplet and $r + r_{tip} > h_{profile}$, the difference Δy has to be taken into account in determination of $h_{profile}$ according to Eq. A.1. The opposite case, i.e. $r + r_{tip} < h_{profile}$, is described by Eq. A.2.

$$h = r + r_{tip} - \Delta y \tag{A.1}$$

$$h = r + r_{tip} + \Delta y \tag{A.2}$$

The base width of the AFM profile $b_{profile}$ is larger by Δx_r and Δx_l on the right- and left-hand side of the actual droplet diameter $2r$ respectively. This difference is taken into consideration in the derivation of the droplet radius r by Eqs. A.3 and A.4

$$b_{profile_l} = r + r_{tip} + \Delta x_r, \tag{A.3}$$

$$b_{profile_r} = r + r_{tip} + \Delta x_l. \tag{A.4}$$

According to Eqs. A.3 and A.4, the overall base width $b_{profile}$ is given by

$$b_{profile} = 2r + 2r_{tip} + \Delta x_r + \Delta x_l. \tag{A.5}$$

Equations A.6 and A.7 describe the geometrical relation of the tilt angle γ and tapering angle φ of the AFM tip with respect to the droplet of radius r.

$$cos(\varphi + \gamma) = \frac{r}{r + \Delta x_{r1}} = \frac{r_{tip}}{r_{tip} + \Delta x_{r3}} \tag{A.6}$$

$$tan(\varphi + \gamma) = \frac{\Delta x_{r2}}{|\Delta y|} \tag{A.7}$$

Δx_{r1}, Δx_{r2}, and Δx_{r3} are additional variables, which are introduced here in order to describe the geometrical relation of the tilt angle γ and tapering angle φ of the AFM tip, in particular, for the right-hand side of the droplet as illustrated in Fig. A.1.

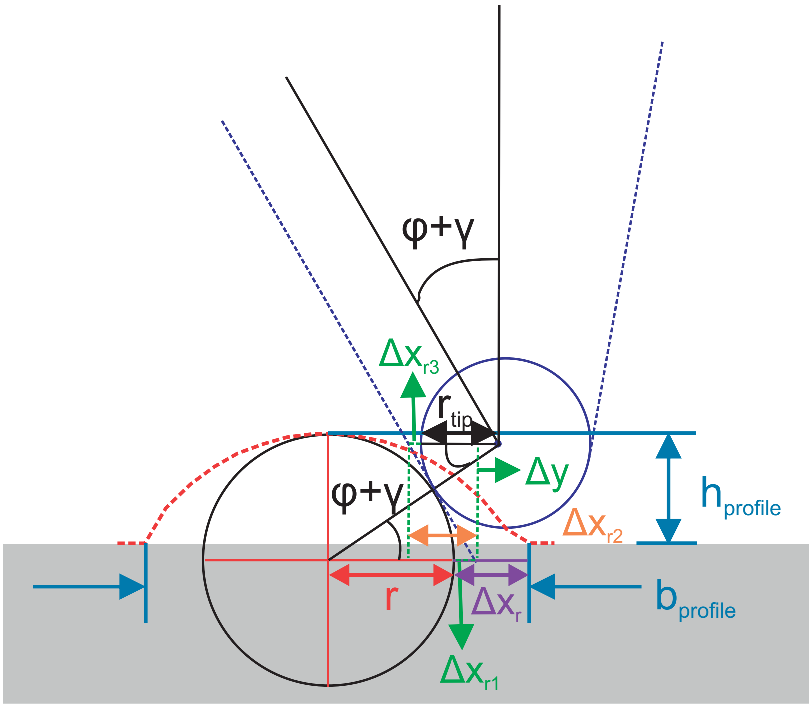

Fig. A.1: Derivation of geometrical relations between the AFM tip and a partially spherical Ga droplet on a substrate.

Finally, the base width of the AFM profile $b_{profile}$, which is measured larger by Δx_r compared the real droplet radius r (here for the right-hand side of the droplet) can be expressed by

$$\Delta x_r = \Delta x_{r1} + \Delta x_{r3} \pm \Delta x_{r2}. \tag{A.8}$$

The description of the mathematical relation of γ and φ of the AFM tip equally applies for the left-hand side of the droplet, and can be expressed analogously according to Eqs. A.9 and A.10

$$cos(\varphi - \gamma) = \frac{r}{r + \Delta x_{l1}} = \frac{r_{tip}}{r_{tip} + \Delta x_{l3}}, \tag{A.9}$$

$$tan(\varphi - \gamma) = \frac{\Delta x_{l2}}{|\Delta y|}. \tag{A.10}$$

Δx_l on the left-hand side of Fig. A.1 is described by

$$\Delta x_l = \Delta x_{l1} + \Delta x_{l3} \pm \Delta x_{l2}. \tag{A.11}$$

After description of the geometrical relation of the AFM tip with respect to the droplet using the defined variables, Eq. 4.1 presented in Chapter 4 is obtained as follows.

Equations A.6 and A.7 are solved with respect to Δx_{r1}, Δx_{r2} and Δx_{r3}.

$$\Delta x_{r1} = \frac{r}{cos(\varphi + \gamma)} - r \tag{A.12}$$

$$\Delta x_{r2} = |\Delta y| \cdot tan(\varphi + \gamma) \tag{A.13}$$

$$\Delta x_{r3} = \frac{r_{tip}}{cos(\varphi + \gamma)} - r_{tip} \tag{A.14}$$

Δx_{r1}, Δx_{r2}, and Δx_{r3} in Eq. A.8 are replaced by Eqs. A.12, A.13 and A.14 as follows.

$$\Delta x_r = r(\frac{1}{cos(\varphi + \gamma)} - 1) + r_{tip}(\frac{1}{cos(\varphi + \gamma)} - 1) \pm |\Delta y| \cdot tan(\varphi + \gamma) \tag{A.15}$$

Analogously, Δx_l can be expressed by

$$\Delta x_l = r(\frac{1}{cos(\varphi - \gamma)} - 1) + r_{tip}(\frac{1}{cos(\varphi - \gamma)} - 1) \pm |\Delta y| \cdot tan(\varphi - \gamma). \tag{A.16}$$

Δx_r and Δx_l in Eq. A.5 are replaced by Eqs. A.15 and A.16.

$$\begin{aligned} b_{profile} = 2r + 2r_{tip} + r(\frac{1}{cos(\varphi + \gamma)} - 1) + r_{tip}(\frac{1}{cos(\varphi + \gamma)} - 1) + r(\frac{1}{cos(\varphi - \gamma)} - 1) \\ + r_{tip}(\frac{1}{cos(\varphi - \gamma)} - 1) \pm |\Delta y| \cdot (tan(\varphi + \gamma) + tan(\varphi - \gamma)) \end{aligned} \tag{A.17}$$

Then, Eq. A.17 is solved with respect to $\pm|\Delta y|$.

$$\pm |\Delta y| = \frac{b_{profile} - 2r - 2r_{tip} - r(\frac{1}{cos(\varphi+\gamma)} + \frac{1}{cos(\varphi-\gamma)} - 2) - r_{tip}(\frac{1}{cos(\varphi+\gamma)} + \frac{1}{cos(\varphi-\gamma)} - 2)}{tan(\varphi + \gamma) + tan(\varphi - \gamma)} \tag{A.18}$$

$\pm|\Delta y|$ in Eqs. A.1 and A.2 is replaced by Eq. A.18, and $h_{profile}$ can be expressed by

$$h_{profile} = r + r_{tip} \pm \frac{b_{profile} - 2r - 2r_{tip} - r(\frac{1}{cos(\varphi+\gamma)} + \frac{1}{cos(\varphi-\gamma)} - 2) - r_{tip}(\frac{1}{cos(\varphi+\gamma)} + \frac{1}{cos(\varphi-\gamma)} - 2)}{tan(\varphi + \gamma) + tan(\varphi - \gamma)}. \tag{A.19}$$

Then, Eq. A.19 is solved with respect to r.

$$\begin{aligned} h_{profile} - r_{tip} - \frac{b_{profile}}{tan(\varphi + \gamma) + tan(\varphi - \gamma)} + \frac{2r_{tip}}{tan(\varphi + \gamma) + tan(\varphi - \gamma)} \\ + \frac{r_{tip}(\frac{1}{cos(\varphi+\gamma)} + \frac{1}{cos(\varphi-\gamma)} - 2)}{tan(\varphi + \gamma) + tan(\varphi - \gamma)} = r(1 - \frac{\frac{1}{cos(\varphi+\gamma)} + \frac{1}{cos(\varphi-\gamma)}}{tan(\varphi + \gamma) + tan(\varphi - \gamma)}) \end{aligned} \tag{A.20}$$

The droplet radius r is finally obtained by Eq. A.21, which has been used in order to calculate the real droplet radii r by taking into account the effect of the tip geometry on the droplet size, i.e. tip radius r_{tip}, the tapering angle φ and the tilt angle γ.

$$r = \frac{h_{profile} - \frac{b_{profile}}{tan(\varphi+\gamma)+tan(\varphi-\gamma)}}{1 - \frac{\frac{1}{cos(\varphi+\gamma)} + \frac{1}{cos(\varphi-\gamma)}}{tan(\varphi+\gamma)+tan(\varphi-\gamma)}} - r_{tip} \tag{A.21}$$

B List of Samples

Tab. B.1: List of samples used for preparation of this dissertation.

Chapter	Figure	Sample ID
2	2.5 (b)	D0301
	2.7 (b)	D0250
	2.13	D0126–D0129
	2.16 (c), (d)	D0321
	2.17 (b)	D0321
	2.18 (a)	D0126
	2.18 (b)–(g)	D0201
3	3.3 (b), (c)	D0297, D0219
4	4.2 (a)–(f)	batch A: #7_1, batch B: #9_7
	4.2 (g)	batch A: #7_1, batch B: #9_1
	4.5	D0232, D0235, D0237, D0238
	4.6	D0303, D0304
	4.8	D0173–D0177, D0198
	4.9 (a)–(c)	D0173, D0176, D0177
	4.9 (d)	D0173
	4.10 (a)	D0232
	4.10 (b)	D0190
	4.10 (c)	D0240
	4.10 (d)	D0232, D0240
	4.10 (e)	D0230
	4.10 (f)	D0236
	4.10 (g)	D0276
	4.11	D0301
	4.12	D0292–D0296
	4.13	D0188, D0201
	4.14	droplet samples: D0173–D0177, D0198 nanowire samples: D0179, D0180, D0182–D0184, D0199
	4.15	D0179, D0180, D0182, D0183
	4.16	D0242, D0244, D0245
	4.17	batch A: D0173–D0177, D0198 batch B: D0244, D0254, D0276, D0294
	4.18	batch A: D0179, D0180, D0182–D0184, D0189 batch B: D0239, D0242, D0244, D0245, D0271, D0274
	4.19 and 4.20	D0179, D0180, D0184, D0276, D0302
	4.21	D0179, D0180, D0184, D0239, D0253, D0276, D0302
	4.22	D0239, D0253, D0276, D0302
	4.23	D0276
	4.24	D0201, D0276
5	5.3 (a), (b)	D0276, D0243
	5.4	D0105, D0109, D0111, D0114, D0166
	5.5	D0114, D0139, D0155, D0157, D0166
	5.6	D0114, D0139, D0155, D0157, D0166
	5.7 (a), (c)	D0167
	5.7 (b)	D0164
	5.7 (d)	D0111
	5.7 (e)	D0155
	5.8 (a)	D0157
	5.8 (b)	D0157, D0164, D0167
	5.9	D0212, D0429, D0437
	5.10 (a), (d), (e)	D0429
	5.10 (b), (f)–(h)	D0437
	5.10 (c), (i)	D0212
	5.11	D0276, D0429, D0437
	5.13	D0454
	5.14	D0478
	5.15 (a), (b)	D0454
	5.15 (c)	D0478
	5.16	D0485
	5.17	D0487

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Figures

Tables

Abbreviations

Abbreviation	**Explanation**
1D	one-dimensional
AFM	atomic force microscopy
BEP	beam equivalent pressure
c-AFM	conductive atomic force microscopy
CMOS	complementary metal-oxide-semiconductor
DCAPE	droplet-confined alternate pulsed epitaxy
Eq.	Equation
EDX	energy-dispersive X-ray spectroscopy
FET	field-effect transistor
FFT	fast Fourier transform
Fig.	figure
HAADF	high-angle annular dark-field
HRTEM	high-resolution transmission electron microscopy
L	liquid
LD	length distribution
LED	light-emitting diode
MBE	molecular beam epitaxy
MEE	migration-enhanced epitaxy
ML	monolayer
MOCVD	metal-organic chemical vapor deposition
NW	nanowire
PL	Photoluminescence
QD	quantum dot
QW	quantum well
Ref.	reference
RHEED	reflection high energy electron diffraction
S	solid
SAED	selected area electron diffraction
SoC	system-on-chip
SF	stacking fault
SSMBE	solid-source molecular beam epitaxy
SE	spectroscopic ellipsometry
SEM	scanning electron microscopy
SMP	surface modification procedure
Tab.	table
STEM	scanning transmission electron microscopy
TEM	transmission electron microscopy
TP	twin plane

Abbreviation	**Explanation**
TPL	triple phase line
UHV	ultra high vacuum
V	vapor
VLS	vapor-liquid-solid
VPE	vapor phase epitaxy
VS	vapor-solid
XPS	X-ray photoelectron spectroscopy
WZ	wurtzite
ZB	zinc blende

Symbols

Symbol	Unit	Explanation
α	1	nucleation delay parameter
γ	$^\circ$	tilt angle of AFM tip
Δ	$^\circ$	phase shift between p and s-components after reflectance
ΔE_B	eV	difference in binding energy
ΔH	J	evaporation enthalpy
$\Delta\vec{k}$	$1/m$	reciprocal lattice vector
ΔL	m	length of the nanowire segments grown in DCAPE
$\Delta\mu$	J/mol	driving force for crystallization
Δt	s	nucleation delay time
$\Delta x_l, \Delta x_{l1}$	m	distance in droplet geometrical model
$\Delta x_{l2}, \Delta x_{l3}$	m	distance in droplet geometrical model
$\Delta x_r, \Delta x_{r1}$	m	distance in droplet geometrical model
$\Delta x_{r2}, \Delta x_{r3}$	m	distance in droplet geometrical model
Δy	m	distance in droplet geometrical model
ϵ	1	nucleation antibunching parameter
θ	$^\circ$	droplet contact angle
Θ_{Ga}	m	amount of deposited gallium per each pulse
Θ_{As}	m	amount of deposited arsenic per each pulse
Θ_{As_4}	m	amount of deposited As_4 per each pulse
λ	m	wavelength
λ_0	m	pre-exponential factor for effective jump distance of adatoms
λ_{Ga}	m	surface diffusion length of Ga adatoms
λ_p	m	mean free path
μ_V, μ_S	J/mol	chemical potential of a vapor phase, solid phase
ρ	1	complex reflectance ratio
σ	m	standard deviation of nanowire length distribution
σ^2	m^2	variance of nanowire length distribution
σ_{atoms}	1	capture number of Ga atoms
σ_{dr}	1	capture number of Ga droplets
σ_m	m	molecule diameter
${\sigma_P}^2$	m^2	variance of a Poissonian length distribution
${\sigma_{sub-P}}^2$	m^2	variance of a sub-Poissonian length distribution
τ	1	mean nanowire length in number of MLs
τ_a	s	mean residence time of Ga adatoms on the substrate
τ_c	s	mean time for Ga adatom capture
τ_d	s	mean time of surface diffusion of Ga adatoms

Symbol	**Unit**	**Explanation**
τ_n	s	mean time for Ga droplet nucleation
φ	$^\circ$	tapering angle of AFM tip
Φ	eV	height of energy barrier in tunneling process
Φ_S	eV	work function of XPS spectrometer
Ψ	1	amplitude ratio of p and s-components after reflectance
a	m	lattice parameter
a_{lay}	m	lattice parameter of epilayer
a_{sub}	m	lattice parameter of the substrate
a_{AC}, a_{BC}	m	lattice parameters of binary III-V compounds with atoms of type A, B and C
A	m^2	aperture area
A_{em}	m^2	emission area of electrons
A_{sub}	m^2	substrate surface
b_{ABC}	1	bowing coefficient
$b_{profile}$	m	base width of AFM line profile
$b_{profile_r}$	m	right base width of AFM line profile
$b_{profile_l}$	m	left base width of AFM line profile
c_{As}	$at\%$	arsenic concentration
c_{As}^{eq}	$at\%$	critical concentration of arsenic in the droplet
c_{As}^{cr}	$at\%$	equilibrium concentration of arsenic in the droplet
d	m	diameter of the template nanowire after DCAPE
d_{AlGaAs}	m	thickness of the $Al_xGa_{1-x}As$ sections
d_b	m	base diameter of Ga droplets
d_{base}	m	diameter of nanowire base
d_c	m	corrected droplet diameter
d_{GaAs}	m	thickness of the GaAs section/quantum dot
d_{NW}	m	nanowire diameter
d_t	m	diameter of the template nanowire
d_{tip}	m	diameter of nanowire tip
D	m^2	variance of Green's function of the nanowire length distribution
D_c	$m^2 \cdot s^{-1}$	diffusion coefficient/diffusivity
$erfc(x)$	$a.u.$	complementary error function
E	eV	energy
E_{ad}	J	adsorption/desorption energy
E_B	eV	binding energy
E_C	eV	conduction band energy
E_{diff}	J	diffusion energy
E_g	eV	band gap energy

Symbol	**Unit**	**Explanation**
$E_{g(AC)}, E_{g(BC)}$	eV	band gap energies of binary III-V compounds with atoms of type A, B and C
E_{kin}	eV	kinetic energy of photoelectrons
E_{ox}	$V \cdot m^{-1}$	electric field of oxide barrier
E_p	1	material-dependent parameter for condensation
E_{Ph}	eV	photon energy
E_V	eV	valence band energy
f	1	lattice mismatch
$f(s, \tau)$	$a.u.$	Poissonian nanowire length distribution
$f(s - \tau)$	$a.u.$	sub-Poissonian nanowire length distribution
F	$m^{-2} \cdot s^{-1}$	beam flux produced by effusion cell
$F(s, \tau)$	$a.u.$	Poissonian Green's function
F_{Al}	m/s	aluminum beam flux
F_{As}	m/s	arsenic beam flux
F_{As_4}	m/s	As_4 beam flux
F_{Ga}	m/s	gallium beam flux
F_{In}	m/s	indium beam flux
F_S	$m^{-2} \cdot s^{-1}$	beam flux impinging on a substrate
G	J	Gibbs free energy
GR_{ax}	m/s	axial nanowire growth rate
GR_{As_4}	m/s	axial nanowire growth rate obtained from direct As_4 flux
GR_{Ga}	m/s	axial nanowire growth rate obtained from direct Ga flux
GR_{rad}	m/s	radial nanowire growth rate
h_c	m	corrected droplet height
$h_{profile}$	m	height of AFM line profile (droplet height)
I	A	tunnel current through oxide barrier
$\vec{k}$	$1/m$	wave vector of electrons
$\vec{k_{in}}$	$1/m$	wave vector of incoming electrons
$\vec{k_{out}}$	$1/m$	wave vector of scattered electrons
$k_{a(Ga)}, k_{a(As)}$	$1/s$	adsorption rate of Ga and As from the substrate surface
$k_{d(Ga)}, k_{d(As)}$	$1/s$	desorption rate of Ga and As from the substrate surface
l	m	distance
L	m	length of the elongated template nanowire after DCAPE
L_{NW}	m	nanowire length
L_{ox}	m	thickness of the native-SiO_x
L_t	m	length of the template nanowire
m	kg	atomic or molecular mass
m_{eff}	kg	effective electron mass

Symbol	**Unit**	**Explanation**
n_{NWs}	1	number of vertical GaAs nanowires
N	m^{-2}	number density of vertical GaAs nanowires
N_{at}	m^{-2}	number of atoms inside the Ga droplets per surface area
N_{dr}	m^{-2}	number density of Ga droplets
N_{GaAs}	m^{-2}	number density of GaAs structures
N_{pulse}	1	number of each pulse in DCAPE/number of DCAPE loops
$N_{pulse(As_4)}$	1	number of As_4 pulses
p	1	material-dependent parameter for condensation
p_0	1	nucleation probability
P	Pa	pressure
P_0	Pa	equilibrium pressure at a temperature T_0
P_{eq}	Pa	equilibrium pressure
P_N	1	nucleation probability density
r	m	droplet radius
r_b	m	droplet base radius
r_c	m	corrected droplet radius
r_p	1	normalized amplitude of *p*-component parallel to plane of incidence
r_s	1	normalized amplitude of *s*-component perpendicular to plane of incidence
r_{tip}	m	radius of curvature of AFM tip
s	m	measured nanowire length
$\langle s \rangle$	m	measured mean nanowire length
S	J/K	entropy
S_{Ga}	1	sticking coefficient of gallium on the substrate
$S_{As_{4/2}}$	1	sticking coefficient of As_4 or As_2 on the substrate
$S_{As_{4/2}(max)}$	1	maximum sticking coefficient of As_4 or As_2 on the substrate
t	s	time
t_{a1}	s	duration of SMP step-1
t_{a2}	s	duration of SMP step-3
t_{As_4}	s	total time of As_4 supply
t_{gr}	s	growth duration
$t_{int.}$	s	duration of growth interruption in DCAPE mode
t_{NW}	1	tapering
$t_{pulse(Al)}$	s	duration of aluminum pulse in DCAPE mode
$t_{pulse(As)}$	s	duration of arsenic pulse in DCAPE mode
$t_{pulse(As_4)}$	s	duration of As_4 pulse in DCAPE mode

Symbol	**Unit**	**Explanation**
$t_{pulse(Ga)}$	s	duration of gallium pulse in DCAPE mode
T	$^{\circ}C$	substrate temperature
T_{a1}	$^{\circ}C$	substrate temperature during SMP step-1
T_{a2}	$^{\circ}C$	substrate temperature during SMP step-3
T_c	$^{\circ}C$	temperature of effusion cell
T_d	$^{\circ}C$	substrate temperature during SMP step-2
T_{gr}	$^{\circ}C$	substrate temperature during nanowire growth
U	J	internal energy
V	m^3	volume
V_{dr}	m^3	volume of Ga droplets
V/III	1	beam flux ratio of group-V and group-III growth species
x_{Al}	1	Al-content in an $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}$ ternary alloy
x_{In}	1	In-content in an $\mathrm{In}_x\mathrm{Al}_{1-x}\mathrm{As}/\mathrm{In}_x\mathrm{Ga}_{1-x}\mathrm{As}$ ternary alloy
Y	1	number yield of vertical nanowires

Constants

Constant	**Unit**	**Explanation**
ε_{Si}	1	emissivity of Si, 0.67
$\nu(E_{ox})$	1	constant, accounts for image force, 0.937
π	1	Archimedes constant, ratio of circumference of a circle to its diameter, 3.141..
a_{GaAs}	m	lattice parameter of GaAs, $5.6533 \cdot 10^{-10}$ m
a_{Si}	m	lattice parameter of Si, $5.431 \cdot 10^{-10}$ m
h	$J \cdot s$	Planck constant, $6.626... \cdot 10^{-34}$ J·s
h_{GaAs}	m	height of one ML of GaAs in $\langle 111 \rangle$ direction, 0.326 nm
k_B	$J \cdot K^{-1}$	Boltzmann constant, $1.38065 \cdot 10^{-23}$ J·K^{-1}
m_0	kg	free electron mass, $9.10938 \cdot 10^{-31}$ kg
n_{Ga}	cm^3	atom density of liquid Ga, $5.099 \cdot 10^{22}$ cm^{-3}
q	C	elementary charge, $1.602... \cdot 10^{-19}$ C
$t(E_{ox})$	1	constant, accounts for image force, 1.011

Author Publications

Peer-Review Journal Articles

This dissertation is based on the following peer-review articles:

1. L. Balaghi, **T. Tauchnitz**, R. Hübner, L. Bischoff, H. Schneider, M. Helm, E. Dimakis, Droplet-Confined Alternate Pulsed Epitaxy of GaAs Nanowires on Si Substrates down to CMOS-Compatible Temperatures, *ACS Nano Letters* **16**(7), 4032–4039 (2016).
2. **T. Tauchnitz**, T. Nurmamytov, R. Hübner, M. Engler, S. Facsko, H. Schneider, M. Helm, E. Dimakis, Decoupling the Two Roles of Ga Droplets in the Self-Catalyzed Growth of GaAs Nanowires on SiO_x/Si(111) Substrates, *ACS Crystal Growth & Design* **17**(10), 5276–5282 (2017).
3. **T. Tauchnitz**, Y. Berdnikov, V. G. Dubrovskii, H. Schneider, M. Helm, E. Dimakis, A simple route to synchronized nucleation of self-catalyzed GaAs nanowires on silicon for sub-Poissonian length distributions, *IOP Nanotechnology* **29**(50), 504004 (2018).

Further peer-review articles:

4. W. Weinreich, **T. Tauchnitz**, P. Polakowski, M. Drescher, S. Riedel, J. Sundqvist, K. Seidel, M. Shirazi, S. D. Elliott, S. Ohsiek, E. Erben, B. Trui, TEMAZ/O_3 atomic layer deposition process with doubled growth rate and optimized interface properties in metal-insulator-metal capacitors, *AVS Journal of Vacuum Science & Technology A* **31**(1), 01A123 (2013).
5. Y. Daskal, **T. Tauchnitz**, F. Güth, R. Dittrich, Y. Joseph, Assembly Behavior of Organically Interlinked Gold Nanoparticle Composite Films: A Quartz Crystal Microbalance Investigation, *ACS Langmuir* **33**(43), 11869–11877 (2017).

Conference Proceedings

1. Y. Berdnikov, V. G. Dubrovskii, N. V. Sibirev, A. A Koryakin, A. S. Sokolovskii, **T. Tauchnitz**, H. Schneider, M. Helm, E. Dimakis, Theoretical analysis of the length distributions of Ga-catalyzed GaAs nanowires, *IOP Conference Series: Journal of Physics: Conference Series* **1124**, 022039 (2018).

Conference Talks

1. **T. Tauchnitz**, H. Schneider, M. Helm, E. Dimakis, The double role of Ga droplets in the self-catalyzed growth of GaAs nanowires on SiO_x/Si(111) substrates, *19th International Conference on Molecular Beam Epitaxy*, Montpellier/France, September 4 – 9, 2016.
2. **T. Tauchnitz**, L. Balaghi, R. Hübner, L. Bischoff, H. Schneider, M. Helm, E. Dimakis, What Ga droplets can and cannot do in the growth of GaAs nanowires on Si substrates, *19th European Workshop on Molecular Beam Epitaxy*, Korobitsyno, St. Petersburg/Russia, March 19 – 22, 2017. (invited)
3. **T. Tauchnitz**, Y. Berdnikov, V. G. Dubrovskii, H. Schneider, M. Helm, E. Dimakis, A simple route to synchronized nucleation of self-catalyzed GaAs nanowires on Si for sub-Poissonian length distributions, *3rd Nanowire Week*, Hamilton/Canada, June 11 – 15, 2018.

Conference Posters

1. **T. Tauchnitz**, H. Schneider, M. Helm, E. Dimakis, Local etching of a SiO_x layer on Si(111) by Ga droplets and its influence on GaAs nanowire growth, *80th Annual Meeting of the DPG and Spring Meeting*, Regensburg/Germany, March 6 – 11, 2016.
2. **T. Tauchnitz**, T. Nurmamytov, R. Hübner, M. Engler, S. Facsko, H. Schneider, M. Helm, E. Dimakis, Ga droplets on SiO_x/Si(111) substrates: nucleation and etching, *19th European Workshop on Molecular Beam Epitaxy*, Korobitsyno, St. Petersburg/Russia, March 19 – 22, 2017.
3. **T. Tauchnitz**, T. Nurmamytov, R. Hübner, M. Engler, S. Facsko, H. Schneider, M. Helm, E. Dimakis, Decoupling the two roles of liquid Ga droplets in the self-catalyzed growth of GaAs nanowires on SiO_x/Si(111) substrates, *2nd Nanowire Week*, Lund/Sweden, May 29 – June 2, 2017.
4. **T. Tauchnitz**, L. Balaghi, I. Fotev, S. Shan, A. Pashkin, G. Bussone, R. Grifone, J. Grenzer, R. Hübner, M. Ghorbani-Asl, A. V. Krasheninnikov, H. Schneider, M. Helm, E. Dimakis, III-As nanowires for telecom applications on Si platforms, *Workshop Helmholtz Association "From Matter to Materials and Life"*, Dresden/Germany, February 13 – 15, 2019.

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Eidesstattliche Erklärung

Hiermit versichere ich an Eides statt, dass ich die vorliegende Dissertation mit dem Titel “Novel Methods for Controlled Self-Catalyzed Growth of GaAs Nanowires and GaAs/$Al_xGa_{1-x}As$ Axial Nanowire Heterostructures on Si Substrates by Molecular Beam Epitaxy” selbstständig und ohne unzulässige Hilfe Dritter verfasst und keine anderen Hilfsmittel als angegeben verwendet habe. Alle wörtlichen und sinngemäßen Übernahmen aus anderen Werken habe ich als solche kenntlich gemacht. Ich versichere, dass diese Arbeit bisher in keiner oder ähnlicher Form weder im Inland noch im Ausland einer anderen Prüfungsbehörde vorgelegen hat und noch nicht veröffentlicht worden ist.

Hiermit erkläre ich, zu keiner anderen Zeit und an keinem anderen Ort zuvor ein anderes Promotionsverfahren eröffnet zu haben. Ich erkenne die Promotionsordnung der Fakultät Maschinenwesen der Technischen Universität Dresden in der gültigen Fassung vom 01.07.2001 an.

Dresden, den 25.07.2019

Tina Tauchnitz

Bautzner Landstr. 400
01328 Dresden, Germany
Tel. +49 351 260-2765
Fax +49 351 260-12765
e.dimakis@hzdr.de
http://www.hzdr.de