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Investigations of internal stresses in high-voltage devices with deep trenches

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ABSTRACT

Deep trenches, as essential elements of silicon chips used in electronic high-power and high-frequency devices, are known as starting points for dislocation generation under the influence of internal mechanical stresses resulting mainly from the difference of the thermal expansion coefficients between silicon and silicon dioxide. Since the electrical insulation of the devices requires a sequence of mechanical, chemical and high-temperature processes during the preparation of the deep trenches, including the formation of an amorphous SiO_2 edge layer, the emergence of the internal stresses is hardly avoidable. The method of cross-correlation backscattered electron diffraction in the scanning electron microscope is used here to determine quantitatively magnitude and local distribution of internal stresses in the silicon around the deep trenches after four different process steps. For this purpose, Kikuchi diffraction images are recorded of the wafer cross-section areas along lines perpendicular and parallel to the deep trenches. After Fourier transformation, these images are cross-correlated with the Fourier transform of the diffraction image from a stress-free reference sample site. The well-established numerical evaluation of cross-correlation functions provides the complete distortion tensor for each measuring point of the line scan, from which the stress tensor can be calculated using Hooke's law. It is found that the in-plane normal stress component σ_{11} perpendicular to the long edges of the deep trench is larger than the other stress components. That means, it essentially determines the magnitude of the von-Mises stress, which was determined as a general stress indicator for all measuring points, too. A characteristic feature is the local distribution of the stress component σ_{11} with maximum tensile stresses of some hundred MPa at the transition between the Si and the amorphous SiO_2 on the long edges of the deep trench, and with even higher maximum compressive stresses immediately below the bottom of the deep trench. At a distance of about 2 µm from the edges of a single deep trench, all stress components decrease to negligibly small values, so that steep stress gradients occur. The range and distribution of tensile and compressive stresses are in accordance with finite element simulations, however, the measured stresses are higher than expected for all investigated states, so that dislocation formation seems to be possible. The influence of the electron acceleration voltage on the determination of the internal stresses is discussed as well.

I. INTRODUCTION

Power semiconductor devices are essential for a wide variety of technical applications. Commonly, Vertical Double-diffused Metal-Oxide-Semiconductor (VDMOS) transistors are used in high-voltage and power components.[1] The VDMOS transistor is suitable for operation in high-frequency systems, too, due to its high switching speed and thermal stability. A major requirement for the functionality of VDMOS transistors in high-voltage and power devices is their isolation from voltages of up to 500 V.[2,3] Such isolation is achieved by deep trenches with different geometries, which are prepared in the process of manufacturing silicon chips.

The trench insulation process comprises a number of successive steps: the directional reactive ion etching (RIE) of the trenches, the formation of amorphous SiO_2 layers on the trench edges by thermal oxidation (TO) at 1050 C and chemical vapor deposition (CVD), the filling of the trenches with polysilicon (SiF), the chemical-mechanical polishing (CMP) to remove the excess polysilicon, and finally, a series of rapid high temperature annealing (RTA) intervals.[4] Because of difference between the thermal expansion coefficients of silicon and SiO_2, internal stresses arise in the TO and CVD steps. Actually, the stresses should be minimized by the SiF process step. However, the subsequent doping implantation and the RTA step increase thermo-mechanical stresses. If the internal stresses are distributed adversely, dislocations can be unintentionally generated in the silicon crystal lattice. Under the influence of the internal stresses the dislocations can slip and interact with each other, leading to the generation of point defects. A disturbed crystal structure in the dislocation core region and the accompanying lattice defects can cause power loss and chip failure.[5,6] For very high local stress in silicon, micro-cracks can be formed causing catastrophic failure. Therefore, the occurrence of dislocations should be mitigated in the manufacturing process.

Several experimental techniques enable the detection of dislocations created during processing of deep trenches. Direct observation of the dislocations is possible by imaging in the transmission electron microscope (TEM) or in the scanning electron microscope (SEM). Since the dislocations are usually located in the silicon near the lower part of the deep trenches, a destructive sample preparation including an etch treatment is often necessary. Additionally, the electron microscopy studies can be combined with micro-photoluminescence imaging. Here, the fact is exploited that the normally observed radiative band-to-band transition in silicon disappears by defect induced band gap variations as well as by shallow or deep level traps in the band gap induced by dislocations.[7] Using optical filters, dislocations can be visualized and a local dislocation density can be determined in micro-photoluminescence images.[8] In micro-photoluminescence investigations the spatial resolution for the detection of dislocations is of the order of 1 µm, but only rough qualitative information is provided on the distribution of mechanical stresses that caused the formation of dislocations. As a more direct method for the determination of internal mechanical stresses around deep trenches, X-ray diffraction imaging is proposed.[9] It is a non-destructive method and the brightness contrast variations provide qualitative information of the strain distributions, associated with high dislocation densities in the silicon next to VDMOS devices.

Diffraction studies provide quantitative information about crystal lattice distortions that can be correlated with the mechanical stresses within the framework of the linear elasticity theory. The interaction volume of the incident radiation in the single-crystalline silicon determines the integral stress values. In the case of electron backscatter diffraction (EBSD) in the SEM, the diffraction pattern is formed by the so-called Kikuchi bands and shows a regular arrangement of almost parallel bright bands over a background of backscattered electrons. The Kikuchi bands represent a gnomonic projection of the crystal lattice planes on a plane detector screen, with the intersections of the Kikuchi bands forming prominent and distinct zone axes.[10] Energy-resolved measurements have shown that the Kikuchi bands are generated by such backscattered electrons, which essentially still have the energy of electrons in the incident beam.[10] The chain of scattering processes leading to the formation of the diffraction pattern thus includes elastic and coherent (Bragg scattering) as well as quasi-elastic and incoherent (phonon scattering) processes.[11] With the usual EBSD geometry, where the stationary electron beam hits a steeply tilted sample surface, these processes occur in a very near-surface region. The information depth of EBSD was proved to be in the order of some 10 nm in silicon[12], the lateral spatial resolution parallel to the sample tilt axis is about 50 nm [13] so that the mapping of local stresses on that scale is feasible with respect to the dimension of the deep trenches in the µm range. Another advantage of the EBSD method is that investigations on bulk specimens can be performed without extensive preparation, provided that no disturbing surface roughness is present and the density of crystal lattice defects in the interaction volume is so low that the Kikuchi bands are not blurred.

A procedure for the evaluation of the Kikuchi diffraction pattern was derived by Wilkinson *et al.*.[14] It allows the calculation of all components of the local distortion tensor. The analysis is based on a cross-correlation between Fourier transformed chosen regions of interest on a Kikuchi diffraction pattern acquired at a sample site with internal stresses and such ones obtained from a stress-free reference region. Since Kikuchi diffraction patterns can be recorded with high precision, the cross-correlation electron backscatter diffraction (CC-EBSD) has been applied to strain mapping of semiconductor materials[13] as well as for the determination of the density of geometrically necessary dislocations in severe plastically deformed metals.[15] A strain sensitivity of ~ 10^{-4} is readily obtained by CC-EBSD.[16]

The aim of the present paper is to determine experimentally the magnitude and the spatial distribution of the internal stresses in the silicon in the surrounding of deep trenches in VDMOS devices after several process steps. Thus, the CC-EBSD data provide valuable information for the optimization of the manufacturing process.

II. EXPERIMENTAL SET UP AND DATA EVALUATION

The imaging of the samples and the EBSD investigations were carried out using a *Zeiss Ultra 55* SEM with field emission gun. For the conventional EBSD analysis, the SEM is equipped with an *HKL/Nordlys* detector system and the *Channel 5* evaluation software. The EBSD measurements were performed at 20 kV acceleration voltage and approximately 3 nA beam current. The experimental set up for the EBSD studies is presented in Fig. 1.

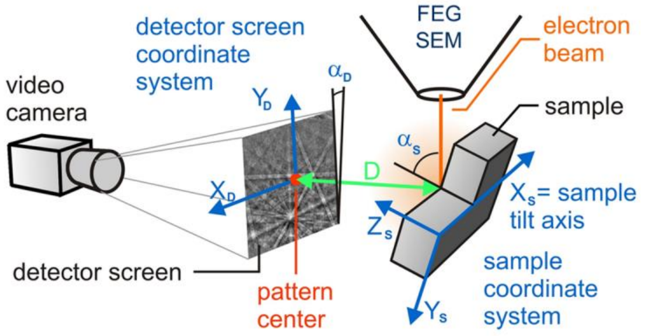
detector screen coordinate system
video camera
α_D
Y_D
X_D
FEG SEM
electron beam
sample
α_S
D
X_s= sample tilt axis
Z_s
detector screen
pattern center
Y_s
sample coordinate system

Fig. 1. Experimental set up for the EBSD investigations where the sample surface normal is tilted by an angle α_S of about 69° to the electron beam. Additionally, the

coordinate systems for the sample as well as for the detector screen are indicated together with the sample to detector distance D and the tilt angle $\alpha_D \approx 6°$ of the detector screen.

For the calculation of the local stress tensor from a Kikuchi pattern, it was necessary to acquire diffraction images of sufficient quality from the measuring point and from a stress-free reference sample site. On the Kikuchi pattern at least 17 regions of interest were chosen to solve the equations for the calculation of the elements of the distortion tensor with good statistical confidence. The orientation of the crystal lattice relative to the sample coordinate system expressed by the three Eulerian angles was determined by conventional EBSD. All geometrical parameters of the EBSD set-up which are shown in Fig. 1, were carefully measured. As recommended by Wilkinson *et al.*[17] band-pass filters in Fourier space were used for the Fourier transformation, and appropriate values for mask size and boundary conditions were set for the cross-correlation function. The software used here for the calculations[7,13] was written by one of the authors (P. Chekhonin) and is based on the work of Wilkinson *et al.*.[14,17] A condition for the determinability of the complete strain tensor is the assumption that the normal stress component σ_{33} perpendicular to the sample surface is equal to zero in the entire EBSD information volume in the sample surface region. As results of the calculations, the lattice rotations ω_{ij}, the three shear strain components ε_{ij} and the three normal strain components ε_{ii} of the strain tensor are obtained for each measuring point referring to the stress-free reference point. By applying Hooks' law, the shear stress components τ_{ij} and the normal stress components σ_{ii} of the stress tensor can be calculated from the strain tensor using the stiffness tensor for Silicon[18] with C_{11} = 166 GPa, C_{12} = 64 GPa and

C_{44} = 80 GPa in Voigt notation after transformation into the sample coordinate system. For a general characterization of the local stress state, the von-Mises stress σ_{vM} with $\sigma_{33} = 0$ is calculated by

$$\sigma_{vM} = \sqrt{\frac{1}{2}\left[(\sigma_{11}-\sigma_{22})^2+\sigma_{11}^2+\sigma_{22}^2+6\cdot(\tau_{12}^2+\tau_{13}^2+\tau_{23}^2)\right]} \qquad (1)$$

for each measuring point.

To minimize the influence of sample adjustment errors on the determination of mechanical stresses, particularly caused by the determination of the exact tilt angle α_S, the Kikuchi diffraction images used for CC-EBSD analysis were always recorded on lines parallel to the sample tilt axis X_S (so-called line scans) with a distance of 10 nm between each measuring point. At each point, the measuring time per frame was 43 ms and 20 frames were superimposed to generate the Kikuchi pattern with a low noise level on the single-crystalline wafer. To enhance the acquisition speed a detector binning of 2 x 2 was set, resulting in a detector resolution of 672 x 512 pixels.

The experimental investigations were performed on the cleaved cross-section area of silicon wafers with deep trenches in four different process states. Examples for the deep trenches are shown in Fig. 2. The depth of the trenches amounts 40 µm and the distance between neighboring deep trenches is 120 µm. The deep trenches were imaged by backscattered electrons in order to illustrate the material contrast between silicon and the amorphous silicon dioxide layer on the trench edges. This contrast is clearly visible after the CMP process (see Fig. 2 c)).

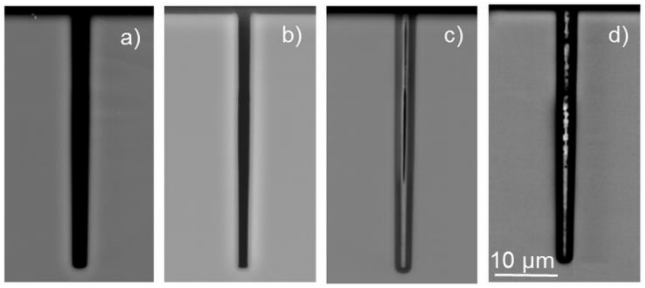

Fig. 2. Deep trenches on the cross-section areas of cleaved silicon wafers after different processing steps ((a) RIE, (b) RIE + TO, (c) RIE + TO + CVD + SiF + CMP, (d) RIE + TO + CVD +SiF + CMP + RTA) imaged by backscattered electrons in the SEM. The scale bar applies to all images a) to d).

Because the mechanical stresses given below are related to the deep trench *x*-*y*-*z* coordinate system, Fig. 3 shows this system for a deep trench after the last processing step RTA. As commonly used, for example, the labelling σ_{11} stands for the description of the normal stress component σ_{xx}. Additionally, in Fig. 3 are depicted the crystallographic orientation of the wafer and a typical Kikuchi diffraction image taken on the $[\bar{1}10]$-oriented cross-section area of the silicon wafer.

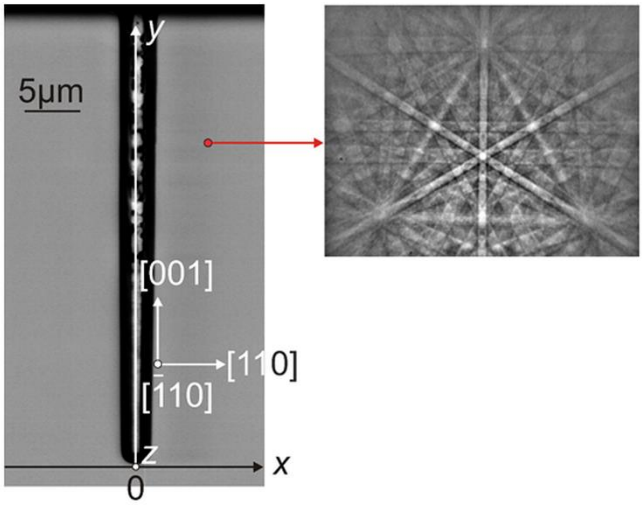

Fig. 3. *x*-*y*-*z* coordinate system referring to the deep trench, crystallographic orientation of the wafer, and typical Kikuchi diffraction image from the red marked point on the $(\bar{1}10)$ plane of the wafer cross-section area at an electron acceleration voltage of 20 kV.

To characterize the mechanical stress state in the bulk wafer material surrounding the deep trench, the EBSD line scans were performed parallel to the *x*-axis at four different distances to the wafer surface, i.e. at different *y*-values, crossing the deep trench. The first line scan at $y_1 \approx 38$ µm is located near the surface of the wafer, the second one at $y_2 \approx 20$ µm is in the middle region of the deep trench and the third one at $y_3 \approx 0$ µm directly below the bottom of the deep trench. The last line scan was carried out at $y_4 \approx$ - 12 µm for testing the absence of stresses in the wafer material far from the deep trench region. Each line scan is positioned symmetrically to the center of the deep trench and contains 800 measuring points in all. Only for the last state after the RTA process, additionally an EBSD line scan parallel to the *y*-axis at a distance of $x_1 \approx 2$ µm from the trench center was performed and 5000 Kikuchi patterns were recorded over a length of 50 µm.

III. RESULTS AND DISCUSSION

In Fig. 4, the major results of the stress calculations are summarized for the EBSD line scans. At first glance, it is obvious that for the line scans at the y_1 and y_2 positions in the range of about 2 µm around the center of the deep trench no values for the stresses σ_{11} and σ_{vM} are indicated in Figs. 4 a) and b). On the one hand, this is due to the fact that no diffraction images are generated in the not yet filled trench areas after the process steps RIE and TO. Furthermore, the amorphous SiO_2 regions at the edges of a deep trench do not provide Kikuchi diffraction patterns but only a relatively homogeneous scattering signal. In the center of the trenches, Kikuchi diffraction patterns can be observed in some cases due to the coherent electron scattering on small Si crystallites after applying the process RTA. However, they cannot be evaluated by comparison with the diffraction pattern from the reference site because they do not show the basic crystallographic orientation of the Si wafer with the typical Kikuchi diffraction pattern given in Fig. 3. It is also worth to mention that for the determination of the stresses in the figures Figs. 4 a) and b) different reference patterns had to be used for the evaluation of the diffraction images from the right and the left side of the trench with respect to the coordinate $x = 0$. This was necessary because the non-connected areas on both sides of the trench relaxed by the cleavage and showed a mutual rotation of some degrees. For such high lattice rotations, the applied CC-EBSD software is of only limited applicability.[15] The reference patterns used were always the first (or the last) diffraction images on a *y* line scan, which were assumed to be from stress-free areas with the greatest possible distance to the trench. For the diagrams in Fig. 4, five stress values neighboring on the line scan were averaged, and these average values were plotted at an interval of 50 nm. This procedure is adapted to the lateral spatial resolution of the EBSD method in a direction parallel to the sample tilt axis X_S. On the other hand, the displayed error bar provides information about the standard deviation of the stress values of these five measuring points. The error bars are small with ± 20 MPa in regions where the stress values do not change significantly, but they are partly considerable in regions with a strong stress gradient. This can also be interpreted as an indication of the high local sensitivity of EBSD measurements.

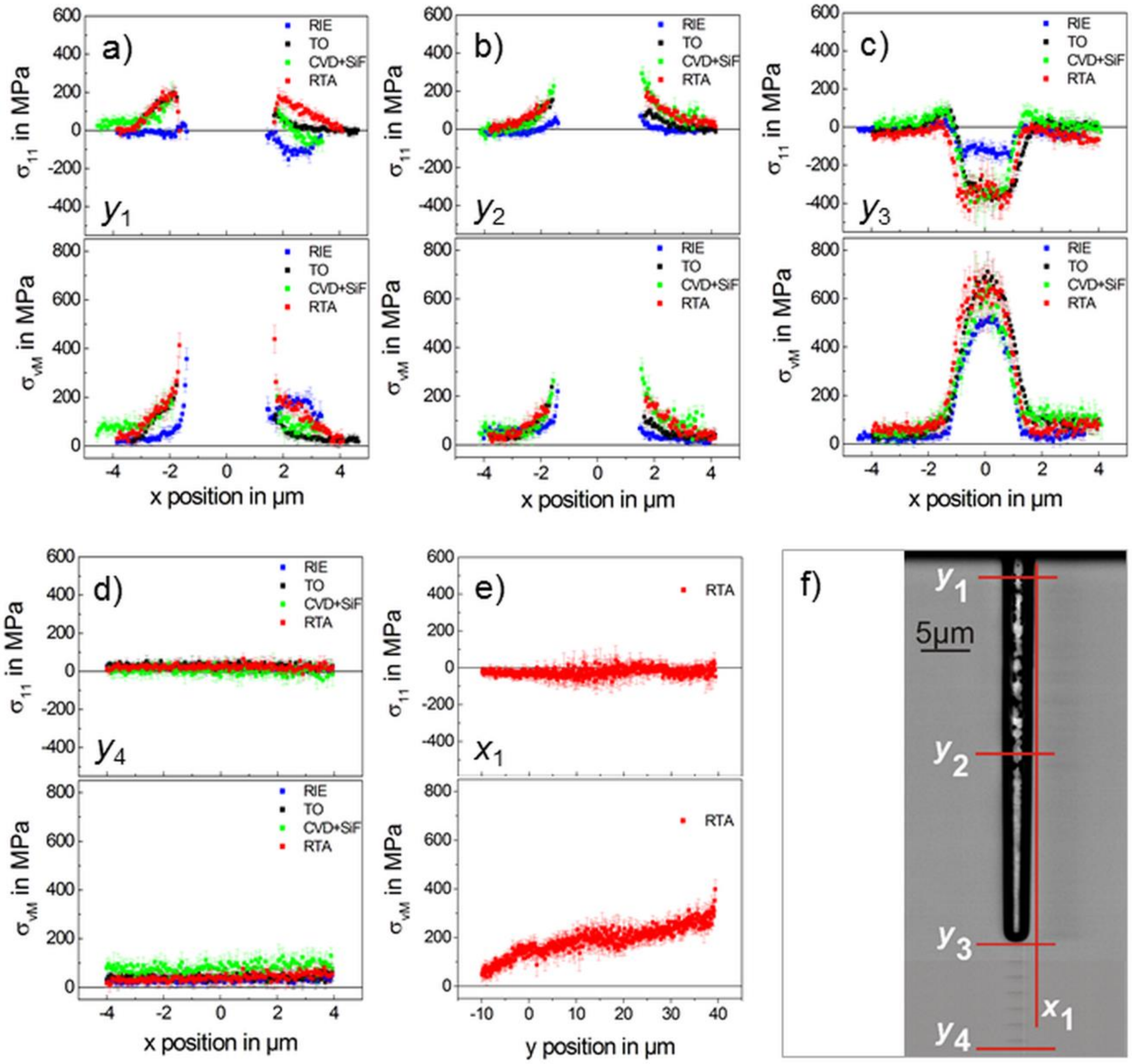

Fig. 4. Normal stress component σ_{11} and von-Mises stress σ_{vM} in the four process states RIE, TO, CVD+SiF and RTA investigated along line scans at different y positions at $y_1 \approx 38$ µm (a), at $y_2 \approx 20$ µm (b), at $y_3 \approx 0$ µm (c), at $y_4 \approx - 12$ µm (d), and along a line scan at $x_1 \approx 2$ µm (e). The respective positions of the line scans are shown exemplarily for the process state RTA in (f).

All CC-EBSD evaluations revealed that the stress component σ_{11} always reaches the highest absolute values compared to the other stress tensor components. The component σ_{11} is therefore shown in Fig. 4 as a representative and an upper limit of the other stress components. For all the y line scans, the mechanical stresses after the RIE process (blue data points in Fig. 4) are lower than the stresses in the other three states of the deep trench investigations. This is in accordance with stress simulations by Greenwood *et al*..[8] The only exception is the y_1 line scan, where an unexpected stress distribution appears on the right side of the trench, probably caused by the cleavage of the wafer to release the cross section. Taking into account the error band, there are no significant differences between the local stresses determined at the same y position of the line scan on three wafers with deep trenches after the process steps TO, CVD+SiF and RTA, respectively. This means that the silicon filling of the deep trenches does not lead to a significant stress minimization as expected, but that the stress distribution created by the thermal oxidation is essentially maintained in all subsequent process steps.

The in-plane stress component σ_{11} which is perpendicular to the long edges of the trench increases over a range of about 2 µm on both sides of the deep trenches with decreasing distance to the amorphous border of the trench. The stress σ_{11} can assume maximum tensile stress values of up to 250 MPa for the line scans at y_1 and y_2 (Fig. 4 a) and b)). The highest stresses occur at the immediate interface between the crystalline wafer and the amorphous edge of the deep trench. In contrast, the line scan at y_3 provides for the stress component σ_{11} compressive stresses of about -100 MPa (after RIE) and of - 400 MPa (for the subsequent process steps), which are nearly constant over a length of 2 µm directly below the bottom of the deep trench (Fig. 4 c)). These compressive stresses are coming on both sides from small positive stress values in front of the edge of the trench, with a strong stress gradient over a range of about 1 µm. The magnitude of the measured stresses is higher than computed in the simulations[8], but the sign and the local distribution of the stresses is just as expected. However, these simulations[8], which were carried out for a bulk sample exposed to the same oxidation temperature of 1050 C, used an only roughly estimated change in stress associated with grain growth in the polysilicon inside the trench. On the other hand, the simulations correspond to the negligibly small stresses that were determined in the line scan y_4 at a large distance from the bottom of the deep trench (Fig. 4 d)).

The von-Mises stress as fictitious equivalent stress for the total stress state shows for the line scans y_1 and y_2 an extremely sharp increase towards the edges of the deep trench and reaches values up to 500 MPa. Directly below the deep trench on line scan y_3, values for σ_{vM} of up to 700 MPa can be reached, indicating that, apart from σ_{11}, the other stress components also contribute to the magnitude of σ_{vM}.

The line scan at a distance $x_1 \approx 2$ µm parallel to the deep trench provides only small values for σ_{11}, which hardly change with the y position on the line scan (Fig. 4 e)). This is essentially the expected behavior from the y line scans. The larger values for σ_{vM} near the surface of the wafer are mainly due to larger contributions of the shear stress components τ_{12} and τ_{23}.

IV. SUMMARY AND CONCLUSIONS

Based on a CC-EBSD stress analysis in silicon after cleavage, magnitude and distribution of mechanical stresses in the vicinity of deep trenches at several processing states were determined. From the EBSD line scans on cross-sections of wafers, it was obtained that all components of the stress tensor are zero within the error limit of about ±20 MPa at distances larger than 2μm from the trench borders. This result is in good agreement with finite element simulations.[8] At lower distance from the deep trench, high stress values are observed, especially for the in-plane normal stress component σ_{11} perpendicular to the long trench edges. In the area around these edges, tensile stresses $\sigma_{11} > 0$ occur, and directly below the bottom of the deep trench, compressive stresses $\sigma_{11} < 0$ are present. Strong stress gradients next to the deep trench are typical for all process states, with maximum values for σ_{11} of up to 250 MPa and -400 MPa, respectively, for the TO, CVD+SiF and RTA process states. The stress values after the RIE process are significantly lower.

Dislocation formation is supposed to be the induced by these internal stresses, especially after higher temperatures processes, since the lower yield stress in Si is about 200 MPa at 600°C.[19] In particular, the high stresses at the bottom of deep trenches can lead to dislocation generation, which could be associated with dislocation slip at {111} lattice planes. This result corresponds to the dislocation distribution found in micro-photoluminescence measurements for the fully processed deep trench.[8]

The assessment of the results of the stress determination applying the CC-EBSD method must take into account that all measurements were carried out on the cross-section area of the wafer after cleavage. Since wafer cleavage is accompanied by relaxation of the off-plane stress components, the determined stresses are lower limits for the stresses occurring in the bulk wafer material.

Though the cross-correlation EBSD method provides reliable stress data, the size of the EBSD interaction volume and thus the extension of the region for the experimentally conditioned stress averaging must be considered, especially for strong stress gradients. The use of lower electron acceleration voltages will lead to a better spatial resolution for the stress determination. However, the reduction of the beam current associated with the voltage reduction in the *Zeiss Ultra 55* SEM as well as the physically induced broadening of the Kikuchi bands at lower electron energies either lead to enhanced image drift and carbon contamination issues for longer lasting measurements, or to lower contrast Kikuchi diffraction images, which makes it more difficult to detect small strain-induced changes in the Kikuchi bands. The chosen experimental parameters appear to be a reasonable compromise for the stress distribution determination in the surrounding of deep trenches.

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FIGURE CAPTIONS

Fig. 1. Experimental set up for the EBSD investigations where the sample surface normal is tilted by an angle α_S of about 69° to the electron beam. Additionally, the coordinate systems for the sample as well as for the detector screen are indicated together with the sample to detector distance *D* and the tilt angle $\alpha_D \approx 6°$ of the detector screen.

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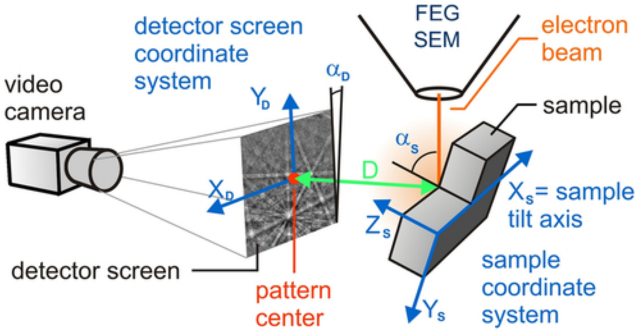
(d) RIE + TO + CVD +SiF + CMP + RTA) imaged by backscattered electrons in the SEM. The scale bar applies to all images a) to d).

Fig. 3. *x*-*y*-*z* coordinate system referring to the deep trench, crystallographic orientation of the wafer, and typical Kikuchi diffraction image from the red marked point on the $(\bar{1}10)$ plane of the wafer cross-section area at an electron acceleration voltage of 20 kV.

Fig. 4. Normal stress component σ_{11} and von-Mises stress σ_{vM} in the four process states RIE, TO, CVD+SiF and RTA investigated along line scans at different *y* positions at $y_1 \approx 38$ µm (a), at $y_2 \approx 20$ µm (b), at $y_3 \approx 0$ µm (c), at $y_4 \approx -12$ µm (d), and along a line scan at $x_1 \approx 2$ µm (e). The respective positions of the line scans are shown exemplarily for the process state RTA in (f).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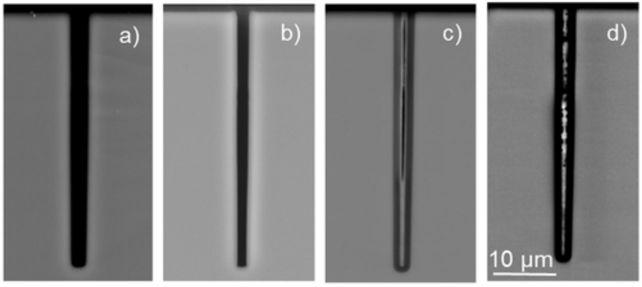
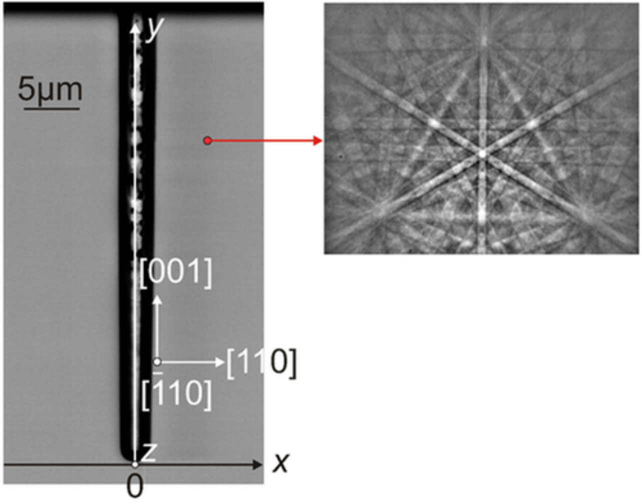

a)
b)
c)
d)
10 µm


y
5µm
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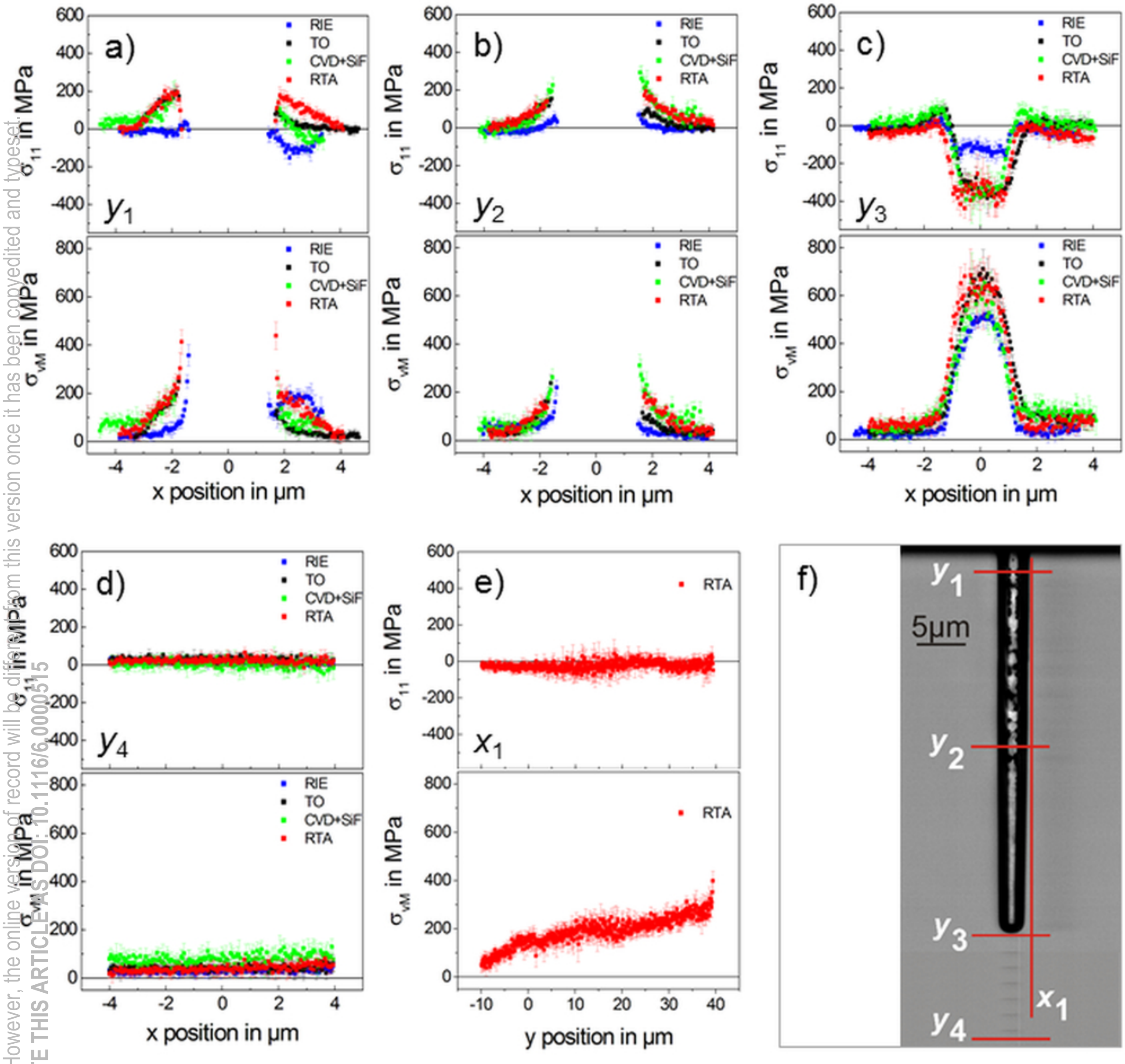
$[\bar{1}10]$
z
x
0


a)
b)
c)
d)
e)
f)
y_1
y_2
y_3
y_4
x_1
RIE
TO
CVD+SiF
RTA
σ_{11} in MPa
σ_{vM} in MPa
x position in µm
y position in µm
5µm