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Nanocluster-rich SiO_2 layers produced by ion beam synthesis: electrical and optoelectronic properties

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1. Introduction

Information technology is one of the greatest challenges of the new millenium. Especially the wide field of communication technology has an enormous growth potential and already today nearly all spheres of everyday life are more and more influenced by microelectronic devices. Novel developments in microelectronics are always related to the following goals: (i) the increase of clock speed for more powerful computers, (ii) the increase of storage capacity of memories and hard disks, (iii) lower power consumption and (iv) the decrease of production costs.

The complexity of integrated circuits increases very rapidly following Moore's law [Moo65]. The ongoing shrinking of electronic device structures has now reached limits set by optical lithography with dimensions in the nanometer range [SIA00, MelA00, Hoso00]. Nanostructures, partly produced by self organization processes, are an interesting and promising approach to overcome these limitations. Due to outstanding innovations in the field of analytical techniques like the high resolution transmission electron microscopy (TEM), the scanning tunneling microscopy (STM) [Binn85] or the atomic force microscope (AFM) new possibilities for the investigation of structures in the nanometer and sub-nanometer range were opened in the eighties and nineties. This and other issues will lead to a paradigm shift in microelectronics, and the nanotechnology will become one of the key technologies of the 21st century, influencing common technologies and working processes in a dramatic way.

Recent developments in the field of mobile computing, novel multimedia applications like handheld computers and digital cameras and the large market of mobile communication lead to a strong increase in the need for non-volatile (nv) memories. Low cost nv-memories with high storage capacities operated at low voltages are necessary to meet the requirements of the growing market. Therefore the common technology of Electrically Erasable Programmable Read Only Memories (EEPROM) will be replaced more and more by novel approaches using nanostructures.

The basis of microelectronics is silicon and its oxide SiO_2. Thousands of papers have been published about the properties of silicon in the past 50 years and so it is one of the best studied materials worldwide. The often announced replacement of silicon by other materials failed up to now. Silicon still remains the dominating material in microelectronics and more than 98% of the commercially available integrated circuits (IC) are based on it [Priv00]. Silicon chips have reached a level of complexity such that the limitation in the overall system speed is the speed of information flow through the interconnects between the different components. Electrical interconnects cannot meet the requirements for high speed data transmission any longer because they are subject to inherent delays due to the distributed inductances and capacitances in the interconnects themselves. Furthermore, the large number of interconnects which are required for modern chips lead to a space problem. This means that the throughput between chips is limited by the number of interconnects which fit on the chip. Electrical interfacing is complex and quite difficult to handle and therefore a strong limitation for the ongoing shrinking of IC's.

In addition, electrical interconnects are vulnerable to electromagnetic interferences and emit electromagnetic radiation itself. Optical interfacing between chips could overcome these problems. Therefore it is necessary to find a light source which can be monolithically integrated in silicon chips. However, silicon has an indirect band gap and the recombination of electrons and holes in the bulk crystalline silicon produces only a very weak luminescence in the infrared, making silicon an unsuitable material for light sources in optoelectronic applications.

In contrary to that, many compound semiconductor materials have a direct bandgap making them the ideal materials for semiconductor light sources which are well-known in optoelectronics for providing a means to generate light. Examples of such semiconductor light sources are semiconductor lasers, light emitting diodes (LED) and electroluminescent display devices. But these light sources fabricated by rather complex and expensive compound semiconductor technologies are not compatible with the common silicon technology used for very large scale integration (VLSI) chips. However, many optoelectronic and display systems use VLSI silicon chips for performing signal processing. Because of the fabrication technologies of the light source which are not sufficiently compatible with or applicable to VLSI chips, the semiconductor light sources have necessarily been provided on separate chips which are electrically interfaced with the silicon chips. The optoelectronic ICs are generally based on binary, ternary or quaternary semiconductor compounds compatible with GaAs or InP substrates which rely on epitaxial crystal growth techniques. LEDs made from these direct bandgap semiconductor materials operate simply as a result of carrier recombination in a p-n junction. The processing of these materials is radically different and more expensive than the processing of standard silicon ICs. Also, the computational and signal processing power which is achieved for modern silicon ICs is normally not available in these more complex materials and the materials are not as stable as silicon in electronic circuits. So applications for fast signal processing would require interfacing the sophisticated compound semiconductor technologies with the common silicon ICs. However, this would result in added weight and added complexity of the circuits leading to higher costs. Recent developments give hope to overcome the problems by using a perovskite (strontium titanate) as an interfacial layer between the silicon circuitry and GaAs as an epitaxial compound semiconductor layer [Moto01]. The relaxed crystal lattice of the perovskite material which lies between that of silicon and GaAs takes the strain and avoids cracks and dislocations that typically would result from the mismatch of the lattices. The future will show if this technique can be established also for other compound semiconductor layers.

This work is focused on the properties and possible applications of nanostructures produced in a silicon based technology. Chapter 2 gives a short introduction into the electric properties of silicon dioxide layers containing silicon based nanostructures. Different approaches for the formation of novel structures for non-volatile memories are analyzed in section 2.3. Despite the success in the formation of memory devices basing on nanocluster rich oxide layers reported by several groups in the last decade, several questions can still not be answered. One of the main open questions is the bond structure in the cluster-rich layers. It is assumed that the storage of the charge does not occur directly in the cluster but in traps at the interface cluster / SiO_2 matrix or in molecule-like defects.

Concerning this, the determination of the properties in the cluster-rich oxides and the trapping characteristics are of eminent interest for the understanding of the charge storage mechanism. Therefore one part for the motivation of this work is the understanding of the trapping behavior of ion beam synthesized nanocluster-rich SiO_2 layers. In order to characterize the influence of the implanted ion species on the trapping properties both, Si^+ and Ge^+ ion implantation was performed. Several authors report very short times for data retention which do not meet the requirements of non-volatile memories (e.g. [Dutt99, Ohzo94, Ohzo96, Guo97, Shen98]). Therefore in this work the retention is investigated in detail, especially at elevated temperatures. Additionally the work is focused on application related issues with the aim to integrate the process into a commercial production line. A straightforward approach starting from MOS capacitors, going to single transistors and finally leading to the formation of a prototype of a 256k nv-SRAM was thus chosen.

Various approaches for silicon based light emitters are discussed in section 2.4. Starting from porous silicon, different methods for the formation of silicon based light emitters are reported. In this study, ion beam synthesis is used for the formation of structures for novel types of memories and electroluminescent devices. One of the main problems of Si based light emitting devices based on the quantum confinement effects of nanoclusters or cluster related defects is their low efficiency. Unfortunately in most of the papers dealing with this topic no efficiency values are given at all. Typical values are below 10^{-5}. Therefore in this work optimizations of the devices were carried out in order to obtain higher power efficiencies. Another critical issue of modified SiO_2 layers used for light emission is the high operation voltage. Since electric fields >7 $MVcm^{-1}$ are necessary for the excitation of the electroluminescence (EL), a device with an oxide layer thickness of several hundred nanometers (e.g. 500 nm in [Rebo99]) requires operation voltages of several hundred volts. Such high voltages do definitely not meet the requirements of modern microelectronics. Therefore an important task of this work is the investigation of thinner oxide layers in order to reduce the operation voltage of the EL devices. Further investigations of this work are related to the PL and EL from SiO_2 layers implanted with different ion species. Sn^+ implanted layers were already investigated regarding the PL [Rebo00b] but for any application related issues EL is much more interesting. Additionally, Si and C co-implantation was carried out as a novel approach for more stable EL devices. Furthermore, in this work the direct integration of the Si based light emitter into an integrated optocoupler was successfully tested in order to check the suitability of the emitter for future device applications.

The main goal of this work is to investigate correlations between microstructural, electrical and optical properties of the devices. Chapter 3 gives an overview about the fabrication process and the methods used for the characterization of the devices. The microstructure of the devices is described in chapter 4 and the results of electrical and optical investigations are presented in chapter 5 and 6, respectively. The aim of the investigations is to get a better understanding of the charge transport, the charge storage and the mechanism of the electroluminescence. This knowledge is necessary for the further optimization of the devices and for possible applications.

2. Nanoclusters in SiO_2 - layers

2.1. Physical properties of nanostructures

Nanostructures are of great interest for applications in microelectronics because of their unique quantum effects. These very special features are also promising for future applications optoelectronics and interdisciplinary fields like the interface between conventional technologies and biotechnology. Quantum confinement effects describe the change of the material properties of elements or compounds as a function of the size of crystallites or clusters. One of the predictions of the quantum confinement effect is the enlargement of the band gap and the increase of the radiative recombination rate with decreasing size of nanostructures. The solution of the one-dimensional Schrödinger - equation gives for the energy eigenvalues of electrons in an rectangular potential well with infinitely high walls:

$$E_n = \frac{\pi^2 n^2 \hbar^2}{2 m_e R^2} \tag{2.1}$$

Here n is the main quantum number, R is the width of the potential well and m_e is the mass of electrons. This relative simple model already shows the increase of the bandgap with decreasing size proportional to $1/R^2$.

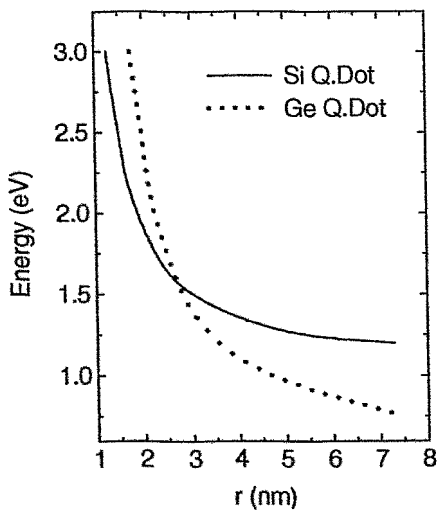


Fig. 2.1:
Bandgap of crystalline and spherical Si and Ge nanocrystals as a function of the cluster radius (after [Taka92]).

Calculations of the bandgap as a function of cluster size for real systems and comparison with experimental data can be found e.g. in [Buur98, Kim97, Trwo98, Vepr97]. All the calculations and experimental investigations show a strong dependence of the bandgap on the size of the clusters. For clusters consisting of amorphous silicon (a-Si) or hydrogenated a-Si the increase in bandgap size is lower than that of crystalline clusters [Alla97]. This means that, if a radiative band transition is present, small changes in the nature and the size of the small nanoclusters will cause a noticeable shift of the emission wavelength. Furthermore, this implies that the distribution of cluster sizes plays an important role for the broadening of luminescence peaks. Fig. 2.1 shows the bandgap energy as a function of the cluster radius [Taka92].

The increase of the radiative recombination rate k_R of excitons with smaller nanocluster size is another interesting effect. Both silicon and germanium have an indirect bandgap and therefore the decay time of the exciton for radiative recombination is relatively long and the exciton can travel over large distances. The probability for non-radiative recombination by passing a trap center is distinctly higher than for radiative recombination. However, with decreasing cluster size the number of traps in the vicinity of the exciton decreases. Thus in smaller nanocrystals the probability for radiative recombination is higher compared to larger crystallites containing more defects. This has to be mentioned because of the occurrence of both surface and volume defects with different defect densities optimum cluster sizes with minimum probabilities for non-radiative recombination exist.

For radiative recombination at an indirect bandgap an additional phonon is necessary carrying a defined momentum. The smaller the nanocrystal size, the stronger the exciton is localized and the momentum of the exciton has an higher uncertainty because of the well known Heisenberg uncertainty relation:

$$\Delta p \cdot \Delta x \geq \frac{\hbar}{2} \tag{2.2}$$

where $\hbar$ is Planck's constant and Δp and Δx represent the uncertainties of momentum and spatial coordinates, respectively. With decreasing cluster size the momentum transmitted by the phonon becomes more variable and k_R increases. In extremely small clusters this leads to a situation where Δk is larger than the difference between conduction and valence band in k-space so that finally no phonon is anymore necessary [Vepr97]. However, for Δk being of the order of the Brillouin zone extension, the cluster size is of the order of the Si lattice constant.

2.2. The system Si / SiO_2

2.2.1. Silicon dioxide: structure and properties

With the development of microelectronics in the early sixties, enormous activities started aiming to improve the process materials. Silicon as the basic material for microelectronic technology became one of the most investigated elements of the periodic table. One of the main reasons for the success of silicon has been its unique oxide and the quality of the interface between the oxide and the silicon substrate. Today silicon dioxide (SiO_2) is the most important material used for isolation in microelectronic devices. Its versatile properties like good electric isolation because of the high bandgap, its easy production process and the compatibility to the silicon substrate can hardly be topped by other materials. Many workers have investigated reliability, long-term stability, the influence of radiation and possible processes to improve the radiation hardness and also various stress related issues, especially the Si/SiO_2 interface. However, even now after about 50 years of ongoing activities a lot of problems are still not fully resolved as are many application related tasks. The main topic of today's research in microelectronics is the decrease of the gate oxide thickness to meet the requirements of future ULSI chip generations predicted by the SIA roadmap [SIA00].

The structure of SiO_2 is based on tetrahedra consisting of a Si atom in the center and four O atoms in the corners. The tetrahedra are connected to each other at the corners and form rings with 3 up to 8 tetrahedra. Because of this variable ring size, the angles between the tetrahedra are in the range of 120 ... 180° and therefore some physical properties like density, refractive index and bandgap vary. In reality the SiO_2 network is not free of defects since the various processing steps and the production environment lead to the formation of imperfections. Disturbances in the short-range order of the SiO_2 network, such as oxygen vacancies, interstitials or under-coordinated Si (dangling bonds) are associated with additional energy levels in the band gap of the SiO_2. These defects are of great importance in MOS technology, which explains the efforts in searching for correlations between their structure with electric properties. Such electronic states in the bulk SiO_2 and especially close to or at the interface Si/SiO_2 are expected to affect both the current voltage (IV) and the capacitance voltage (CV) characteristics of a MOS device.

The following section gives a short overview about possible defects in SiO_2. The amorphous SiO_2 network can be described by a ≡Si-O-Si≡ bond structure. During ion implantation the bonds of the SiO_2 network may be destroyed. The occurrence of atomic defects can be observed by two different methods: electron spin resonance (ESR) [Afan00] and luminescence investigations, where the spectral characteristic provides the evidence for different defects [Skuj00, Grisc00]. If the Si-O bond is broken, the so called E' center may be formed. It consists of a Si atom having one dangling bond (trivalent Si) $\equiv Si^{\bullet}$. The formation can be described by two processes: firstly, by ionizing irradiation and secondly, by hole trapping of strained $(\equiv Si\text{-}O\text{-}Si\equiv)^{*}$ bonds [Gris89].

$(\equiv Si\text{–}O\text{–}Si\equiv)^{*} + E \rightarrow \equiv Si^{\bullet}\ {}^{\bullet}O\text{–}Si\equiv$ ionizing radiation

$(\equiv Si\text{–}O\text{–}Si\equiv)^{*} + h^{+} \rightarrow \equiv Si^{\bullet}\ {}^{+}O\text{–}Si\equiv$ hole trapping

The E' center may act as a hole trap becoming positively charged after capturing a hole and it is neutral when it remains empty. If such an E' center is located at the Si-SiO_2 interface it can act as an interface state. Different types of the E' center are known [Warr92] depending on the chemical bond structure in the surrounding region of the defect. The classic Fowler-Feigl-Yip or composite E' center has the structure $\equiv Si^{\bullet}$ ...$^{+}Si\equiv$ and is positively charged in its paramagnetic state. In the neutral state which is the case for a well annealed, unstressed sample, it cannot be detected by the ESR technique [Kaln90b]. Another possible configuration of a broken Si-O-Si bond is the so called nonbridging oxygen hole center (NBOH) with the structure $\equiv Si\text{-}O^{\bullet}$. The NBOH is also detectable by ESR because of the unpaired spin of the single electron. By capturing of an OH group a peroxyl bond H-O-O-Si$\equiv$ is formed. For a detailed review on the defects in SiO_2 the reader is referred to [Naza99].

E' centers can also be transformed into neutral oxygen vacancies (NOV), a special kind of so called oxygen deficiency centers (ODC). The structure of a NOV defect can be expressed as $\equiv Si\text{-}Si\equiv$. It is formed if the bridging oxygen atom is knocked out of its former position. NOVs are known to act as both, hole and electron traps [Rudr87, Hori97]. If two oxygen bonds of a Si atom are broken the so called twofold-coordinated Si is formed. Instead of Si also other group IV elements implanted into SiO_2 cause the formation of ODCs. The implantation of Si or other group IV elements (e.g. Ge or Sn) leading to an overstoichiometric environment of Si, Ge or Sn and subsequent annealing steps must a priori create such Si-Si, Ge-Si, Ge-Ge, Sn-Si or Sn-Sn linkages and therewith lead to the formation of ODCs.

A lot of activities have been dedicated to the fabrication of SiO_2. The thermal oxidation process was steadily improved over the last decades and during the last years a strong interest in alternative methods for the production of SiO_2 could be observed. During the thermal oxidation the interface occurs as a SiO_x - monolayer ($1 < x < 2$) on a single crystalline silicon substrate. Following that a strained region exists on which the stoichiometric amorphous SiO_2 is situated. Because of the ongoing thinning of gate oxide layers and the necessity for the reduction of the total thermal budget thermal processes for oxidation are tried to be replaced by other techniques, e.g. plasma processes or sputtering methods. However, for these very thin oxide layers with a thickness below 1.5 nm (today: 2.0 nm) the requirements concerning reliability and interface quality are very strong since the influence of the interface Si/SiO_2 on the properties of the devices becomes more and more important [Guse00].

2.2.2. Charges in the Si / SiO_2 system

For electrical investigations MOS (Metal - Oxide - Semiconductor) capacitors as a special kind of the MIS (Metal - Insulator - Semiconductor) structure are used. Fig. 2.2 shows a schematic picture of a MOS capacitor. It consists of a SiO_2 layer on top of a Si substrate. The gate contact is made of Al (or ITO and poly-Si for EL and memory devices, respectively) which is lithographically patterned into dot structures. On the backside of the wafer an Al layer is deposited.

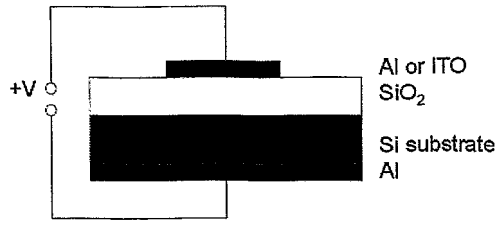


Fig. 2.2:
Schematic of a MOS - capacitor. The device is contacted at the gate (dot on top of the SiO_2 layer) and a Al layer on the backside of the wafer.

For a typical MOS - capacitor structure the total capacitance can be calculated as a series of two capacitors.

$$\frac{1}{C} = \frac{1}{C_{OX}} + \frac{1}{C_{SC}} \tag{2.3}$$

Here C_{ox} is the capacitance of the oxide and C_{SC} that of the space charge region below the Si/SiO_2 interface in the bulk Si. For the typical capacitor the following equation is valid:

$$C_{OX} = \varepsilon_r \cdot \varepsilon_0 \cdot \frac{A}{d_{OX}} \tag{2.4}$$

where ε_r is the relative dielectric constant of the oxide, A the area of the capacitor plates and d the distance between the two plates. The following explanations are valid for n-type silicon. In accumulation, which is for positive gate voltage, a very narrow space charge region occurs in the Si. Because of this thin region the capacitance C_{SC} is very large and with formula (2.3) C becomes constant with $C = C_{ox}$.

If a very small negative voltage is applied to the gate a depletion zone on the $Si-SiO_2$ interface occurs. This zone can reach a width of several 100 nm. With increasing negative voltage this depletion zone becomes broader and the capacitance C_{SC} decreases and also C decreases. Finally the depletion zone reaches a maximum value on which inversion occurs. The process of the generation of charge carriers however is very slow and cannot follow the high frequency of the measurement signal. So for HF-CV the capacitance C remains constant on a minimum value for a further increase of the negative voltage.
The charges in a MOS device can be classified as follows (see Fig. 2.3):

1. Interface trapped charges Q_{it} located at the interface Si / SiO_2 with energy states in the silicon bandgap. The charge exchange with the Si can occur in very short times. Such traps are created by excess silicon (trivalent Si), excess oxygen or by impurities at the interface.

2. Fixed oxide charges Q_f located at or near the interface. These charges are immobile under an applied electric field.

3. Oxide trapped charges Q_{ot}. These traps are distributed in the volume of the oxide layer and can be created by radiation damage or hot electron injection.

4. Mobile ionic charges Q_m, mainly Na^+ or K^+ ions. These Alkali-ions have a negative influence on the reliability behavior of MOS devices because of their high mobility. To protect microelectronic circuits from these contaminations cleanroom processing is necessary. Additional protecting layers like Si_3N_4 are used to prevent the indiffusion of these mobile ions from outer sources.

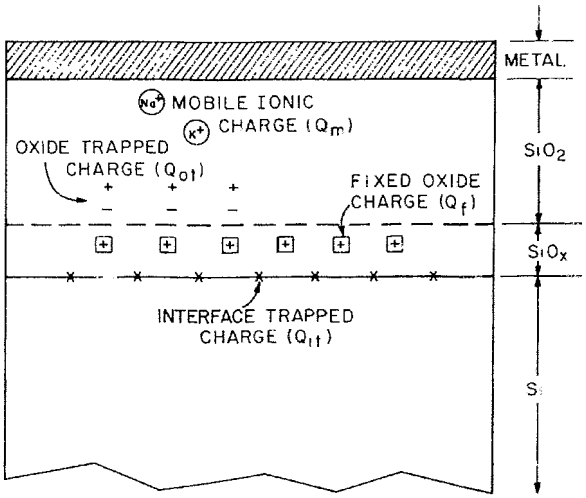


Fig. 2.3:
Types of charge in a MOS - device (after [Sze81])

The sum of Q_f, Q_{ot}, Q_{it} and Q_m is the so called oxide charge. Fixed oxide charges lead to a change in the HF-CV-characteristics as shown in Fig. 2.4. The shift of the CV curve is a measure for the fixed oxide charge Q_f, but one has always to consider the location of the charges in the oxide layer. So the measured charge is more or less an effective charge.

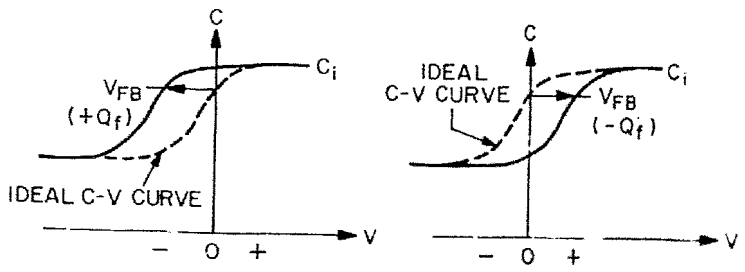


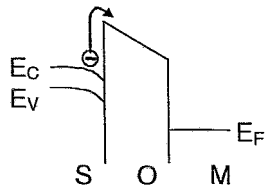
Fig. 2.4:
HF-CV curve of a MOS - capacitor (n-type Si) with different oxide charges. Positive charges lead to a shift towards negative voltages. negative charges cause a shift towards positive voltages. (after [Sze81])

2.2.3. Charge injection and transport through SiO_2 layers

The following section gives a short overview about possible injection and conduction mechanisms in SiO_2.

Schottky – Emission:

This mechanism describes the thermal emission of an electron into the conduction band of the insulator. The equation (2.5) describes the current density J, where A^* is the effective Richardson constant, T the measuring temperature, k Boltzmann's constant, Φ_B the barrier height, e the electron charge, ε_0 the dielectric constant, ε_p the specific dielectric constant and E the applied electric field [Sze81]. Because of the high barrier of the system Si/SiO_2 Schottky emission should not play an important role for investigations at temperatures close to room temperature. The plot on the left side shows the band diagram of the metal-oxide-semiconductor (MOS) device.

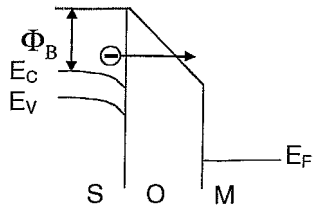


$$J_{SE} = A^* \cdot T^2 \cdot \exp\left(-\frac{e(\Phi_B - \sqrt{\frac{eE}{4\pi\varepsilon_r\varepsilon_0}})}{kT}\right) \qquad (2.5)$$

Fowler-Nordheim tunneling (FN):

If the applied electric field E becomes high enough, the probability for the tunneling of electrons into the conduction band increases. The tunneling of electrons through any high barrier shows only a rather weak temperature dependence which is related to the influence of the temperature on the energy distribution of the electrons. Therefore the increase in the current with temperature is due to the electrons having an energy between the Fermi energy E_F and $E_F + kT$. However, this gives only a weak thermal influence to the tunneling characteristics. A detailed description of this temperature dependence, which occurs to be $J \sim T^2$ is given in [Hest86]. As a special case, the tunneling of highly energetic electrons is known as Fowler-Nordheim injection, described by equation (2.6) [Hori97]. In the derivation of the basic FN-formula which is valid for strong bias usually any temperature dependencies are neglected. The exponential term is a measure of the tunneling probability and therewith independent of the temperature.

The current density at FN injection is expressed as:



$$J_{FN} = \frac{A}{4\Phi_B} E^2 \exp\left(-\frac{2B \cdot \Phi_B^{\frac{3}{2}}}{3E}\right) \tag{2.6}$$

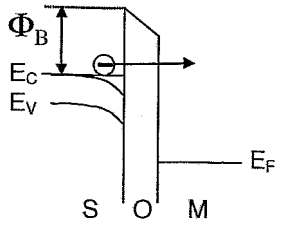
where: $$A = \frac{e^2}{\hbar} \tag{2.7}$$

and $$B = \frac{2\sqrt{2em^*}}{\hbar} \tag{2.8}$$

Here ħ is Plancks constant and m^* is the effective electron mass in the SiO_2. By plotting the results of IV measurements in a diagram with the ordinates $\ln(J/E^2)$ as a function of 1/E one can determine the effective barrier height for the FN injection if m^* is known.

Direct tunneling (DT):

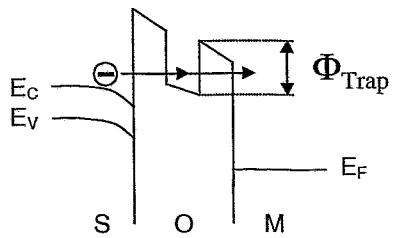
For very thin layers (<4 nm) tunneling trough the trapezoidal barrier becomes possible. This mechanism is known as direct tunneling (eq. 2.9) [Hori97]. Here A and B are the constants given by (2.7) and (2.8), d_{ox} is the thickness of the oxide layer and V is the voltage which is applied to the gate.



$$J_{DT} = \frac{A}{d_{ox}^2}\left[\left(\Phi_B - \frac{V}{2}\right) \cdot e^{-Bd_{ox}\sqrt{\Phi_B - \frac{V}{2}}} - \left(\Phi_B + \frac{V}{2}\right) \cdot e^{-Bd_{ox}\sqrt{\Phi_B + \frac{V}{2}}}\right] \tag{2.9}$$

Trap assisted tunneling (TAT):

Insulators containing traps show an increase in the current at an electric field in the range of 4...7 $MVcm^{-1}$. The mechanism is strongly connected to the density and type of defects. Following the work of Chen et. al [Chen88] modifications and simplifications of the TAT - model were made in order to find an analytical solution of the equation which can be basically described by the following formula [Flei92, Houn99]:

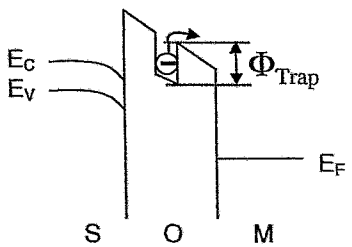


$$J_{TAT} \sim \exp\left(-\frac{4\cdot\sqrt{2qm^*}}{3\hbar}\Phi_t^{3/2}/E\right) \qquad (2.10)$$

Here E is the electric field across the oxide and Φ_t the trap energy level below the conduction band of the SiO_2.

Poole-Frenkel-conduction (PF):

This model corresponds to the field induced thermal emission of electrons from traps in the volume of the insulator. The Coulomb-potential of the traps is decreased by the applied electric field. The effect is bulk limited and similar to the Schottky-effect at the electrodes. The PF effect describes the decrease of a Coulomb-potential caused by an external electric field. Assuming a single trap with the energetic depth Φ_{Trap} below the conduction band the current density of PF - conduction (J_{PF}) can be expressed as



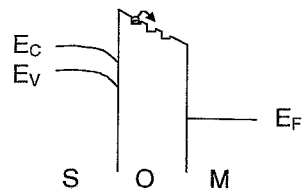
$$J_{PF} = \sigma_0 \cdot E \cdot \exp\left(-\frac{\Phi_{Trap} - \Delta\Phi_{Trap}(E)}{kT}\right) \qquad (2.11)$$

where $\Delta\Phi_{Trap}(E) = \sqrt{\frac{q\cdot E}{\pi\varepsilon_0\varepsilon}}$ (2.12)

is the decrease of the trap depth caused by the high electric field [Sze81]. σ_0 is the electric conductivity of the layer system at low electric fields. A good review concerning PF conduction is given in [Hill71].

Hopping conduction (HC):

One of the thermally stimulated conduction processes is the so called "hopping" conduction. Electrons pass through shallow traps close to the conduction band. This effect leads to an enhancement of the current with increasing temperature. The process is limited by the volume and can be described by:



$$J_{HC} \sim E \cdot \exp\left(-\frac{\Delta E_{ah}}{kT}\right) \tag{2.13}$$

where ΔE_{ah} is a measure for the activation energy.

Space Charge limited current (SCL):

The charging and discharging effects of traps inside the insulator may lead to the buildup of space charge which takes strong effect on the conduction processes [Rose55]. The current density can be described as:

$$J_{SCL} = \frac{8\varepsilon\varepsilon_0\mu}{9d_{ox}^{\ 3}}V^2 \tag{2.14}$$

where d_{ox} is the thickness of the insulator layer, μ is the mobility and V the applied voltage. A special case of the SCL is the trap filled limited (TFL) current. It describes the current after filling of all the traps and can be usually observed as a sharp increase in the current with a power law dependence. It can be expressed as:

$$J_{TFL} \sim E^{\left(\frac{T_c}{T}+1\right)} \tag{2.15}$$

where T_c is a parameter describing the trap properties. A detailed description of this mechanism is given in [Rizz77].

2.3. Memories based on nanocluster-rich SiO_2-layers

This section describes the main issues related to the use of SiO_2 layers containing nanostructures for memory applications. The following parameters will be discussed in detail: the programming voltage and pulse time which is used to perform the write/erase procedure, the programming window defined as the shift of the threshold voltage, the data retention, describing the possible time of data storage without refresh cycles and the endurance, which is the maximum possible number of write/erase cycles.

2.3.1. Advantages of nanocluster memories

Today Electrically Erasable Programmable Read Only Memories (EEPROM) are the most common type of non-volatile (nv) memories. They usually consist of a gate oxide layer including a so called floating gate as shown in Fig. 2.5a. Their principle of operation is based on the injection of electrons into the floating gate (Fig. 2.6a) which leads to a shift of the threshold voltage of the metal oxide semiconductor field effect transistor (MOSFET). Therewith, it is possible to distinguish between two different states "0" and "1" of the MOSFET (Fig. 2.6b). The shift of the threshold voltage depends on the amount of the injected charge and the parameters of the layer system. EEPROMs exhibit a very long retention time, typically more than 10 years. For a detailed review on the common EEPROM technology the reader is referred to [Brow98].

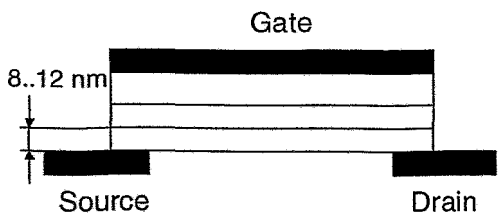


Fig. 2.5a:
Schematic of a floating gate memory cell. The floating gate (marked as grey area) lies in a distance of about 8..12 nm from the Si/SiO_2 interface.

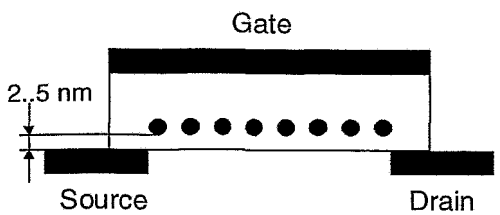


Fig. 2.5b:
Nanocluster memory cell. A layer of nanoclusters is positioned at 2..5 nm from the interface.

To achieve non-volatility of the memory the thickness of the gate oxide has to be chosen in such a way that leakage currents are minimized. The time to lose 20% of the charge stored in the floating gate for instance is 10 years for 60 Å gate oxide thickness, 1 day at 50 Å but only 5 min at 45 Å [Mode99]. However, in order to apply direct tunneling for charging of the floating gate the layer thickness of the gate oxide has to be < 50 Å. This

means that such a device could not meet the requirements of non-volatile memories. On the other hand the charging by means of the injection of electrons into thicker gate oxides is only possible at high electrical fields. However, this will lead to a increasing oxide degradation because of hot electrons.

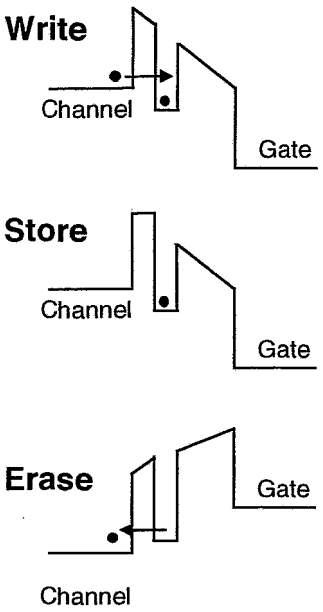


Fig. 2.6a:
Band diagram of a nv-memory. By applying positive or negative voltage to the gate, a "write" or "erase" cycle is performed, respectively.

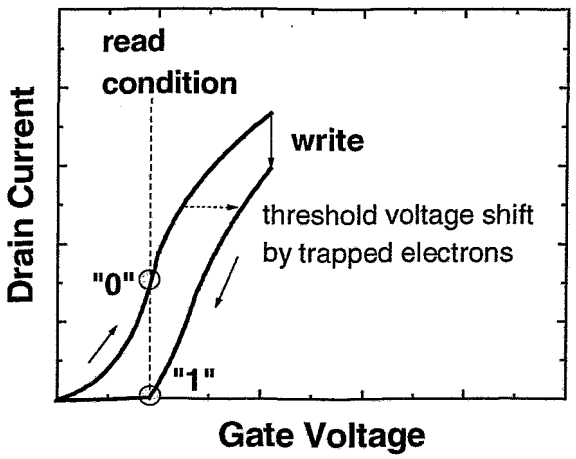


Fig. 2.6b:
Working principle of a nv-memory. The shift of the threshold voltage leads to two different states "0" or "1", which can be detected via current sensing at a fixed read condition.

Starting with the work at IBM in the mid-90ties [Tiwa95, Tiwa96a, Tiwa96b] strong activities towards the application of nanoclusters in novel non-volatile memories have developed. The concept of this new type of a memory is based on nanoclusters in the gate insulator of the FET as shown in Fig. 2.5b. So basically the nanocluster layer replaces the floating gate of the common EEPROMs. By charging or discharging of these nanoclusters the threshold voltage of the transistor is influenced. This principle is comparable to the common EEPROM technology but shows important advantages:

- The write / erase voltages are in the range of 2 .. 5 V because of a ultrathin gate oxide layer which allows direct tunneling. This is much less than the typically used 12 .. 15 V for common EEPROMs. This fact is of great importance especially for the use of such nv-memories in modern mobile communication applications, for smart cards and also with respect to the growing market for embedded systems.
- Because of the very thin gate oxide between the Si / SiO_2 interface and the cluster layer the charging and discharging of the clusters can be carried out by direct tunneling. The high electric fields, which are usually required to perform FN -

tunneling for the programming of EEPROMs, can be prevented. The stress on the oxide is reduced which leads to a significant increase in the endurance (number of possible write / erase cycles). For nanocluster based memories it reaches values > 10^{10} which is much superior than the common values of 10^5 .. 10^6 for EEPROMs.

- The charge is stored in separated clusters isolated from each other by the SiO_2 matrix. Such systems are also described as „floating dot" devices. Because of the „digital" storage conditions the information is kept even if several clusters lose their charge. This is a main advantage compared to floating gate systems, where all charge is lost if a leakage path is present.
- With the decrease in the size of the nanostructures up to the nm-range, quantum effects start to dominate the charge storage. This causes a significantly longer charge storage leading to improved retention characteristics of the device.

The techniques which were used to achieve the desired properties will be discussed in the following part of this chapter.

2.3.2. Nanocluster memories based on deposition techniques

The main technological challenge in the production process of nanocluster memories is the formation of a cluster band with densely packed clusters at a distance of <5 nm from the Si/SiO_2 interface, with a homogeneously distributed size of the clusters. The control of the distance from the interface is a key feature to obtain well defined conditions for charging and discharging of the clusters. Therefore different deposition techniques like chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), magnetron sputtering, laser ablation and aerosol spraying have been used to produce nanoclusters. Very first investigations of Si-rich SiO_2 layers were already carried out in the beginning of the eighties [DiMa80, DiMa84]. The development of cluster-rich oxide layers for memory applications took a rapid increase after the publication of Tiwari [Tiwa95, Yano94]. The investigated FET structures with Si nanoclusters were produced by CVD. Shen et al. [Shen98] used a stack structure consisting of a Si-nanocrystal layer and a poly-Si floating gate produced by means of PECVD. The achieved programming window was distinctly higher than for samples with only a floating gate and no nanocrystal layer. Another advantage of the stack structure is the strongly reduced writing time. However the retention of the stack-device dropped down drastically (down to 10s).

The influence of interface traps on the storage properties of Si-cluster layers was studied in [Shi98]. The model of the discharging by tunneling of the electrons from the clusters towards interface traps was investigated for different interface properties. For this case the amount of interface traps is increased by means of vacuum annealing or decreased by means of hydrogen annealing. In [Shi99] the retention characteristics shows only a very weak temperature dependence. This implies that the charge storage is really caused by a direct charging of the clusters and is dominated by quantum confinement effects. The structures were produced by means of low pressure CVD (LPCVD). Ohba et al. [Ohba00]

describe a method using a 1 nm thick a-Si layer, which is deposited on a 3 nm thermal oxide. After vacuum annealing crystalline clusters were found. The investigated devices show a programming window of 0.5 V and a retention of only 10^4 s. The authors claim that quantum confinement effects dominate the charge storage. But since a vacuum annealing step was performed, this statement should also consider interface states which could influence the charge trapping characteristics. The short retention time might be an indication that not only cluster related charge trapping occurs.

A single electron memory (SEM) is described by Durrani et al. [Durr99, Irvi00]. They investigated a lateral SEM device (L-SEM) using a so called memory-node, which can store up to 10^6 electrons. The writing is performed using nanowires. The structure is operated at 4.2 K. Referring to the authors it should be possible to optimize the device for the operation at 77 K. In [Irvi00] the successful operation at 45 K is observed. The main problem of the several approaches for SEM is the low temperature required for device operation. According to a review on SEM devices [Wass98] room temperature operation becomes only possible for feature sizes below 3nm. This strong need for low operation temperatures for most of such devices is the major limitation for the introduction into commercial applications.

2.3.3. Nanocluster memories produced by ion beam synthesis

A very promising method for the production of nanostructures is ion beam synthesis (IBS). This technology combines the versatile method of ion implantation with additional high temperature treatment of the modified layers. Because of the well tunable process parameters it is a suitable and reproducible technique attracting more and more attention. The properties of the nanoclusters can be controlled by the ion energy, the ion fluence and the parameters of the following annealing process. The general features of IBS can be described as follows: At the initial stage of ion implantation the implanted oxide layer becomes supersaturated by the implanted ion species. If the implanted ions are sufficiently mobile during the process of ion implantation, small precipitates of the implanted atoms and their compounds with the matrix atoms may be formed. For atoms which are not mobile during the ion implantation these nucleation processes are even stronger during the post implantation annealing at elevated temperatures. During this annealing step, the precipitates grow and coarsening of the nanoclusters occurs due to Ostwald ripening. With increasing size of the nanoclusters coalescence processes contribute to the coarsening. If the implanted ion fluence is sufficiently high, the coalescence of the nanocluster precipitates may even lead to the formation of a buried layer in the matrix.

MOSFET structures with Si^+ implanted SiO_2 gates were produced by Ohzone [Ohzo94, Ohzo96]. The used Si concentrations were in the range of 1 .. 15 at.%. The observed endurance value is 10^{11}. The implantation of Si^+ [Hana96, Ohzo96] and Ge^+ ions [Hana95, Hana96] into SiO_2 layers with subsequent annealing processes can be used for the formation of nanocluster based memory structures. Hao et al. [Hao93a] investigated SiO_2 layers with a thickness of 21 nm implanted with $3x10^{15}cm^{-2}$ Si^+ (10 keV) ions. Annealing was performed in a furnace at 950°C for 35 min. No Si clusters were detected.

The observed memory effects are explained by a trap assisted charge storage which is known for Si-rich SiO_2 layers [Kaln90a].

A significant dependence of the endurance characteristics on the implantation energy was found by Ohzone [Ohzo96]. 50 nm SiO_2 layers implanted with 50 keV Si^+ ions showed up to 10^{11} write/erase cycles while oxide layers implanted with 25 keV Si^+ ions showed only up to 10^9 cycles. The pulses for writing / erasing were applied at an electric field of 8 $MVcm^{-1}$ for 10 µs. The endurance is strongly enhanced with increasing ion fluence. For 25 keV Si^+ implanted SiO_2 layers the observed endurance was 10^3 , 10^8 and 10^9 cycles for fluences of 1, 2 and $3x10^{16}$ cm^{-2}, respectively. The energetic position of the traps causing the charge storage is determined to be 3.0 or 2.4 eV below the conduction band of SiO_2 [Kaln90a].

In [Thee00] SiO_2 layers with a thickness of 20 and 30 nm were implanted with Ge^+ or Si^+ ions at energies ranging from 6 .. 20 keV to fluences of $1x10^{15}$ ... $1x10^{16}$ cm^{-2}. After the implantation furnace annealing (900°C, 30 min) or rapid thermal annealing (RTA) at 950°C for 30 s was performed. The MOS capacitors were produced in a standard LOCOS (local oxidation of silicon) process. A summary of the microstructural results is given in [Bora99b]. Electrical characterization was carried out using IV and CV measurements. The observed memory effect increases with Ge concentration, however, the retention time for Ge implanted structures is relatively short. In comparison to this Si implanted SiO_2 layers show a smaller programming window size but very good retention even at elevated temperatures (up to 250°C). After storage for 90 h at 250°C the programming window is still larger than 0.5 V [Gebe99]. This already shows that the characterization of the binding structure of Ge or Si in the cluster-rich region of the SiO_2 layers is of great importance for the understanding of the charge storage and transport mechanisms.

A comparison of the memory properties of devices produced by different methods is given in [Hana96]. Comparable systems with a tunnel oxide thickness of about 20 Å show a strongly reduced write- and erase time for devices produced by ion implantation. For write times of 300 ns with a 4 V write pulse a threshold voltage shift ΔV_T of 0.3 V is observed whereas a write time of 3 µs is necessary to achieve the same ΔV_T for deposited layers. Hanafi explains this increase of the electron capture cross-section by a factor of 10 with a broader depth distribution of the Ge clusters in the layers produced by ion beam synthesis. This should lead to a decrease of the effective oxide thickness for the injection. The observed effect is even more dramatic for the erase times. Ion implanted layers show erase times in the millisecond-range while deposited clusters show times in the range of several seconds. Microstructural investigations are not described in [Hana96] but the electrical results, especially the reduced write/erase times, lead to the assumption that apart from the charge storage in Ge clusters other ion beam induced traps have to be taken into account. The ΔV_T window of SiO_2-layers implanted with Ge or Si were found to be comparable indicating an analogous charge storage mechanism for Ge- and Si-nanoclusters. However, results concerning the retention and endurance properties of the devices are not reported in [Hana96] and so a direct comparison to our results [Gebe01a, Bora02] is not possible. The following table gives an overview on the memory parameters of relevant articles. It is sorted according to the element (Ge or Si) used for the formation of the nanostructures.

Ref.	Structure	El.	Programming window	Retention	Endurance
[Hana95] [Hana96]	12 nm SiO_2, 10 keV Ge^+ impl.	Ge	0.3 V at 4 V pulses (300 ns)	after 10^5s at RT no change	10^9 cycles measured, no change
[Hana96]	20 nm SiO_2, 20 keV $7.5x10^{14}cm^{-2}$ Ge^+ impl.	Ge	0.4 V at 3 V (10µs) 0.3 V at 7 V (300 ns)	n.a.	n.a.
[Kape99]	9 nm SiO_2, 3 keV Ge^+ $5x10^{15}$ cm^{-2} $1x10^{16}$ cm^{-2}	Ge	0.2 V at 10V (3 ms) 0.5 V at 10V (3 ms)	n.a.	n.a.
[Kape99]	12 nm SiO_2, 3keV Ge^+ $5x10^{15}$ cm^{-2} $1x10^{16}$ cm^{-2}	Ge	0.3 V at 13V (3 ms) 0.5 V at 13V (3 ms)	n.a.	n.a.
[Gebe99] [Thee00]	30 nm SiO_2, 20 keV Ge^+, $5x10^{15}$ cm^{-2}	Ge	2.0 V at 10 V pulses (10 ms)	about 1 h at 250°C	10^5
[Gebe01a] [Bora02]	20 nm SiO_2 implanted with 12 or 20 keV Ge	Ge	12 keV: 1 V 20 keV: 4V at 12.5 V (100 ms)	< 1h at RT about 10 h at RT	
[Hao93a] [Hao93b]	21 nm SiO_2, 10 keV $3x10^{15}cm^{-2}$ Si^+ impl.	Si	0.5V at 12V (10 µs)	300 h, prognosis: 10a no change also at 100°C	10^9 cycles measured
[Ohzo94] [Ohzo96]	50 nm SiO_2, 25 keV $3x10^{16}cm^{-2}$ Si^+ impl.	Si	8 V at 30 V pulse (10 µs)	1000 s	10^9
[Tiwa95] [Tiwa96a]	1.5 .. 3.0 nm oxide + Si clusters + 7 nm control oxide	Si	0.55 V (at 3V, write: 1µs, erasing: ms pulses)	>1 week at RT, >> 1h at 85°C	10^9 measured, prognosis up to 10^{13} cycles
[Ohzo96]	50 nm SiO_2, 50 keV $1x10^{16}cm^{-2}$ Si^+ impl.	Si	15 V at 40 V (10 µs)	n.a.	10^{11} prognosis: $3.3x10^{15}$
[Hana96]	20 nm SiO_2, $1x10^{15}cm^{-2}$ Si^+ impl.	Si	0.52 V, 3 V (10µs)	n.a.	n.a.
[Guo97]	SOI, poly-Si Q.-Dot (9 nm), operated at RT	Si	discrete shift in 55 mV steps	5 s	n.a.
[Shen98]	Stack of floating gate, Si – NC (PECVD) + 9 nm Tunnel oxide	Si	3.4 V (at +10V, and – 5V, 50 ns)	10 s	minimum 10^7
[Shi98] [Shi99]	Si channels on SOI substrate, 3 nm SiO_2, Si LPCVD clusters, 30 nm Gate oxide	Si	0.83 V at 2 $MVcm^{-1}$ pulses	about 10^5 s	n.a.
[Dutt99]	SIMOX, electron beam writing, 25..45 nm Si Cluster, operated at 20 K	Si	0.56 V at 2.5 V pulses	4 h	n.a.
[Ohba00]	3 nm SiO_2, 1 nm a-Si, vacuum anneal, 50 nm control SiO_2	Si	0.5 V at 10 V pulses	about 10^4 s at RT	n.a.
[Gebe99]	30 nm SiO_2, 12 keV Si^+	Si	4.6 V at 6.25 $MVcm^{-1}$ (100ms)	>90 h at 250°C	
[Gebe01a] [Bora02]	20 nm SiO_2, 6 keV Si^+	Si	2 V at 12.5 V, 100 ms pulses	> 1 week at 200°C	10^6

Table 2.1: Summary of memory parameters of different approaches for the formation of nanocluster-rich nv-memories. References given in bold letters are part of this work and will be discussed in detail in chapter 5.

2.4. Optoelectronic properties of nc-rich SiO_2 layers

2.4.1. Silicon based light emission from nanocluster-rich SiO_2 layers

Silicon is the standard material of the common microelectronics industry. However, due to its indirect bandgap and the small optical dipole matrix element it is highly inefficient as a light source. Therefore at first sight integrated optical systems in Si-technology do not seem to be possible. Much effort has been devoted to solve the problem of the physical inability of silicon for light emission in the visible wavelength range. The following section gives a short introduction into the different approaches. First, some important parameters which will be used in the following are explained. Efficiency and stability are of great importance for the application of optoelectronic devices. Industrial requirements are based on a minimum of 10000 hours of operation at the typical operation temperature, mostly 85°C. The following list gives an overview on the common parameters used to describe the efficiency of the electroluminescence:

- the internal quantum efficiency (IQE):
  describes the ratio between the number of emitted photons and injected electrons in a single luminescence center
- the external quantum efficiency (EQE):
  describes the ratio between the total number of emitted photons and injected electrons of the whole device
- and the power efficiency (PE):
  describes the ratio between the optical output and electrical input power

In general the following relation is valid: IQE > EQE > PE. In this paper the PE is used to describe the efficiency.

Starting with the successful photoluminescence (PL) investigations from porous silicon (PS) in the beginning of the nineties [Canh90, Lehm91] a lot of activities in the field of Si-based optoelectronics were launched. Not only the light-emitting properties of porous silicon but also its suitability as wave-guide, modulator and detector is of great interest for optoelectronic applications. A detailed review on porous silicon is given by Canham [Canh96]. However, the complicated production process for porous silicon showed quite early the missing suitability of PS for integrated solutions in the common silicon technology.

Other approaches for silicon based light emission are the implantation of erbium into modified SiO_2 layers. The emitted wavelength of these structures is in the infrared range (1.5 μm) and therefore of great interest for optical communication. These structures and their properties will not be discussed in this work here. The reader is referred to several excellent review papers on this topic [Polm97, Coff98].

Another interesting system used for Si based light emission is the controlled formation of defects in the Si substrate. Dislocation loops in Si are produced by means of boron implantation and subsequent annealing steps [Svei96]. The produced dislocations introduce

a strain field in three dimensions. This leads to a modification of the bandgap in such a way that silicon itself can be used to provide confinement in three dimensions. In actual investigations of such structures an EQE of $2x10^{-4}$ was observed [Ng01].

The formation of Si- or Ge-nanocluster-rich SiO_2 layers is another promising approach for silicon based light emission. Several techniques like LPCVD [Tomp94, Nass98], PECVD [Fors95, Wang98b], magnetron sputtering [Atwa94, Qin96, Seif98,], laser ablation [Yosh98], and, last but not least, IBS were used to produce such layers. Several papers describe the PL of these systems. Blue PL from Si and Ge implanted SiO_2 layers was described in the mid nineties [Rebo97, Liao96a, Bao97]. The PL intensity of Ge implanted layers was found to be distinctly higher than that for Si implanted layers. The spectra of PL and EL show similar peaks which implies that the same centers cause the luminescence. The strong violet EL at RT from Ge^+ implanted samples is visible with the naked eye [Rebo97]. The nanostructures were produced by ion implantation of Ge and a following annealing step. From samples containing an approximately box like implantation profile which is produced by double implantation at different energies a better electrical stability is observed [Rebo99, Gebe00a]. The comparison with sputtered Ge rich SiO_2 layers shows a much stronger luminescence for the devices produced by IBS which can be explained by the synergy of changes in the stoichiometry and the high energy deposition during ion implantation [Rebo00b].

The success of the PL observations of several research groups lead to an enormous increase of the activities in this field and gave useful hints for the understanding of the luminescence mechanism and the ongoing optimization of the devices. However, for any kind of practical applications in micro- and optoelectronics the EL is of much greater interest than the PL. For EL up to now no satisfactory explanation is available. ODC in the amorphous network of the SiO_2 are the mainly discussed luminescence centers. The publications related to EL from Si or Ge rich SiO_2 layers can be divided into two groups:

- The excitation occurs at high electric fields ($E>5$ $MVcm^{-1}$). Fowler-Nordheim tunneling or trap assisted tunneling regimes are the dominating processes. Electrons tunneling through the oxide in a FN - regime lead to the excitation of the luminescence centers. This implies that mainly hot electrons cause the luminescence by impact excitation.
- A few authors report on EL which is excited at low electric fields [Liao96b, Lute00, Mull99, Zhan99]. In this regime usually relatively high current densities (of the order of 1 Acm^{-2}) are necessary to achieve luminescence.

The following sections give an overview on articles concerning EL-devices and their properties. The methods for the fabrication of EL devices emitting in the visible wavelength range can be divided into two groups, namely deposition techniques and ion beam synthesis.

2.4.2. Approaches for Si-based light emission using deposition techniques

Nassiopoulou et al. [Nass98] observed EL based on quantum confinement effects (700-800 nm) and on localized defects (500-600 nm) in Si-rich SiO_2 layers produced by LPCVD. The current densities necessary to achieve EL are relatively high (1.75 Acm^{-2}) but the authors observed a stability of several hours, and using thicker thermal oxides (18 nm) even up to several days. The presented spectra cover only a range of 450-850 nm, and therefore no further information about the occurrence of violet luminescence of the structures is possible. The IV characteristics can be described by FN tunneling and a symmetric shape for positive and negative bias of the IV curve was observed. After high-field stress the formerly symmetric IV curve shows a rectifying behavior. Forsythe [Fors95] observed also a symmetrical IV characteristics for Si rich oxide layers which were produced by means of CVD. At temperatures of 240 K a reduction of the current of one order of magnitude and a drastic decrease of the EL intensity was observed. The EL peak found at 380 nm did not shift for lower temperatures.

EL from oxinitride layers was described in [Pric99]. The EL spectra show a redshift compared to the PL ones. EL peaks are observed around 410 and 495 nm. The efficiency is found to be $4x10^{-6}$ for forward and $7x10^{-7}$ for reverse bias. The large difference for the different polarities may be explained by the reduced amount of hot electrons which is available at reverse bias.

Wang et al. [Wang99] observed EL from native SiO_2 layers on Si contacted with an indium-tin-oxide (ITO) layer, which were subsequently annealed. Two peaks occur, one at 360 nm and the second one at 820 nm. The peak in the UV is assumed to be caused by ≡Sn-Sn≡ or ≡Sn-Si≡ centers. This implies that diffusion of Sn atoms from the ITO layer into the native SiO_2 layer takes place during the high temperature step after the ITO deposition. The shift of the spectra towards shorter wavelengths is explained by the heavy - atom - effect. In [Yuan99] EL from similar devices consisting of an Ag contact on native SiO_2 are reported. The relatively broad spectrum shows a peak at 650 nm.

Yoshida et al. [Yosh98] found a non-linear dependence of the EL intensity on the excitation current for an EL-peak at ~750 nm. The samples containing Si nanocrystallites were produced by pulsed laser ablation. The luminescence intensity shows a power law relation $I_{EL} \sim j^a$ with a=3.5. This behavior is explained by impact ionization of the injected minority charge carriers and the ongoing radiative recombination.

2.4.3. Ion beam treated SiO_2 layers for Si-based light emission

Ion implantation appears to be the dominating method for the formation of EL devices. Knapek et al. [Knap98, Mull99] found blue EL at 470 nm with an EQE of $6x10^{-7}$ for 540 nm SiO_2 layers implanted with Si^+ ions. The implanted fluences were relatively high ($1.2x10^{18}$ cm^{-2}). The electric field necessary for the excitation of the EL was at about 5 $MVcm^{-1}$ and the current density $>10^{-4}$ Acm^{-2}. These currents at such "medium" electric fields indicate a strong damage of the oxide. The authors claim that device breakdown

occurred if higher electric fields were applied. The EL is definitely caused by defect induced luminescence centers in the SiO_2 because the clusters sizes determined by TEM are larger than 15 nm, which does not allow a cluster based luminescence in the visible wavelength range. Another important effect is the reduction of the conductivity after high temperature annealing, which indicates a decreasing concentration of the implantation induced defects. The EL intensity however is increased. One could argue that during annealing the electrically active defects are modified into other defects which can act as luminescence centers. Obviously the electric field for excitation plays a significant role for the EL because after annealing the currents at higher fields are lower but the EL intensity increases.

Song et al. [Song97] compared PL and EL spectra of 34 nm thick Si^+ implanted SiO_2 layers. They found a different shape of the PL and EL spectra and fit the spectra by 3 different peaks. For PL the peaks at 470 and 730 nm are dominant. However for EL these peaks are only weak and the spectra are dominated by a peak at 600 nm. The single peaks are explained as followed: the 470 nm peak is caused by NOV, the 600 nm - peak by NBOH centers or self-trapped excitons and the 730 nm-peak is caused by the luminescence of Si-nanocrystals. However, no influence of the annealing on the 730 nm peak was found. This indicates that quantum confinement is not a likely reason for this peak because in this case the annealing should cause a shift of the peak towards higher wavelengths due to growing clusters.

Matsuda et al. [Mats97] found EL from 50 nm thick SiO_2 layers implanted with Si. The structures were prepared in a LOCOS process and the Si implantation was performed at energies of 20 and 50 keV to fluences of 1..3 x 10^{16} cm^{-2} resulting in a relatively high amount of excess Si (up to 20 atomic percent). The investigated wavelength range of the EL is 400 - 900 nm. The spectra of both the implanted and the pure oxides show similar peaks around 550, 650 and 780 nm. The EL intensity of implanted layers is only 2 orders of magnitude higher than for the pure oxide and shows only a weak dependence on implantation fluence and energy. Since the shape of the spectra does not change significantly in the investigated wavelength range after implantation only an increase in implantation induced defects should lead to the enhanced EL. The EL intensity increases towards 400 nm for the implanted samples while it decreases for the pure oxide which could be attributed to the formation of ODC during ion beam synthesis. The IV curves shift towards lower electrical fields for higher Si concentrations.

Ovchinnikov [Ovch00] observed blue and orange EL from Si - implanted SiO_2 layers (130 nm) with an external quantum efficiency of 1x10^{-4}. After etching of 20 or 30 nm of the modified SiO_2 layer the orange luminescence was significantly decreased while the blue luminescence remained unchanged. The authors explain this by a reduction of the nanoclusters causing the orange luminescence and draw the conclusion that the blue luminescence is caused by centers close to the SiO_2 / Si interface.

The understanding of both the influence of the implanted excess Si or other group IV elements and the implantation induced damage is a main issue for an optimized processing of EL devices. Garrido [Garr97] observed an increase in the EL intensity of one order of magnitude for Ar^+ implanted SiO_2 layers compared to pure thermal oxide. In addition to the peak observed in pure SiO_2 at 650 nm and 288 nm an additional peak at 460 nm was

found. Another comparison of Ar^+ implanted SiO_2 layers with pure SiO_2 show only a slightly enhanced PL peak at 290 nm which disappears at moderate annealing [Rebo99]. This implies that not only the radiation damage caused by the ion implantation but the combination with changes in the stoichiometry are necessary for the luminescence. The reason therefore is that excess Si (or atoms of other group IV elements) enhances the formation of Si-Si bonds leading to the formation of ODC, which cause the luminescence.

Several authors report on EL from modified SiO_2 layers under operation at low electric fields. The observed high current densities indicate that the excitation mechanism of such structures is completely different to samples discussed in the previous section. Zhang et al. [Zhan99] implanted Ge^+ ions at an energy of 120 keV into 120 nm thick SiO_2 layers. EL with a sharp peak at 400 nm and a broad peak at 600 nm was observed. Interestingly the voltages used for EL excitation were extremely low. The broad EL peak at 600 nm is observed at 5 and 7 V for samples with Ge fluences of 10^{16} cm^{-2} and 10^{17} cm^{-2}, respectively. The sharp 400 nm peak is only observed for the sample with the lower Ge-dose if a voltage of at least 30 V is applied. Regarding the efficiency no comments are made. During EL operation the devices show remarkable high currents with values of the order of several Acm^{-2} even at quite low electrical fields of 1.5 $MVcm^{-1}$. For devices with the higher implantation fluence the peak at 400 nm peak disappears but the 600 nm peak can still be observed with a ten times lower intensity. This is explained by the high electric fields necessary for the impact ionization to excite the Ge-ODC which can not be reached at layers containing such high doses of Germanium. The IV-characteristics of the devices indicate that the system is highly conductive and that the insulating properties of the SiO_2 have changed completely. The high current at the low electric fields cannot be explained by the common models of TAT or FN-tunneling.

Luterova et. al [Lute00] describe EL from a Si implanted sol-gel SiO_2 layer. The spectra of PL shows a peak at about 430 nm which is related to defects while the EL shows a broad spectrum between 600...800 nm and no blue luminescence. The IV characteristics shows an ohmic behavior for both polarities and the current density reaches extremely high values of several Acm^{-2} at low voltages of +/- 10V. The EL is only observed when positive bias is applied to the substrate (n-type Si) and it is only visible in tiny spots randomly distributed over the device area. The authors claim that the EL is caused by electron hole recombination. The occurrence of the small EL spots and the high current density leads to the assumption that local breakdown spots cause this red luminescence. Blue EL cannot be excited since the strongly reduced resistance of the implanted oxide layer does not allow electric fields which are high enough to perform impact ionization of hot electrons. A similar behavior was observed by Shcheglov [Shch95] for Ge-implanted $Si/SiO_2/Si$ stacks. The EL was also only detectable at reverse bias and electric fields of about 1 $MVcm^{-1}$ had to be applied. Also, the light was only emitted in several spots of the gate contact which should be related to local non-uniformities in the gate oxide thickness.

The following table gives an overview on articles concerning Si based EL from material systems based on modified oxide layers.

EL observed at high electric fields (>5MVcm^{-1}):

Reference	wavelength (nm)	efficiency	Parameters	mecha-nism	remarks
[Bai98]	640-660	n.a.	3 nm natural SiO_2		EL as a result of bipolar injection of holes and electrons
[Baru97]	600 (broad)	n.a.	Si + 50 nm SiN_x + 10 nm Au	FN	EL at neg. bias, at pos. bias no EL, cluster related luminescence
[Bota96]	290, 460, 650	n.a.	Ar impl. SiO_2, const. current, 2μA		ODC
[DiMa84]	250-830	EQE: <10^{-6}	Si rich oxide (13 % Si), CVD		cluster related EL
[Fran02]	~850 nm	n.a.	SiO_x (80 nm) by PECVD	TAT FN	electron-hole pairs in Si-nc by impact ionization
[Fors95]	380, 600-800	n.a.	Si rich oxide (1μm), PECVD		cluster related EL
[Fujita95]	650, 570	EQE: $5x10^{-5}$	a-Si layer with Si-NC		nanocrystals
[Gebe00a] (sect. 6.2.1)	400	PE: 0.5 %	Ge implanted 130 nm SiO_2	FN	ODC
[Garr97]	288, 460, 650	n.a.	Ar implanted SiO_2		ODC
[Kame99]	infrared	n.a.	Si impl. SiO_2		Si-NC
[Knap98]	450-520	EQE: $6x10^{-7}$	Si impl. SiO_2 (operation at 5.2MVcm^{-1}, BD at higher fields)	FN	
[Kozl97]	460	n.a.	Si^+ impl. SiO_2		defects
[Lali99]	650-800	n.a.	Si^+ impl. SiO_2 12-18 nm layers, $1x10^{17}$ cm^{-2}, operation at 9-13 MVcm^{-1}	FN	nanoclusters
[Mats97]	650 + EL at <500 nm	n.a.	Si^+ impl. SiO_2 50 nm layers, 1..$3x10^{16}$ cm^{-2}, operation at 35..55 V	FN	impurities
[Nass98]	500-600 and 700-800	n.a.	5-10 nm therm. SiO_2 + Si rich oxides, deposited by LPCVD (about 20 nm), operation at 7-9 V	FN / TAT	quantum confinement for 700 - 800 nm, localized defects for 500 – 600 nm
[Ovch00]	460 and 770-880	EQE: $1x10^{-4}$	Si implanted 130 nm SiO_2 layers $5x10^{16}$ cm^{-2}, operation at > 100 V	FN / TAT	defects and also Si nanoclusters
[Pric99]	410, 495	forw. bias: $4x10^{-6}$, rev. bias: $7x10^{-7}$	oxynitride layers (50 nm)		double injection, recombination
[Qin96] [Qin99]	640	n.a.	Si / Ge rich oxides or oxynitride, 8 nm, RF - sputtered	FN	defects in the SiO_2, no cluster lum., (spectra for Si and Ge are comparable)
[Rebo97b]	366, 407, 455 420-470	PE: $5x10^{-4}$ PE: 10^{-4}	Ge^+ impl. SiO_2 Si^+ impl. SiO_2 (500 nm SiO_2, oper. at 380 V)	FN	ODC, ≡Si-Si≡ , ≡Ge-Si≡ or ≡Ge-Ge≡
[Song97]	470, 600, 730	n.a.	Si^+ impl. SiO_2, 34 nm SiO_2, 25 keV, $1x10^{16}$ cm^{-2}		NBOH center / self-trapped exciton

this work (sect. 6.2.2)	390, 480	PE: $2.4x10^{-4}$	Sn^+ implanted, 200 nm SiO_2	FN	ODC, ≡Sn-Sn≡ or ≡Sn-Si≡
this work (sect. 6.2.3)	450 450-500 and 375	PE: $6x10^{-6}$ PE: $1.3x10^{-5}$	Si and C co-implanted, 360 nm SiO_2 7.5 or 10 % excess Si / C 5 % excess Si / C	FN	defects of the type $Si_yC_{1-y}O_x$
[Tomp94]	370, 630	n.a.	Si rich oxide, LPCVD deposition from SiH_4: GeH_4:N_2O gas mixture		red EL is attributed to nanocrystals
[Wang98a]	600	n.a.	NC-Si in a-Si / a-SiN_x:H super-lattices produced by KrF excimer laser annealing		quantum confinement
[Wang98b]	530	n.a.	PECVD a-Si:H film, cw Ar^+ laser annealing		EL due to anode hole injection
[Wang99]	360, 820	n.a.	ITO / native SiO_2 / Si, subsequently annealed, operated at 6 V	FN	≡Sn-Sn≡ or ≡Sn-Si≡ centers for 360 nm EL
[Yosh98]	750	n.a.	Si-nc by laser ablation		impact ionization
[Yuan98]	640	$1x10^{-5}$	mechanically damaged SiO_2 layers on Si		NBOH - center
[Yuan99]	620-640		native SiO_2 on Si, 5 nm, operation at 5 V (forw. bias)	FN	NBOH - center
EL observed at low electric fields:					
[Liao96b]	620, 730	n.a.	Si^+ impl. SiO_2 300 nm layers, $2x10^{16}$ cm^{-2}, operation at 15 V	operat. at low E	implanation induced defects
[Lute00]	720 (PL: 430)	EQE: $1x10^{-7}$	250 nm SiO_2 (sol-gel), Si^+ impl. (20..70 keV, $5.5x10^{15}$ .. $3x10^{16}cm^{-2}$), operated at 10V	at low E	radiative recombination of injected holes and electrons, only neg. bias
[Mull99]	470	$6x10^{-7}$	Si^+ impl. SiO_2 (750 nm), $1.2x10^{18}$ cm^{-2}, 160 keV Si^+, operation at about 280 V	TAT (?) (mid E)	implantation induced defects, no cluster luminescence
[Shch95]	broad spectrum, increase in the IR range	estimated PE: 10^{-5}..10^{-4}	Ge^+ impl. SiO_2 (70 nm), 1..$4x10^{16}$ cm^{-2} Ge^+ operated at 1 $MVcm^{-1}$		Ohmic behavior
[Tong96]	640, 730	n.a.	Si rich oxide, PECVD, 300 - 400 nm thick, operat. at 20 V		
[Zhan99]	400, 600	n.a.	Ge^+ impl. SiO_2 120 nm SiO_2, 120 keV Ge^+, 10^{15}, 10^{16} u. 10^{17} cm^{-2}, operation at 5 ... 30 V	operat. at very low E	ODC

Table 2.2: Summary of EL-parameters of different approaches for the formation of nanocluster-rich oxide layers. References given in bold letters are part of this work and will be discussed in detail in chapter 6.

3. Experimental

This chapter gives an overview about the methods used for sample preparation and characterization. It provides also information concerning the process parameters in a summarized form.

3.1. Sample Preparation

3.1.1. Structure of the MOS - devices

Two and three inch wafers of n - type (100) Silicon were used as substrate material. The native oxide layer was etched back using HF acid. Subsequently the Si substrate was thermally oxidized to form a SiO_2 layer. Oxide layers with a thickness of up to 200 nm were produced by means of dry oxidation, thicker layers by wet oxidation. After the oxidation the ion implantation was performed (see section 3.1.2 for details). Following that the annealing procedures (see section 3.1.3) were carried out and different metal contacts were deposited depending on the specific electric and optoelectronic investigations. For simple MOS capacitors a 300 nm Al layer was sputter-deposited on the front side and was lithographically patterned. For the memory structures poly-Si was used as gate contact. These devices were produced in standard LOCOS technology [Hill95]. A 300 nm Al layer was sputtered on the backside of the wafer as a back contact.

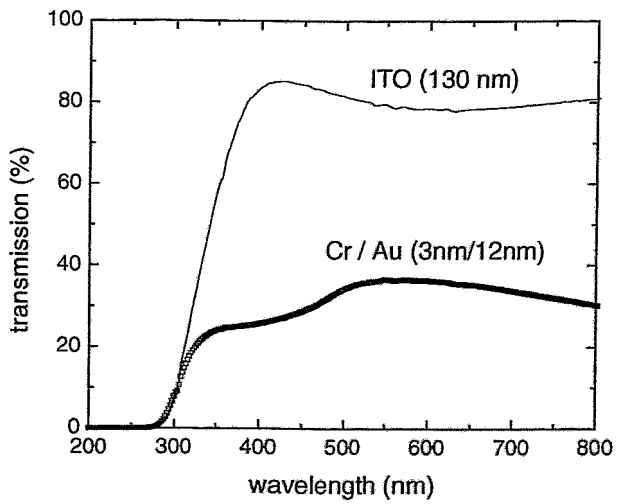


Fig. 3.1:
Transmission of ITO and ultrathin Au layers. The transmission of the Au layer is about 27%, for the ITO layer about 80% at a wavelength of 400 nm.

The investigation of the electroluminescence requires transparent and conductive gate electrodes. Indium-tin-oxide (ITO), a special kind of a transparent conductive oxide (TCO) was deposited using a sputtering process. The thickness of the layers was 80 ... 130 nm. Patterning was performed using standard lithography. The typical sizes of the devices were 1 mm or 0.5 mm in diameter in a periodic pattern of 2 mm pitch. Because of the poor thermal stability of the ITO layers (stable only up to 200°C) no contact anneal was performed. In other publications methods for the formation of transparent electrodes using ultrathin aluminum or gold-layers (< 20 nm) are described [Zhan99]. Typically at temperatures >250°C the ITO starts to dissociate [Borc00]. This may be one reason for the breakdown at high field operation. In future applications alternative materials may be used e.g. ultrathin metal layers. Since no homogenous gold layers with a thickness around 10 nm can be formed because of the possible island formation, a thin Cr layer is used as an interfacial layer. First tests were carried out using a 3/12 nm Cr/Au system. Fig. 3.1 shows the transmission spectra of such ultrathin Cr/Au layers in comparison to a 130 nm thick ITO layer. For the ITO layer a transmission around 80% was achieved at a wavelength of 400 nm, while the Cr/Au layer system shows only 27%. However, with thinner metal layers and the possible operation at higher current densities similar EL intensities could be achieved.

3.1.2. Implantation conditions

The ion implantation was carried out at room temperature unless stated otherwise. However, depending on the ion current density an increase in the sample temperature up to about 100°C was observed in some cases. The implantations were performed at an angle of 7° off axis to prevent channeling effects. In this work the isotopes ^{12}C, ^{28}Si, ^{40}Ar, ^{74}Ge and ^{120}Sn were used. Ge^+ implantations at energies >60 keV were carried out with a 500 keV implanter manufactured by the company "High-Voltage-Engineering". Implantations with energies of 15...50 keV were performed with a home-built implanter. For low-energy (<12 keV) ion implantation a special designed chamber mounted to a 200 keV Danfysik-implanter was used. An ion beam with an energy of 30 keV was decelerated by means of an electrical field down to 2 keV. A detailed description of this special design is given in [Teich01].

3.1.3. Annealing conditions

High temperature treatment of the structures was performed to anneal implantation induced defects and to enhance the formation of nanoclusters. The annealing was carried out by different methods. Conventional furnace annealing was used for long-term treatment at temperatures of 400 ... 1000°C for 30 ... 60 min. Rapid thermal annealing (RTA) was used for short time annealing (1 ... 150 s) at temperatures of 950 ... 1150°C. The annealing of

the memory structures (up to 30 nm oxide thickness, for details see Table 3.1) was carried out using RTA at 950°C for 30 s. The atmosphere during annealing was nitrogen unless otherwise mentioned. Flash lamp annealing (FLA) was also performed on several samples using the unique FLA apparatus of the Research Center Rossendorf. It can deliver thermal spikes up to 2000°C in a millisecond range. In this work pulses of 1000...1300°C for 20 ms were used.

3.1.4. Parameters of the investigated sample sets

For the investigated memory structures SiO_2 layers implanted with Ge^+ or Si^+ ions were used. A summary of the parameters used for the memory structures is given in Table 3.1. The implanted ion fluence was chosen in order to achieve peak concentrations at the projected range (R_p) around 3.5 .. 10 at%. The displacements per atom (dpa) are given in the table as a measure of the damage at the interface.

Implantation	R_p (nm)	d_{ox} (nm)	Fluence ($x10^{15}$ cm^{-2})			
			3.5	5.0	7.0	9.0
12 keV Ge^+	13	20 30	5.0 % 1.4 dpa 0.04 dpa	7.1 % 2.0 dpa 0.06 dpa	10.0 % 2.8 dpa 0.08 dpa	-
20 keV Ge^+	18	20 30	3.5 % 5.9 dpa 1.0 dpa	5.0% 8.4 dpa 1.5 dpa	7.0 % 11.8 dpa 2.1 dpa	-
6 keV Si^+	11	20	-	5.6 % 1.0 dpa	7.7 % 1.4 dpa	9.9 % 1.8 dpa
12 keV Si^+	21	30	-	3.2 % 2.3 dpa	4.5 % 3.2 dpa	5.8 % 4.1 dpa

Table 3.1:
Parameters of the investigated memory structures. The given concentrations describe the maximum peak concentration of the implantation profile. Dpa–values are given at the Si/SiO_2 interface

For PL and EL investigations thicker oxide layers were used. The layers were implanted with Ge^+ or Sn^+ ions. Table 3.2 gives an overview of the implantation parameters. SiO_2 layers with a thickness of 80 nm were the most investigated samples. For this oxide thickness variations the implantation energy (30 ... 50 keV) and the fluence were carried out in order to get a direct correlation of these parameters to the EL, the IV and the trapping properties, respectively.

Beside the fabrication of Ge-, Sn- and Si-rich oxide layers the co-implantation of Si and C was carried out. The motivation was the possible formation of SiC-clusters in the SiO_2 matrix, which could provide efficient LC with very short decay times. For the formation of Si/C rich SiO_2 layers 350 nm thick layers were thermally grown on <100>-oriented, n-type Si-substrates at 1000°C. First, the oxide films were double-implanted with Si^+ ions at an energy of 90 keV followed by a second Si^+ implant at 47 keV. Three different samples were prepared. The fluences were chosen in such a way that a broad implant profile with a nearly constant concentration of excess Si at a depth of 60...180 nm below the oxide surface of about 5 %, 7.5 % and 10 % was formed, respectively. Table 3.3 gives an overview of the parameters. After the two Si-implantations the devices were furnace annealed at 1100°C for 30 min in a N_2 ambient. Then, C^+ ions at an energy of 43 keV were implanted, followed by a second C^+ implant at 22 keV. A post-implantation heat treatment at 800°C for 60 min followed by a final annealing step at 1100°C for 60 min was applied.

SiO_2 layer, oxide thickness	**Ion**	**Energy (keV)**	**Rp (nm)**	**Fluence ($x10^{15}$ cm^{-2}) to achieve peak conc. of:**			
				0.3 %	*1%*	*3%*	*6%*
50 nm	Ge^+	20	18		1.1	3.2	6.4
70 nm	Ge^+	30	25		1.4	4.3	8.5
80 nm	Ge^+	30 40 50	25 31 38		1.8	4.3 5.3 6.3	10.4
100 nm	Ge^+	50	38	0.6	2.1	6.3	12.6
130 nm	Ge^+	60	44		2.4		
160 nm	Ge^+	75	54		3.0		
200 nm	Ge^+	100	69	1.2	4.0	12.0	
500 nm	Ge^+	350 350+200	233 233+130			28.0 28 + 18	
100 nm	Sn^+	60	38		1.6	4.8	
200 nm	Sn^+	130	68		2.9	8.6	

Table 3.2:
Parameters of devices used for luminescence investigations. The fluences ($x10^{15}$ cm^{-2}) given in the four columns on the right side are related to the maximum peak concentrations of 0.3, 1, 3 and 6 %, respectively.

Implantation	**Implant**	**E (keV)**	**R_p (nm)**	**Fluence ($x10^{16}$ cm^{-2}) to achieve peak conc. of:**		
				5%	*7.5%*	*10%*
Si^+	1^{st} 2^{nd}	90 47	133 68	4.1 1.2	6.1 1.8	8.2 2.4
C^+	1^{st} 2^{nd}	43 22	131 68	3.4 1.5	5.1 2.2	6.8 3.0

Table 3.3:
Parameters of the Si / C co-implantations. Each element was implanted with two different energies to form a box like profile. The fluences ($x10^{16}$ cm^{-2}) given in the three columns on the right side are related to the maximum peak concentrations of 5, 7.5 and 10 %, respectively.

3.2. Microstructural investigations

This chapter gives a short overview about the methods used for the investigation of the microstructural properties of the MOS devices.

TEM

For transmission electron microscopy (TEM) a Phillips CM 300 microscope was used. The device was operated with a LaB_6 cathode at an acceleration voltage of 300 kV. The line resolution was 0.14 nm. Cross - section preparation of the samples was performed with the standard face-to-face glueing of the specimen and a dimpling method using sputtering with 5 keV Ar^+ ions.

RBS

Depth profiling of Ge^+ or Sn^+ implanted SiO_2 layers was done using the Rutherford backscattering method (RBS). He^+ ions with an energy of 1.7 MeV produced by a Van-de-Graff accelerator were injected orthogonal and detected at an angle of 10° off axis. The investigations were performed in a "random orientation" of the substrates preventing channeling effects. The RUMP simulation software was used to simulate the total fluence and the depth profile of the Ge / Sn atoms in the SiO_2 layers.

EDX

Energy dispersive X-ray spectroscopy (EDX) is another method which allows depth profiling of the Ge / Sn atoms. It is performed in the electron microscope using the electrons of the microscope e^- - beam, which is focused to about 10 nm for excitation. The electrons from the beam can hit electrons in the K-shell of an atom, thereby creating vacancies. Electrons from the other shells of the atom will fill the vacancy emitting element specific X-rays. The detected intensities of these X-ray lines give information about the density of the element in the layer. By scanning a significant line or area of a cross section sample with the focused electron beam, the EDX information can be used for depth profiling (STEM - EDX).

AES

Auger electron spectroscopy (AES) was used for the investigation of Si / C coimplanted layers. In combination with ion sputtering a depth profiling of the implanted layers was carried out.

XPS

X-ray induced photoelectron spectroscopy (XPS) as a method to investigate the binding properties of materials by measuring the ionization of electrons from the core levels was used to describe the structure of the nanoclusters observed in TEM.

3.3. Electrical Measurements

3.3.1. Current-Voltage (IV) and Capacitance-Voltage (CV) measurements

IV - Measurements were performed on a Süss PM-5 Waferprober using a Keithley 237 source measuring unit (SMU). A Keithley 590 CV-meter was used for HF-CV – investigations. The measuring frequency was 100 kHz. Both devices were computer operated with a self-made program using the Testpoint^{TM}-software [Test97] environment.

3.3.2. Determination of the charge centroid

The position of the charge centroid in the modified oxide layer is of eminent interest for applications. One method to determine this charge centroid is the photo - IV method [Wohl74,Wohl75, DiMa76, DiMa78, DeKe80]. This method is sensitive to internal fields in the oxide since the photocurrent characteristic of a MOS structure is determined by the barrier height and the position of the potential maximum in the insulator close to the interface of the injecting layer. Such internal fields are caused by trapped charges which influence the barrier height and the position of the potential maximum. In the experiment the traps are charged by applying an electrical field (typically <4 MVcm^{-1}) to the gate. The structure is kept under illumination with an halogen lamp. Following the charging an IV - curve is measured in the low field region (<2 .. 3 MVcm^{-1}) in accumulation and inversion. The shift of the IV curve along the voltage axis gives the information about the position of the charge centroid.

3.3.3. Trapping and reliability investigations by stress measurements

For investigations of reliability and long term stability of the modified oxide layers both constant current and constant voltage measurements were carried out. The measurements were performed using a computer operated Keithley 237 source measuring unit (SMU). The trapping characteristics were investigated by a method using a combination of IV - and CV measurements. IV - curves were driven up to a certain electric field, then a CV scan was recorded. The shift of the V_{FB} value is a measure of the trapped charge. Following this, another IV measurement starting from 0 up to breakdown of the device was performed, in order to investigate the stress induced leakage current (SILC).

When a MOS device is subjected to stress at high electric fields it will finally reach dielectric breakdown. The main difference of the dielectric breakdown to other MOS parameters is its statistical nature. This is because it is always the weakest defect, which leads to the breakdown. Thus, statistical data evaluation is required. Two methods are used to characterize the dielectric breakdown: first, the "time-zero" breakdown. In this method the applied voltage is ramped at high rates, thus enabling very rapid measurements and fast

data evaluation. Typically for this test >50 devices are used due to the statistical nature of the observed effect. Another method, which recently became more and more important is the time-dependent-dielectric breakdown (TDDB). In this method constant stress conditions are employed, either constant-voltage or constant-current stress. Longer test times are required in this case which leads to very time consuming measurements. However, this method is more straightforward with respect to the device reliability.

3.4. Optical properties

3.4.1. Photoluminescence

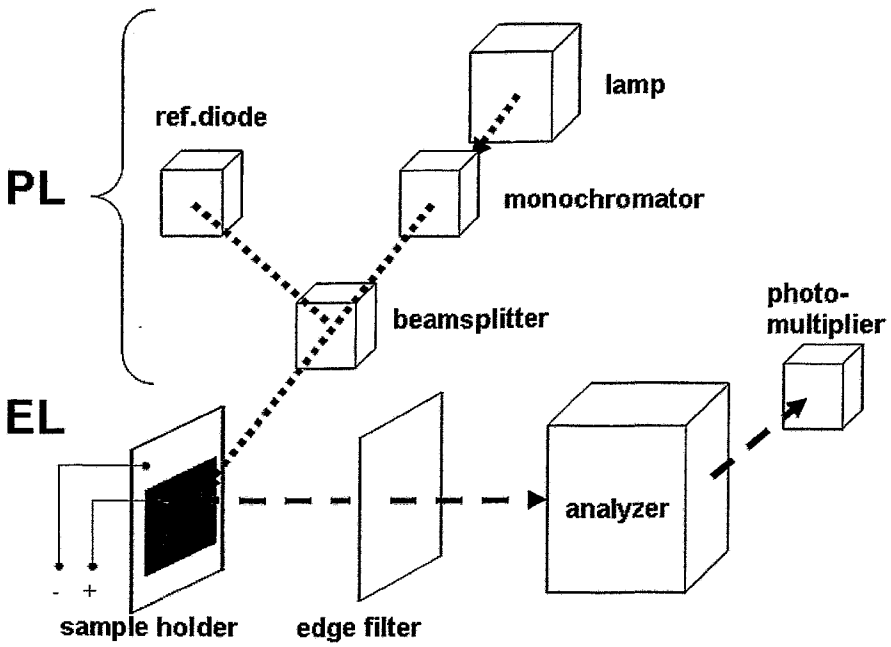


Fig. 3.2:
PL / EL setup consisting of a stage for excitation and the detection unit.

Photoluminescence measurements were performed using a SPEX Fluoromax-spectrometer. The schematic setup of this apparatus is shown in Fig. 3.2. The system consists mainly of the following parts: for excitation a Xenon lamp (power 150 W) with a continuous emission spectrum and a monochromator for wavelength selection are used. A part of the light used for excitation is transferred to a reference diode using a beamsplitter in order to measure the light intensity. The incoming light may then excite the PL of the sample which is mounted to a holder. An edge filter is used in order to block the excitation light in the detector. A second monochromator ("analyzer") allows the wavelength scanning of the emitted light which is then detected by a photo multiplier.

3.4.2. Electroluminescence

For electroluminescence measurements the PL setup described in 3.4.1. was slightly modified (Fig. 3.3). The optical excitation unit was replaced by a electrical excitation stage. A Keithley 237 SMU was used for the excitation of the MOS structures. The ITO front contacts of the devices were contacted with of a tungsten needle while the aluminum back contact was connected to a grounded gold plate. The detection unit was the same as in the case of PL investigations. For EL excitation the devices were operated under forward bias (positive voltage to the gate) in a constant current regime. For transient measurements of the EL, the voltage and the current, the experimental setup shown in Fig. 3.3 was used. A voltage pulse with an amplitude of 30 V and a pulse duration of 9 ms was added to a constant voltage of about 150 V. R_1 and C_1 were used to smooth the edges of the voltage pulse in order to obtain a defined time constant of about 3 µs. C_2 was used to bridge the constant voltage generator for AC pulses. Whereas the voltage transient is recorded by oscilloscope B, the current transient is monitored by oscilloscope A measuring the voltage drop across the 10 kΩ resistance. The EL transient measurements were performed by detecting the intensity yield at a photon emission energy of 3.18 eV (corresponding to a wavelength of 390 nm) with a water-cooled C4877 Hamamatsu photomultiplier tube and by analyzing it with a photon-counting multi-channel scaler (SR 430, Stanford Research Systems) triggered by the pulse generator. The time response of the detecting system is about 30 ns.

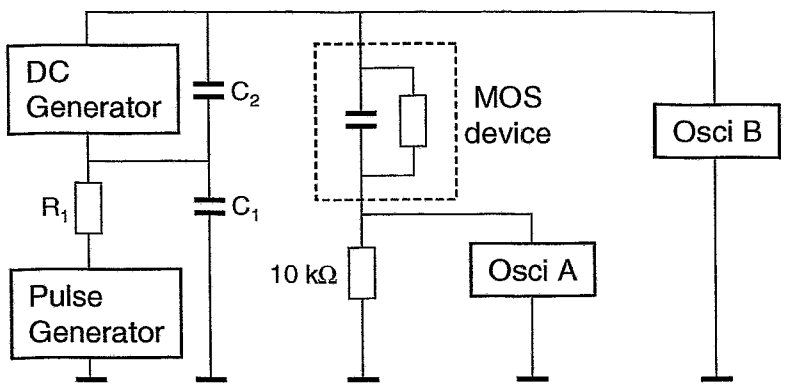


Fig. 3.3:
Setup for transient EL measurements. The current and the voltage were recorded by the oscilloscopes A and B, respectively.

4. Microstructure

4.1. Implantation profile and damage

The implantation of ions into a solid at a constant energy leads to the formation of a distribution in a specified depth region. This distribution with a Gaussian-like shape can be described by the projected range (R_p) and the projected range straggling ΔR_p. Calculations of the implantation profiles were performed with the TRIM-code [SRIM00]. The calculated implantation profiles for Si^+ and Ge^+ implantations for memory applications are shown in Fig. 4.1 for 20 nm SiO_2 layers and in Fig. 4.2 for 30 nm layers. All calculations were carried out in the full cascade mode. The closed symbols in the Figs. 4.1 and 4.2 are related to the concentration of the implanted ion species while the open symbols show the corresponding displacements per atom. The parameters were chosen in such a way that the peak of the profile was located at about half or 2/3 of the SiO_2 layer thickness. Additionally a 20 keV Ge implant into a 20 nm oxide layer was performed leading to a Ge-peak directly located at the interface SiO_2 / Si (Fig. 4.1). The calculated projected ranges are 13, 18, 11 and 21 nm for the 12 keV Ge, 20 keV Ge, 6 keV Si and 12 keV Si implants, respectively. A detailed description of the parameters is given in chapter 3.

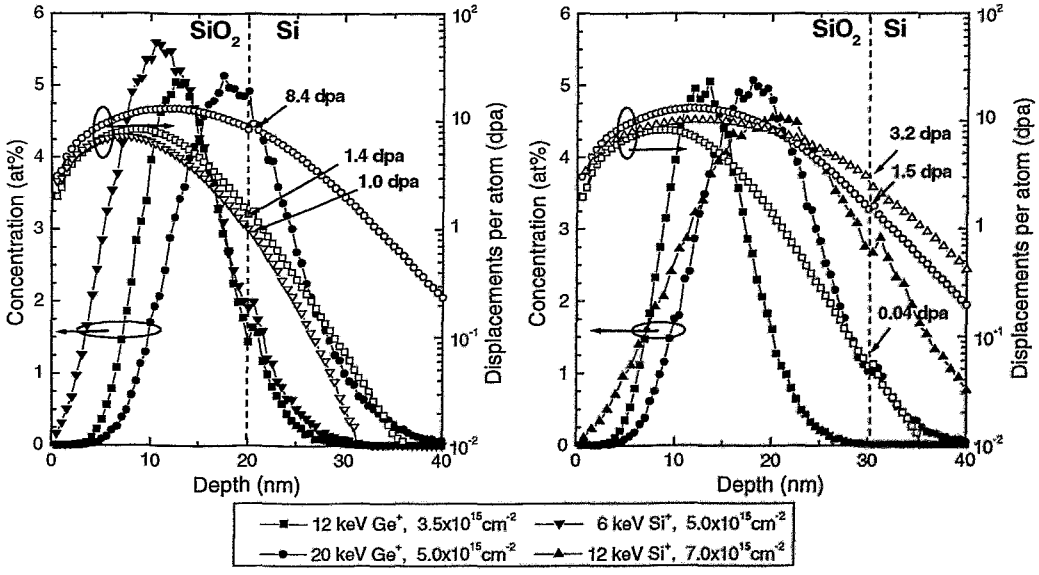


Fig. 4.1:
TRIM-calculation of Ge^+ / Si^+ implants into 20 nm SiO_2 layers. Closed symbols show the concentration, open symbols represent the dpa distribution profile.

Fig. 4.2:
TRIM-calculation of Ge^+ / Si^+ implants into 30 nm SiO_2 layers. Closed symbols show the concentration, open symbols the dpa distribution profile.

Since the properties of the SiO_2/Si interface play a dominant role for all injection and trapping processes, the interface damage induced by the ion implantation is of great interest. The plotted dpa-values are a good measure for this damage because they describe the changes in the SiO_2 network. Displacement-per-atom (dpa) values larger than one imply that every atom was displaced at last one time. This means that the network is totally destroyed during the implantation process. In order to compare results of structures with different implantation parameters, not only the concentration profile but also this damage has to be taken into consideration.

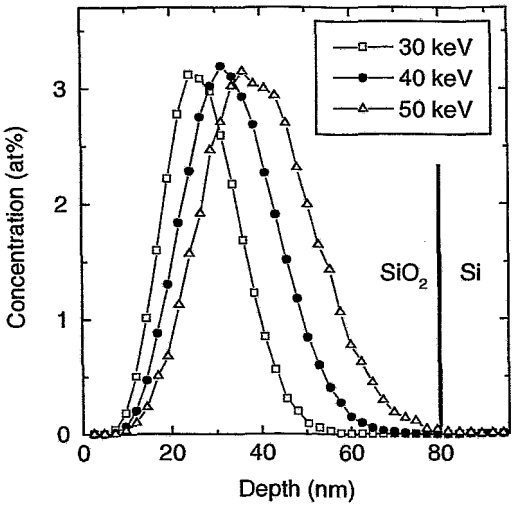


Fig. 4.3a:
Ge distribution of Ge implanted SiO_2 layers with a thickness of 80 nm. The profile was calculated using the TRIM-code [SRIM00].

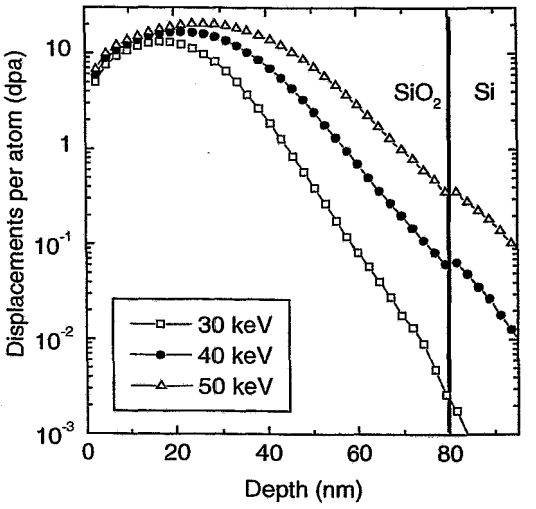


Fig. 4.3b:
Calculated dpa-values after Ge implantation (3% peak concentration). For the 50 keV implant 0.35 dpa are obtained at the interface.

For PL and EL investigations thicker oxide layers were used. The layers were implanted with Ge^+ or Sn^+ ions. Table 3.2 in section 3.1.4 gives an overview of the implantation parameters. Implanted SiO_2 layers with a thickness of 80 nm were the major materials used for electrical and electrooptical investigations. Fig. 4.3 shows a calculated TRIM - profile [SRIM00] for Ge^+ ion energies of 30, 40 and 50 keV. The implanted fluence was chosen is such a way that maximum peak concentrations of 3% were achieved as shown in Fig. 4.3a. For the 40 keV implant also concentrations of 1% and 6% were used (not shown here). The profiles show only a small variation of the R_p values, namely 25, 31 and 38 nm for the 30, 40 and 50 keV implants, respectively. The enormous effect of this shift on the dpa values at the SiO_2/Si interface is displayed in Fig. 4.3b. The values are 0.002, 0.06 and 0.35 dpa for the 30, 40 and 50 keV implants, respectively. This means that the damage at the interface is strongly enhanced with increasing implantation energy.

In order to investigate the possible formation of SiC clusters and the properties of Si/C rich oxide layers the co-implantation of Si^+ and C^+ ions was carried out. The calculated TRIM profile of the Si/C co-implantation (for 5% atomic concentration) is shown in Fig. 4.4. The parameter set was optimized in order to obtain a box-like profile for both ion species (see Table 3.3 in section 3.1.4 for details). First Si^+ ions were implanted at two different energies, displayed by the small circle symbols in Fig. 4.4. Then C^+ was implanted using again two single implantations at different energies to doses resulting in a nearly constant C concentration of about 5 %, 7.5 % and 10 % in the same depth region as the excess Si concentration. A post-implantation heat treatment at 800°C for 60 min was applied, followed by a final annealing at 1100°C for 60 min. The calculated dpa values (not shown here) at the SiO_2/Si interface are below 10^{-3} dpa. AES and TEM were used to characterize the microstructure of the devices.

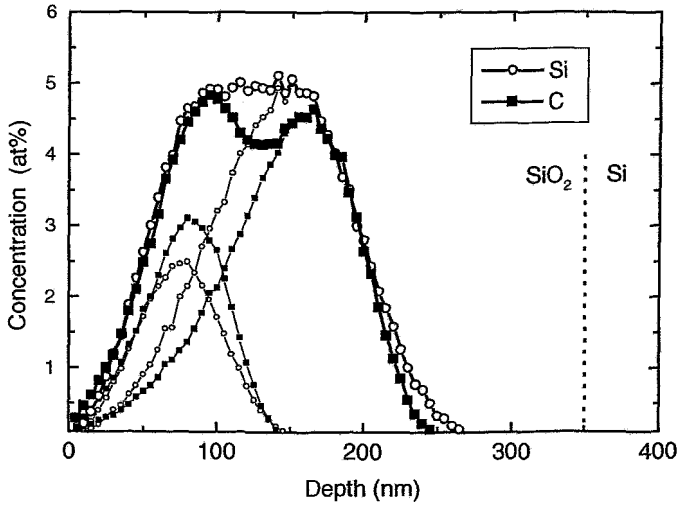


Fig. 4.4:
Profile of a Si/C co-implanted SiO_2 layer. Two implantations at different energies were carried out for both, Si and C. The small symbols are related to the single implants.

4.2. Influence of thermal annealing

4.2.1. The annealing of defects

Thermal treatment of ion implanted layers is essential for the annealing of implantation induced defects. During the annealing process the implanted atoms diffuse within the layer and may form nanoclusters. The changes of the microstructure were observed by means of RBS, STEM-EDX and TEM and are discussed in the following sections.

The diffusivity of Si implanted into SiO_2 layers is relatively low. Typical values are of the order of 8.8×10^{-7} $cm^2 s^{-1}$ at 1000°C [Tsou01]. This means that noticeable changes of the implanted profile are observed only after long time treatment at high temperatures (e.g. for a few days [Tsou01]).

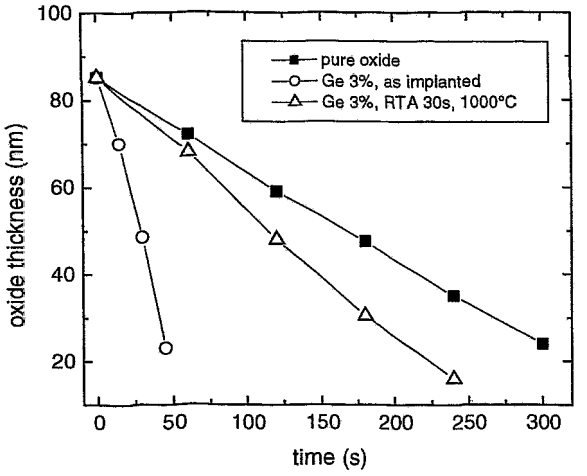


Fig. 4.5:
Oxide thickness of pure and modified SiO_2 layers after P-etch. Implanted layers show an increase of the etching rate.

The influence of thermal annealing steps on the recovery of implantation induced defects can be very well demonstrated by the investigation of changing etching rates. The oxide layers (85 nm) were etched using a standard P-etch. The etchant for this method consists of 300 ml H_2O, 19 ml HF and 11 ml H_3PO_4. Fig. 4.5 shows the oxide thickness as a function of etching time. The measurement of the remaining SiO_2 layer thickness was performed using ellipsometry. The etch rate of pure SiO_2 is 12 nm/min which is in good agreement with the values known from the literature. For implanted layers without annealing the rate is increased by a factor of 6.5 to a value of 78 nm/min. This can be explained by implantation induced damage which leads to broken bonds. The distorted network of the SiO_2 leads to an enhancement of the etching reaction. After annealing most of the implantation induced defects recover and the etching rate decreases to 18 nm/min.

4.2.2 Redistribution of the implanted germanium

The profile of the implanted ions was investigated by RBS. Fig. 4.6 shows the RBS-profiles as a function of the annealing time. Starting from the as-implanted profile with a Gaussian-like peak the redistribution of the Ge shows several features. First, the initial peak decreases and a broadening of the profile can be observed. This effect is accompanied by a strong diffusion of the Ge towards the interface SiO_2 / Si. The formation of a near-interface peak occurs for longer annealing times. Especially for the 50 keV Ge implant the initial Ge distribution becomes asymmetric and the peak at the interface dominates the distribution for long annealing times, reaching a concentration of up 1.4 at% Ge. For a better understanding of this effect Fig. 4.7 gives an overview about the distribution of the Ge in the two peaks in stacked column plots. The columns are divided into two parts where the black part refers to the Ge peak at the interface and the open part the bulk peak. The plotted values correspond to the implanted Ge fluence and were determined by evaluation of the RBS results (Fig. 4.6). Two methods, fitting with Gaussian peaks and numerical integration were used. However, the Gaussian fit leads to very broad peaks for

the situation of low Ge concentrations in the R_p region, especially for the case of 150s RTA. Since such fits do not represent the real RBS results and may lead to misinterpretations, the numerical integration was preferred for the calculation of the Ge content. The integration limit between the two peaks was set to 60 nm. The row of the plot arrangement corresponds to different Ge concentrations (maximum peak concentration in the as-implanted case) while the column is related to different implantation energies. It can be clearly seen that the amount of Ge remaining in the R_p region of the original implantation profile is strongly reduced with increasing annealing time, especially for the case of 1% Ge and for the 30 keV implant. This effect is of great importance for the charge trapping properties (see section 5.4.1).

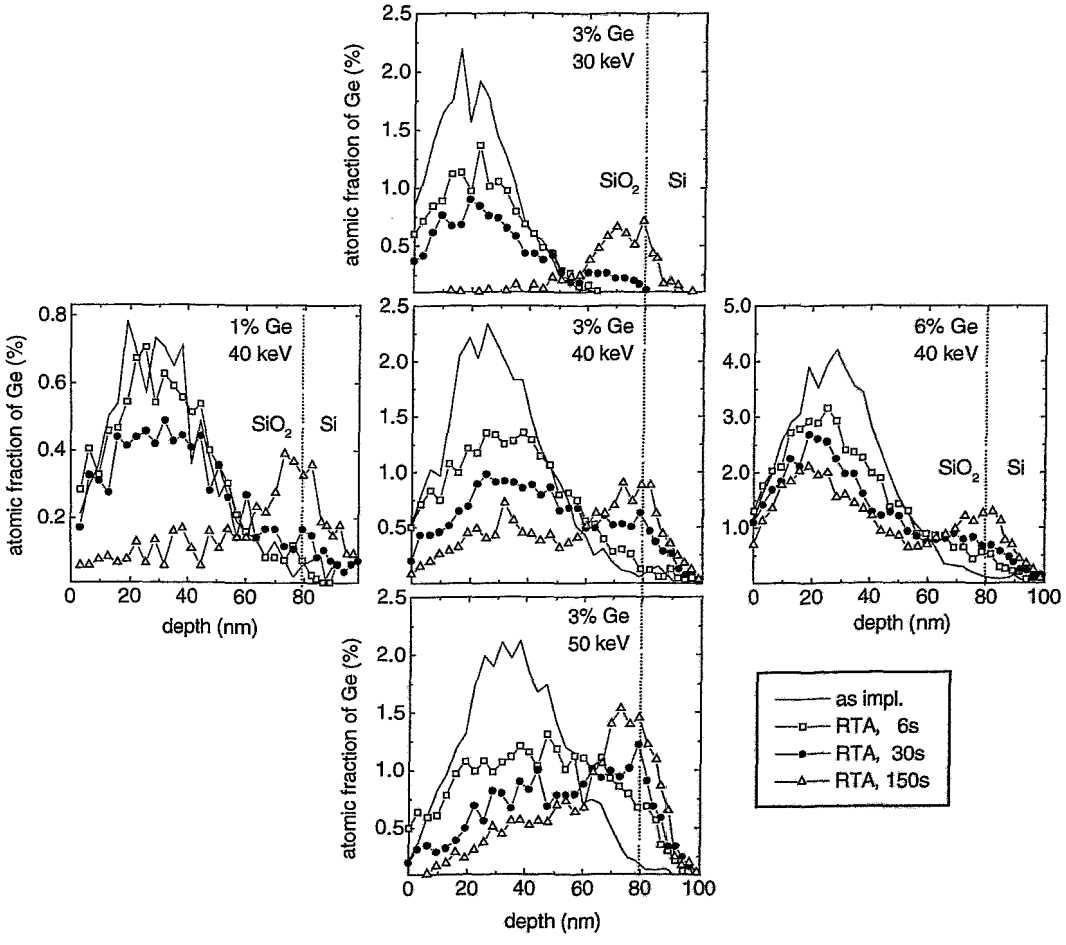


Fig. 4.6:
RBS results show the redistribution of Ge in the SiO_2 layers as a function of the annealing time. With increasing annealing time the Ge diffuses towards the SiO_2/Si interface (indicated by the thin vertical line). The arrangement of the plots is sorted regarding the implantation energy (column) and the Ge-concentration (row). The plots in the middle row have different scales of the Ge-concentration for the sake of better comparison.

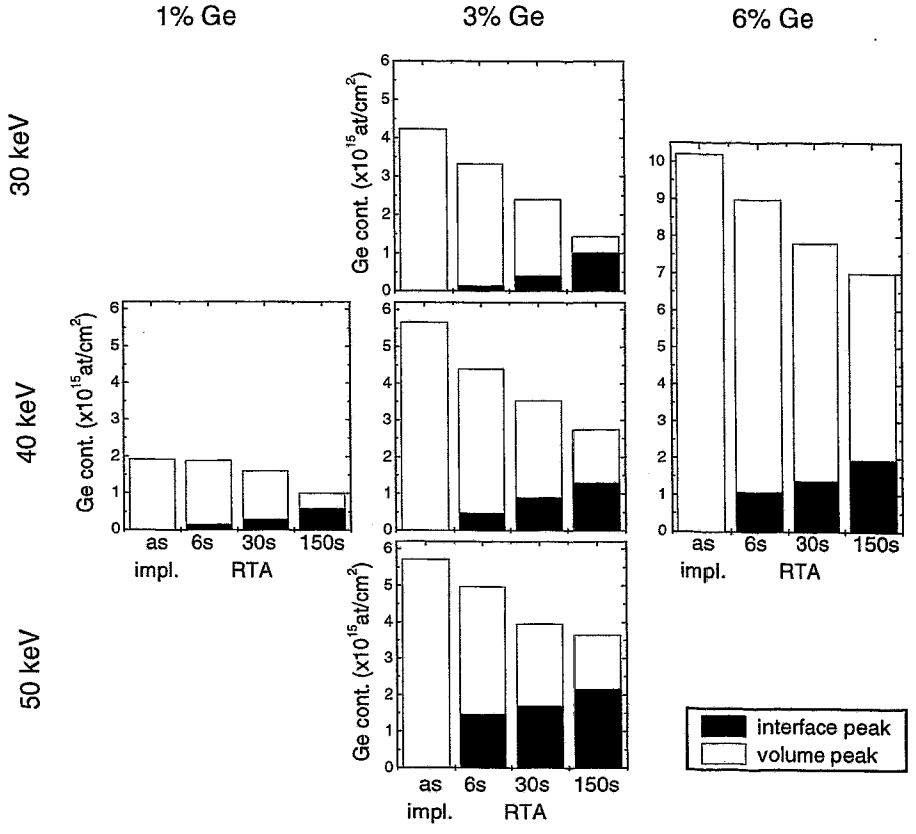


Fig. 4.7:
Ge content (given as Ge fluence) as a function of the annealing time. A loss of Ge occurs due to outdiffusion through the surface. With increasing annealing time the fraction of Ge located at the interface increases. Note, that the fluences for the different implantation energies are different, because the implantation parameters were chosen to yield the same maximum concentration in the peak (e.g. 3%).

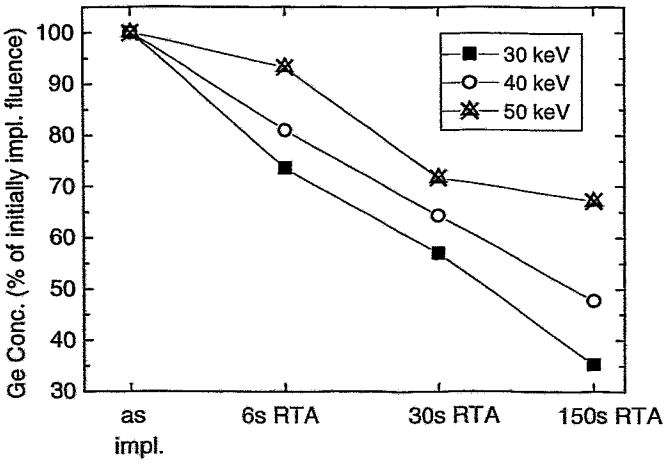


Fig. 4.8:
Ge concentration as a function of the annealing time. A loss of Ge occurs due to outdiffion through the surface.

The second observed effect is the decrease of the total amount of the Ge with increasing annealing time. The presence of hydrogen containing species (like H, H_2O, -OH) in the atmosphere between the processes ion implantation and annealing and also the moisture in the residual gas during annealing causes the indiffusion of hydrogen and oxygen bonded in different compounds into the damaged SiO_2 layer. This effect leads to the loss of Ge by the formation of GeO_xH_y compounds (especially GeH_4) and its outdiffusion. The Ge loss is enhanced for implants near the surface. This can be seen in Fig. 4.8, where the fraction of Ge remaining in the SiO_2 layer after RTA treatment is plotted. The loss of Ge increases with annealing time and is enhanced for lower Ge implantation energies. It should reach saturation because of the competing process of diffusion of Ge to the SiO_2/Si interface. This can be seen for the 50 keV implant, where the remaining Ge dose appears to saturate. SiO_2 layers with the 50 keV implant show a loss of about 32%, the 40 keV implant of 53% and the 30keV implant of even 65 % of the initially implanted Ge fluence. The only chance to reduce this effect is to avoid the moisture contamination of the layers. This could be achieved if the whole process including oxidation, implantation and annealing is carried out in a completely closed chamber, e.g. in a so called cluster tool.

4.2.3 Redistribution of the implanted tin

The redistribution of the implanted Sn^+ ions was investigated by RBS and TEM. 60 keV Sn^+ ions were implanted into the SiO_2 layers with a thickness of 100 nm. According to the calculations performed with the TRIM-program [SRIM00] the projected range was 38 nm. Layers implanted with a fluence of $1.6x10^{15}$ ions/cm^2 (1 % peak concentration) do not show clusters, but in the depth region of 30 .. 50 nm covered by the peak in the RBS spectrum, one can observe modifications of the SiO_2 structure in the TEM image (Fig. 4.9). The changes in the structure show up as a stronger contrast and may be attributed to dispersed Sn. In 100 nm thick SiO_2 layers implanted with an atomic fraction of 3% Sn the formation of clusters takes place. Two different bands of clusters can be observed by TEM. In a distance of about 6 .. 8 nm from the surface a band of clusters with sizes up to 4..5 nm occurs while in the region of the RBS peak the clusters reach sizes up to 10..12 nm.

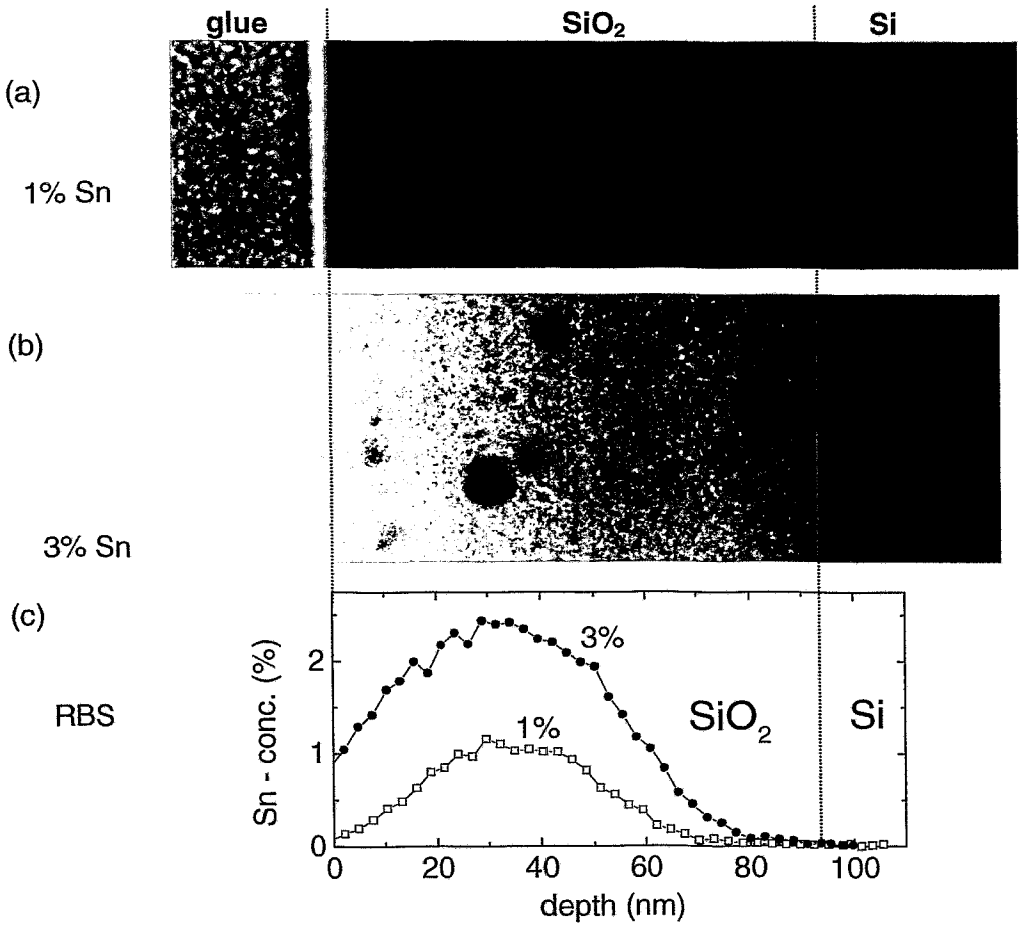


Fig. 4.9:
TEM (a,b) and RBS (c) results of 100 nm SiO_2 layers implanted with 60 keV Sn^+ ions. The samples were annealed at 1000°C for 6 s.

Samples with 200 nm SiO_2 were implanted with 130 keV Sn^+ ions, corresponding to an R_p of 68 nm [SRIM00]. The microstructure of these implanted layers is displayed in Fig. 4.10. The RBS spectra exhibit peaks with an asymmetric shape. A longer tail in the direction towards the interface can be observed. For a Sn concentration of 1% a narrow cluster band becomes visible which is located at a distance of 50 nm from the surface at the maximum of the RBS peak. On the right hand side of this cluster band additional clusters are present. This is a first indication for the formation of clusters in the tail of the Sn profile which is even more pronounced for the 3 % Sn implanted SiO_2 layers (Fig. 4.10b). Here clusters up to a size of 14 nm are visible. The clusters in the near-surface cluster band reach only sizes up to 8 .. 10 nm. In the dark-field image only clusters of the central cluster band give bright spots indicating a crystalline structure of the clusters.

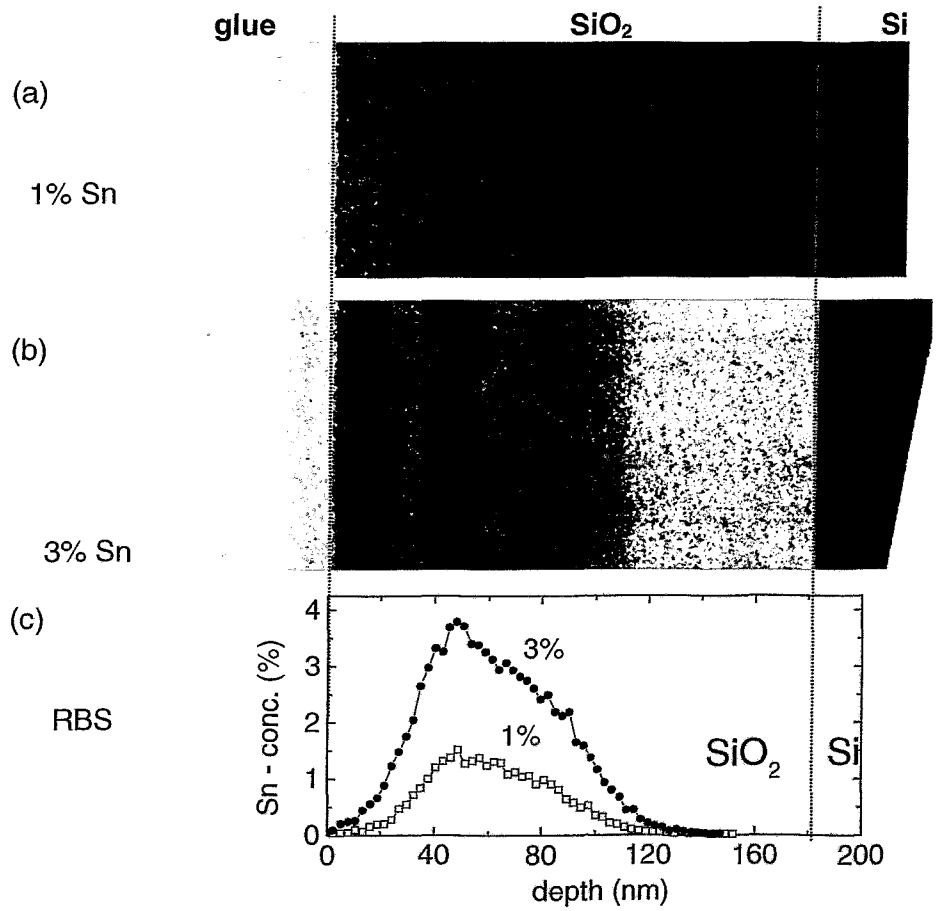


Fig. 4.10:
TEM (a,b) and RBS (c) results of 200 nm SiO_2 layers implanted with 130 keV Sn^+ ions. The samples were annealed at 1000°C for 6 s.

4.2.4 Co-implantation of Si and C

During the investigation of Si/C co-implanted SiO_2 layers by TEM only very small nanoclusters could be observed. In this case the RBS method - like also in the case of Si implanted SiO_2 layers - is not very helpful to determine a depth profile of both, Si and C in the SiO_2 matrix. Therefore other methods had to be applied to understand the microstructure of these modified layers. Fig. 4.11 shows the depth profile of the Si, O and C concentration measured by AES in a layer with 10 % excess Si and C. A constant Si concentration of 32 % near the value of 33.3 % for stoichiometric SiO_2 was measured. However, the expected increase to 36 % at a depth of 60..180 nm was not observed. So far the reason for this effect is not understood. In contrast to this, the O concentration drops down from 68 % to 58 % at a depth of 115 nm. The C profile behaves inverse to the O profile and shows a maximum of 10 % at a depth of 115 nm. The loss of O measured from a concentration level of 68 % is identical with the excess of C. At a depth of 170 nm a 30..40 nm broad band of amorphous nanostructures with sizes between 2 and 3.5 nm can be seen in the TEM (not shown).

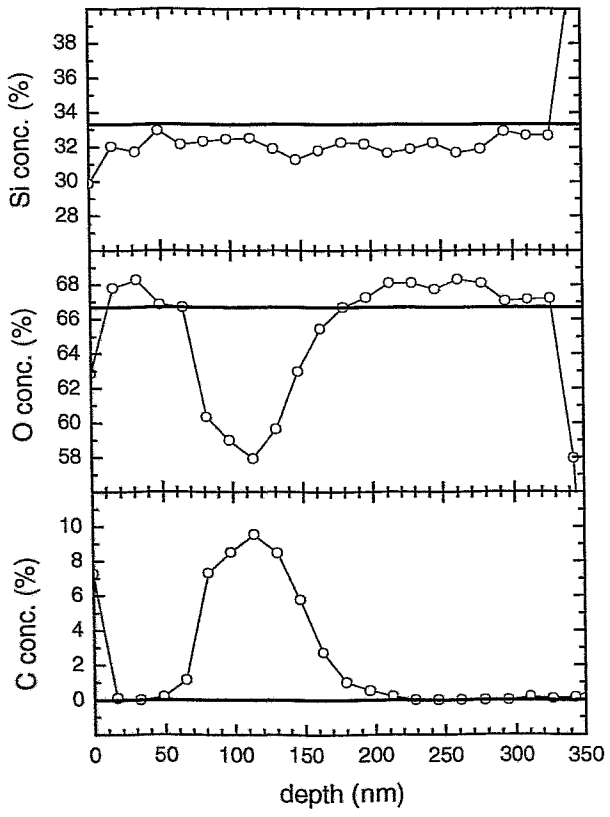


Fig. 4.11:
Concentration of Si, O and C atoms determined by AES as a function of depth. The SiO_2 layer contains 10 % excess Si and 10 % C. The thick solid lines represent the concentration value of stoichiometric SiO_2.

Fig. 4.12a displays the Si(KLL) Auger peaks for an oxide layer co-implanted with Si and C to peak concentrations of 10%. For comparison, the Si(KLL) Auger peaks of unimplanted SiO_2 and of SiC synthesized by C implantation into Si [Kögl97] are given in Fig. 4.12b. Close to the surface a Si(KLL) Auger peak (solid circles) is observed, which is very similar to that of unimplanted SiO_2, but shifted by 0.9 eV to the low-energy side. In the depth region of high C concentration between 80 and 150 nm the shape of the Si(KLL) Auger peak has changed considerably (up triangles) and shows now a peak at 1606.1 eV like the SiO_2 reference, but no peak at 1614.6 eV. Instead of this, a pronounced shoulder appears on the high energy side of the peak at 1606.1 eV. For the depth region > 150 nm, the Si(KLL) Auger peak alters gradually (down triangles) to that of the SiO_2 reference. Finally the Si(KLL) Auger peak changes to that from bulk Si with a strong peak at 1616.1 eV (stars).

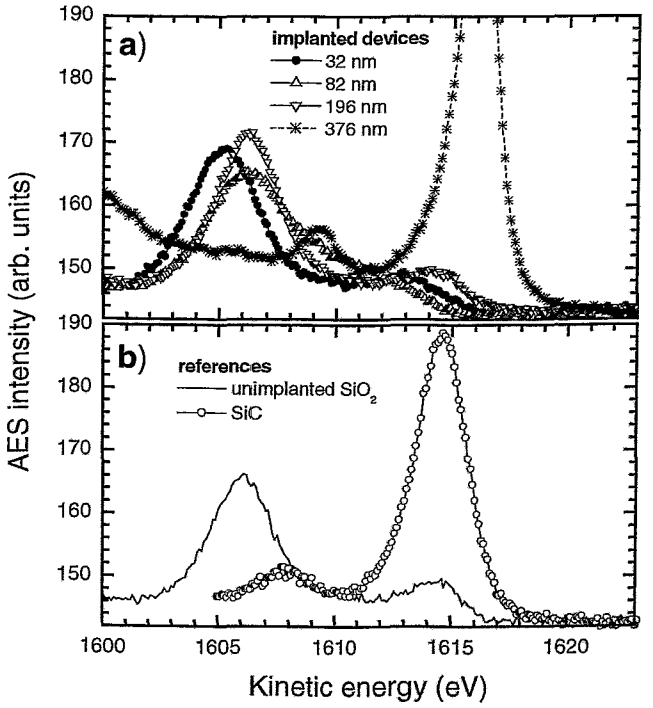


Fig. 4.12:
Si(KLL) Auger peak at different depths of a Si- and C-coimplanted SiO_2 layer containing 10 % excess Si and 10 % C (a). For comparison, the Si(KLL) Auger peak of unimplanted SiO_2 and SiC is also given (b).

In previous investigations the formation of Si nanoclusters was observed after Si implantation and annealing at 1100°C [Rebo99]. However, the following C implantation which was performed in this work will destroy these nanoclusters. Furthermore, the presence of C seems to hamper the formation of pure Si clusters in the final annealing step, as no PL in the red and infrared spectral region was detected (see section 6.1.2). The depth region with high C concentration between 80 and 150 nm does not correspond exactly to the band of nanoclusters observed in the TEM, but overlaps with the nanocluster band in a depth of 150 nm. There are two possible interpretations of the high energy shoulder of the 1606.1 eV peak. It could be due to suboxide states, namely SiO, which should be located between 1605 and 1616 eV depending on its formal oxidation number. But it could be also due to the SiC peak at 1607.8 eV, and the absence or shift of the large SiC peak at

1614.5 eV could be explained by the fact that not pure SiC clusters but isolated Si-C bonds are present.

These results imply the presence of $Si_yC_{1-y}O_x$ complexes with $x<2$ in the C rich region. As C has a smaller atomic mass than O, these complexes may not be visible in the TEM for a low Si content. It also could be possible that for a high amount of C a part of the C atoms is bound in small C clusters. In the region with the nanostructures the amount of C decreases, the nanostructures have a higher Si content and become visible in the TEM. Due to the small amount of C, the C-cluster formation is not likely in this region, and the C atoms could be bound to Si. So the visible nanostructures are composed predominantly of Si, but still contain enough C, which introduces imperfections to the Si clusters.

4.2.5 Nanocluster bands in ultrathin SiO_2 layers

The formation of nanoclusters in ultrathin SiO_2 layers (20..30 nm) used for memory devices was investigated by TEM. In the case of Ge implanted oxide layers clusters could be observed after RTA treatment. For SiO_2 layers of 30 nm thickness, which were implanted with 20 keV Ge^+, $5x10^{-15}$ cm^{-2}, the formation of two separated nanocluster layers was observed (Fig. 4.13). One of the bands is located in the region of the maximum Ge peak concentration and the other one is situated in a distance of about 3 nm from the Si/SiO_2 interface. The mean cluster size and density is about 3 nm and $5x10^{11}$ cm^{-2} (± 50%), respectively. All clusters were found to be in the amorphous state. The formation can be described by a model based on the dynamics of irradiation effects [Bora99a, Bora99b, Hein99]. From TRIM [SRIM00] calculations the dpa-value at the interface Si/SiO_2 was determined to be 1.5 dpa for the implantation of $5x10^{15}cm^{-2}$ Ge^+ ions. This value of >1 dpa implies that due to the collisional mixing which is mainly caused by recoil atoms, every atom of the SiO_2 network is displaced more than one time, leading to the dissociation of the SiO_2 network into its elemental components silicon and oxygen. In the bulk layer the components will recombine, but the region close to the interface behaves different, since the Si/SiO_2 interface acts as a sink for oxygen. Oxygen diffuses to this sink, leaving a oxygen depleted region behind, which now contains an overstoichiometric fraction of silicon. This excess silicon may form small precipitates which act as nucleation centers for the diffusing Ge. Rate-equation studies reveal a maximum value for the excess silicon concentration at a distance of 3..4 nm from the Si/SiO_2 interface [Bora99a]. During the annealing process, diffusing Ge is trapped at these centers and forms clusters. As a result a sharp δ-like cluster band is formed. Samples of the same thickness implanted with 12 keV Ge^+ ions showed only a bulk cluster band after the same annealing procedure. The reason for the missing interface cluster band is the low dpa value of only 0.06 at the interface, which suppresses the formation of excess Si acting as nucleation centers for Ge clusters. The experimental results were reproduced theoretically using a kinetic 3D-lattice Monte Carlo simulation [Strob99]. In this simulation, which starts from a Gaussian-profile of the implanted Ge and takes into account the excess silicon in the near-interface region, the formation of the near-interface cluster band and the band in the R_p region of the

implanted profile is demonstrated. The region between the two cluster bands does not contain nanoclusters, which is in good agreement with the experimental results.

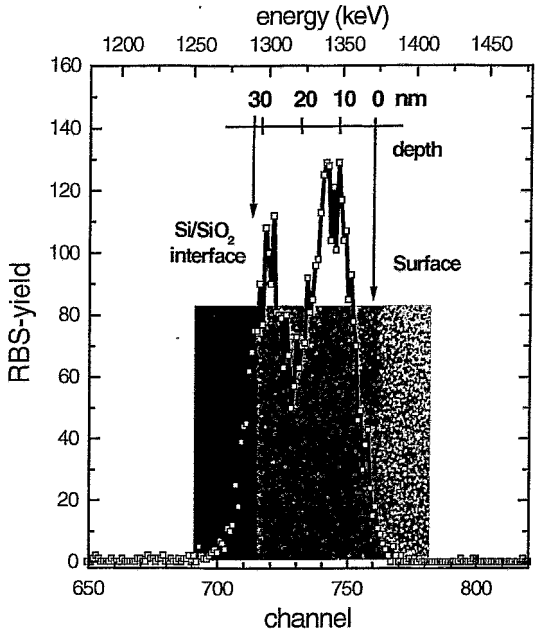


Fig. 4.13:
A 30 nm SiO_2 layer was implanted with 20 keV, $5x10^{15}$ cm^{-2} Ge^+ ions. The picture shows TEM and RBS results after RTA annealing (950°C, 30 s, N_2 atmosphere). Two cluster bands were found, one in the bulk region and the other one near the interface. All clusters are in the amorphous state.

The specific structure of the clusters is not clear, since one cannot clearly distinguish between pure Ge and GeO_x clusters. In order to do this, one has to apply XPS analysis [Oswa00]. However, by using this method in combination with depth profiling, which is typically done by Ar^+ sputtering, the XPS results themselves will be influenced by the damage produced through the sputtering process. The ion bombardment causes the breaking of bonds, therefore this method may lead to misinterpretations.

In the case of Ge implanted layers the TEM mass contrast is sufficient to observe amorphous nanoclusters in the SiO_2 matrix. For Si nanoclusters in a SiO_2 matrix, however, the phase contrast is too weak. Thus the only possibility to detect clusters is to observe the lattice fringes of randomly distributed crystalline nanoclusters. Amorphous Si clusters are hence not visible. Another limitation for the detection is the size of the clusters which should be at least 2 nm. It is known from the literature that the formation of crystalline Si clusters typically requires an excess Si content of more than 10 % [Lomb96, Norm98, Kape00]. This means that in our Si implanted layers clusters are very difficult to detect due to the low Si content and the correspondingly small cluster size. Devices with the parameters given in section 3.1.4, which were used for the electrical investigations, did not show any nanoclusters in the TEM images. However, for slightly modified parameters (30 nm SiO_2 layer implanted with 12 keV Si^+ ions, $1x10^{16}$ cm^{-2}, RTA 1050°C, 30 s) Si nanoclusters could be observed. The inset in Fig. 4.14 shows a nanocrystal with a size between 2-3 nm, recorded near the projected range ($R_p \pm 5$ nm) of the implant. No Si nanoclusters were detected very close to the Si/SiO_2 interface contrary to the Ge case. The ion implantation with the used parameters usually results in a substrate amorphization within a thin layer (< 5nm). But after annealing a complete recovery of the lattice structure

and a very smooth Si/SiO_2 interface with a "roughness" of only 1-2 Si lattice plane distances was obtained, which was verified by large area X-ray reflection using synchrotron radiation (rms-roughness of the Si/SiO_2 interface: 0.4 nm). It has to be mentioned that the electron irradiation itself can also influence the cluster formation. Growing nanoclusters during the TEM investigation are described in [Klim00]. Even in samples implanted with Ge, which did not show clusters at the beginning of TEM investigations after a irradiation for several minutes clusters were observed.

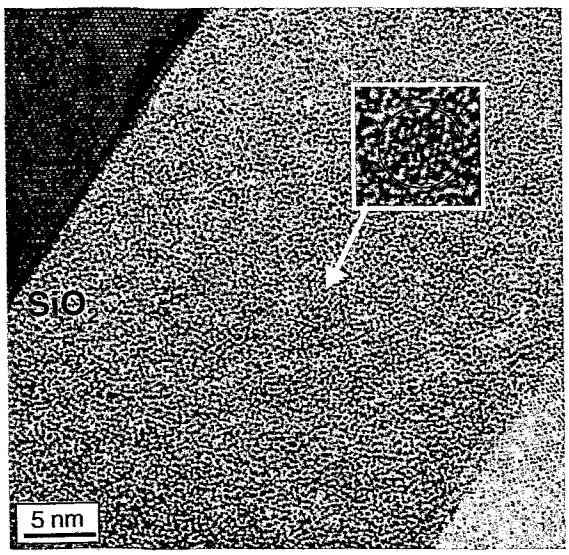


Fig. 4.14:
High resolution TEM micrograph of a Si implanted (12 keV, $1x10^{16}cm^{-2}$) SiO_2 film after rapid thermal annealing at 1050°C, 30 s in dry nitrogen. The inset shows in a further magnification the [111] lattice planes (distance: 0.33 nm) of a single Si nanocrystal of about 3 nm size. The measured lattice plane distance corresponds very well to the Si bulk value (0.325 nm).

4.2.6 Additional top layers and their role during annealing

To minimize the influence of the annealing atmosphere, additional capping layers can be deposited in order to protect the structures. In this work a 50 nm silicon nitride (Si_3N_4) layer was deposited by LPCVD after implantation. Si_3N_4 is known as an excellent material for the suppression of oxidation of the covered layers. It is used for instance in the standard LOCOS technology during the field oxidation process [Hill95]. Here the capping layer acts as a diffusion barrier for oxygen and oxygen containing species which are present in the annealing atmosphere. Fig. 4.15 shows the RBS results of Ge implanted layers with (a) and without (b) a capping layer. A significant influence on the distribution of the Ge in the bulk and interface peak can be observed. The protection from oxygen leads to a decrease of the amount of Ge which is fixed in the R_p region. So more Ge remains unoxidized and diffuses towards the SiO_2/Si interface.

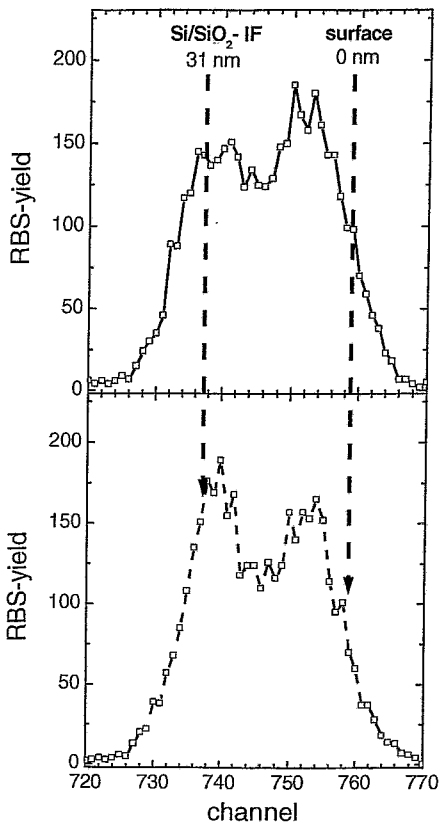


Fig. 4.15:
RBS results of Ge implanted SiO_2 layers after annealing. The oxidation of Ge in the R_p region can be reduced due to a capping layer (b) leading to an enhancement of the amount of Ge at the interface.

(a) without capping layer (ratio interface:bulk = 45:55)

(b) with 50 nm Si_3N_4 capping layer (ratio interface:bulk = 52:48)

From these results one can conclude that the presence of a capping layer and its properties give an additional parameter for the controlled "design" of nanocluster rich SiO_2 layers. It has to be mentioned that not only moisture and oxygen from the residual gas of the temper atmosphere may cause the oxidation of the Ge. After implantation the SiO_2 layer is highly damaged and moisture of the storage environment may already cause the presence of oxygen in the layer [Schm02]. Several treatments are possible to minimize this effect. First, the capping layer could be deposited before the implantation. This would cause a direct protection of the SiO_2 layer but the implantation profile would be broader because of the higher implantation energy. Second, the implantation and the following annealing could be performed in-situ in a cluster tool preventing additional moisture diffusing into the damaged SiO_2 layer.

5. Electrical Properties

5.1. Charge transport and injection mechanism

5.1.1 IV-characteristics of nanocluster-rich SiO_2 layers

Investigations of the IV characteristics are required for the understanding of the charge injection, transport and trapping mechanisms. Nanoclusters or molecule-like defects in the SiO_2 layer induced by ion beam synthesis will change the tunneling barrier and therewith the tunneling mechanism. For the EL investigations ITO was used as material for the formation of the gate contact. During measurements of the electrical properties of these device several difficulties were observed. First, the stability of the devices was worse compared to typically used devices with Al or poly-Si contacts. Larger variations in the charge-to- breakdown and also in the flatband voltage shift were observed by scanning several devices over a whole wafer. Second, ITO is known to deteriorate at higher temperatures (>200°C) and is hence not a suitable material for temperature dependent measurements. Therefore in this work additional sets of samples with Al electrodes were fabricated in order to minimize any disturbing influence of the electrode on the device structure and to focus on the intrinsic device properties and the specific modifications due to ion implantation and annealing. Fig. 5.1 shows the J-E plot of 80 nm SiO_2 layers implanted with Ge and annealed with RTA procedures. For comparison the as-implanted layers were also investigated. The characteristics of the J(E) curves can be divided into three main parts:

(i) the low field region (LFR), which is dominated by a very weak ohmic conduction and the displacement current,
(ii) the mid-field region (MFR), typically ranging from 5..7 $MVcm^{-1}$ and
(iii) the high field region (HFR) above 7 $MVcm^{-1}$ which is dominated by FN or FN-like injection.

In the LFR the samples implanted with 40 or 50 keV Ge^+ ions show a relatively weak dependence on the annealing time. For the 30 keV implant a stronger influence of the RTA time is observed which should be related to the enhanced outdiffusion of Ge as shown in Fig. 4.8 in section 4.2.2. The as-implanted samples with Ge concentrations of 3 or 6 at% exhibit higher currents which are slightly reduced during annealing at high temperature. Since this effect is most pronounced for the low-energy implant and decreases for higher implantation energies, this implies that mainly the Ge in the surface region causes this higher leakage current. The devices implanted to a concentration of 1 at% Ge show a different behavior. Obviously in that case some of the defects are first not present in the as-implanted case but then formed during the annealing step. This is different to the defect formation during the implantation process, like for samples with higher Ge concentrations.

The MFR is characterized by a linear section of the lnJ(E) curve. The onset of this region varies for the different samples and ranges from 4.0 $MVcm^{-1}$ (3% Ge, 50 keV implant) up to 6.5 $MVcm^{-1}$ (40 keV, 1%). In general, a shift of the MFR-onset towards lower electrical fields is observed with increasing implantation energy and increasing fluence of the implanted ions. This is an indication for a trap-related injection/conduction mechanism. Since the injection of electrons occurs from the Si/SiO_2 interface, one can explain the earlier onset with an increasing number of traps formed by the Ge which is present at the interface. The same effect occurs for longer annealing times because of the increasing Ge concentration in the interface peak, as shown by the RBS results in section 4.2.2.

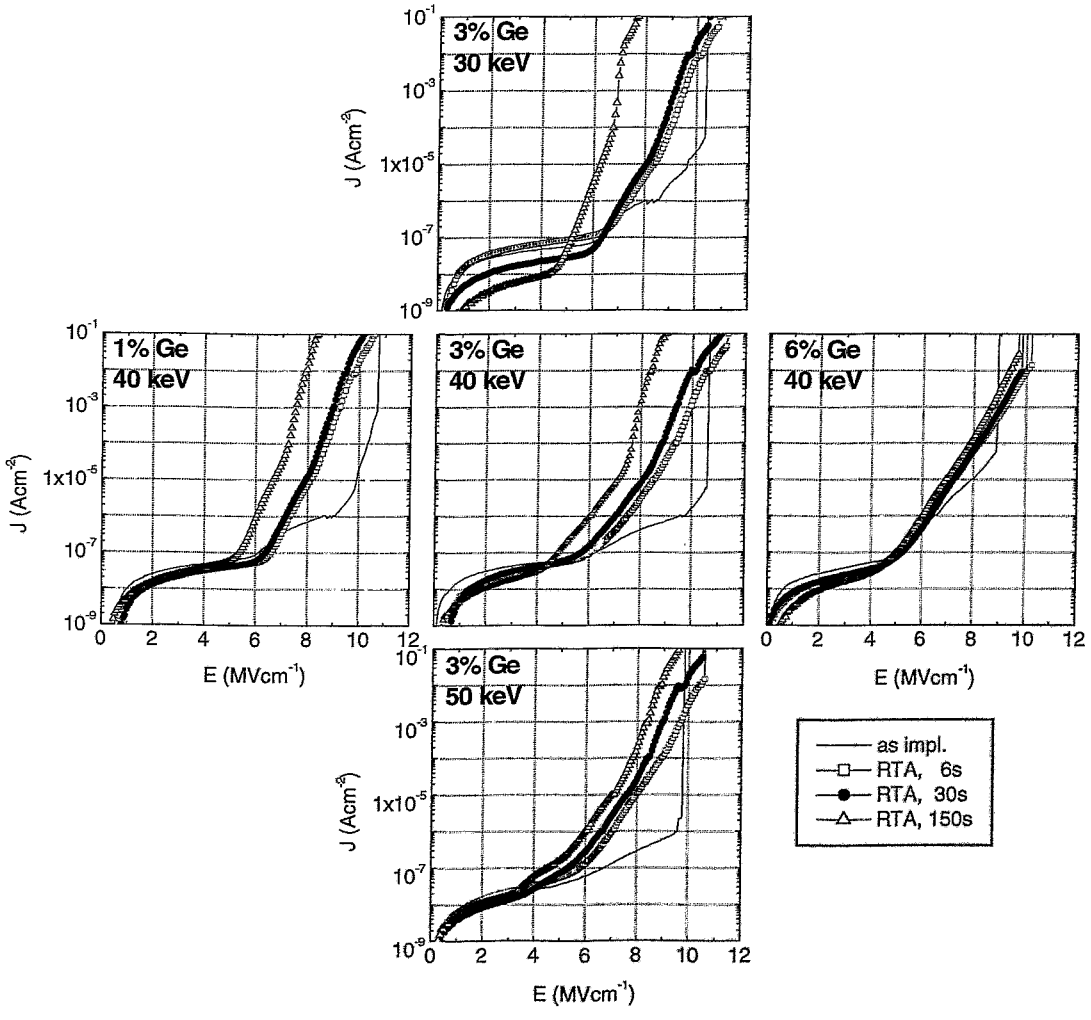


Fig. 5.1:
IV-characteristics of Ge implanted 80 nm layers. The samples implanted with ion energies of 30, 40 or 50 keV to atomic peak concentrations of 1, 3 and 6% were annealed (RTA) at 1000°C for 6, 30 and 150 s.

With the beginning of the HFR the linear lnJ(E) characteristics typically changes abruptly and exhibits a steeper increase. To explain this behavior one has to consider a change in the injection/conduction mechanism which occurs at high fields. This effect is more pronounced for low implantation energies, for low fluences and the longest annealing times. In contrast to that, the MOS capacitor implanted with 6% Ge even shows no remarkable difference in the slope between MFR and HFR.

The J(E) curves of the as-implanted layers show a different behavior compared to annealed samples. The curves follow the behavior of the LFR even in the MFR and the HFR. Only for the 30 keV, the 40 keV 1% and 3% devices one can observe a change of the slope at an electric field of about 9..10 $MVcm^{-1}$ before the device breakdown occurs. This slope is comparable to that of the J-E characteristics of annealed layers in the HFR. The maximum current densities reached before device breakdown are more than 3 orders of magnitude smaller compared to annealed samples. As an exception the layer with 6% Ge shows J-E curves for all, the as-implanted and the annealed samples, which do not show such remarkable differences.

The I-V characteristics of the unimplanted SiO_2 layer which was used as a reference show a very good agreement with a FN-fit (Fig. 5.2). The IV plots for various annealing procedures do not show large differences except for the 150 s RTA treatment.

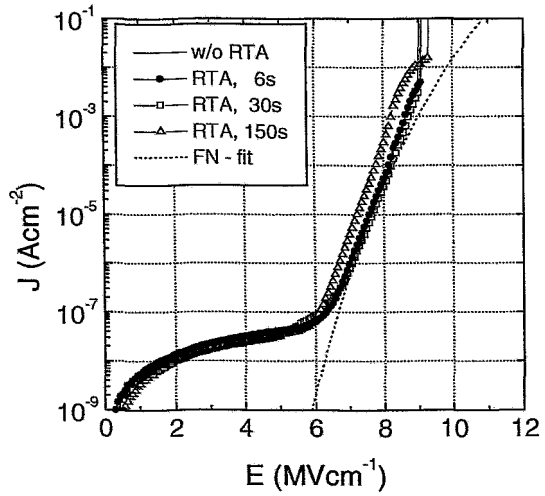


Fig. 5.2:
IV characteristics of an unimplanted reference SiO_2 layer. The dependence on the annealing is very weak for short RTA treatment. The dotted line represents a FN-fit (m^*=0.4, Φ_B=2.95eV)

IV characteristics of Si or Ge implanted SiO_2 layers with a thickness of 20 nm used for memory structures are plotted in Fig. 5.3. An enhanced conduction can be observed in the LFR and MFR. The onset of this enhanced conduction is shifted towards lower electric fields with increasing Ge or Si concentration. In Fig 5.3a samples with different implantation energies are compared. Especially for higher implantation fluences for the 12 keV implant with a projected range R_p in the middle of the oxide layer (13 nm) this onset occurs earlier compared to the 20 keV implant with an R_p of 18 nm, which is close to the Si/SiO_2 interface. The slopes of the IV curves are similar for the lowest fluences, but in the case of higher Ge concentrations the 12 keV implanted SiO_2 layer exhibits a weaker slope compared to the interface implanted layers. This could be related to a more bulk-limited

conduction mechanism while the 20 keV implanted samples show a more interface-limited IV behavior. The characteristics of the unimplanted SiO_2 layer can be fitted using the FN formula. The estimated barrier height of 2.95 eV is in good agreement with the values known from the literature.

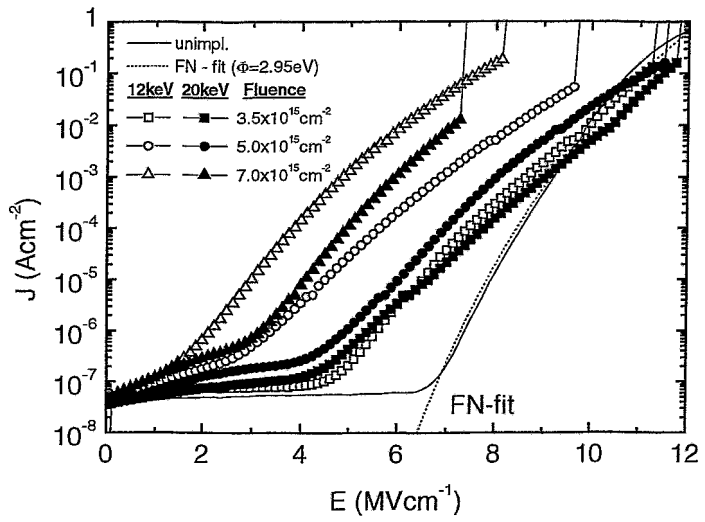


Fig. 5.3a:
IV characteristics of 12 and 20 keV Ge^+ implanted 20 nm SiO_2 layers.

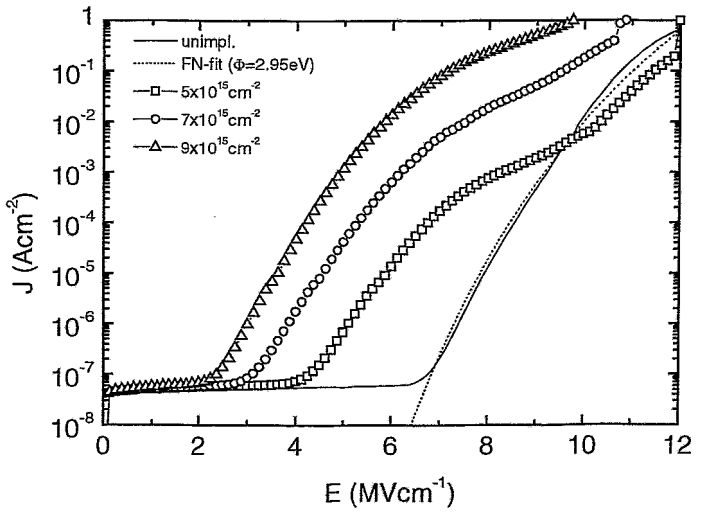


Fig. 5.3b:
IV characteristics of 20 nm SiO_2 layers implanted with 6keV Si^+ ions.

Fig. 5.3b shows the J(E) characteristics of a 20 nm gate oxide implanted with 6 keV Si^+ ions measured on MOS structures in accumulation, which means that positive bias is applied to the gate. Compared to the unimplanted reference one can clearly observe an additional contribution to the tunneling current for electric fields of 2.5...8 $MVcm^{-1}$. Both, the onset of enhanced conductivity as well as the current level itself increase with the implantation fluence. Such a behavior in the MFR is well known from stress-induced leakage current (SILC) after exposing thin SiO_2 films to high electric fields [Ricc98]. The shape of the characteristics shows a different behavior compared to Ge implanted samples. The slope of the curves is reduced at fields around 7..9 $MVcm^{-1}$ but then again increased. For the lowest implanted dose at high fields (>10 $MVcm^{-1}$) even a good agreement with

the unimplanted samples was observed. This implies that at such high fields the charge injection is dominated by FN tunneling and effects from trap like defects become negligible. For the samples containing higher doses this behavior cannot be observed since the achieved current densities are already too high before the onset of the FN regime.

According to formula (2.6) one can easily calculate the effective barrier Φ_B from the results of the IV measurements by plotting them in a so called FN – plot and fitting the slope. It should be mentioned that this effective barrier includes all effects causing the enhanced injection and conduction - and therewith also volume effects - in the HFR. This means that the calculated values show only the basic trend of the injection mechanism with increasing fluences, but one cannot directly plot them in the schematic band model. In Fig. 5.4 the results of these investigations are given for 20 nm (a) and 30 nm (b) thick SiO_2 layers. For better comparison, the barrier Φ_B of the unimplanted is given as a reference, plotted at the fluence 0. In both cases, (a) and (b), a decrease in the barrier height is observed with increasing Ge fluence. The effect is more pronounced for the thinner oxide layer. This could be related to the fact that the shorter tunneling distance leads to an enhancement of TAT. For the 30 nm layer the trend is also visible for the different implantation energies. For the case of the 20 keV implantation the decrease in the measured effective barrier height is increased. It was found for both oxide thicknesses that the Si implanted layers show slightly higher effective barriers in comparison to similar Ge fluences. However, if one considers the different shape of the implantation profile of the Si and Ge implants and takes also into consideration the slight differences in the peak concentration (see table 3.1. in chapter 3) the differences are not so remarkable.

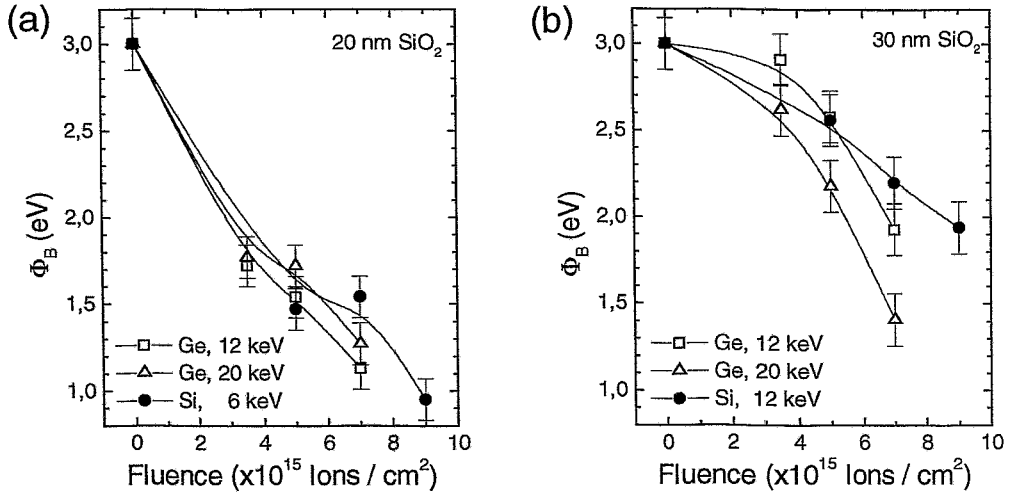


Fig. 5.4:
Effective barrier height Φ_B calculated from FN-plots of the IV characteristics (a: 20 nm SiO_2, b: 30 nm SiO_2) as a function of the implanted ion fluence.

Fig. 5.5a shows the time-zero-breakdown behavior of Si^+ implanted SiO_2 films for different implantation fluences measured with a fast voltage ramp of 3.3 V/s. Typically 50 devices were tested in order to consider the statistical nature of the dielectric breakdown. The breakdown field (E_{BD}) was defined for a current density of 3 Acm^{-2}. For better

comparison both, the distribution of the different breakdown events and the Weibull-plot, showing the cumulative device breakdown is given. Starting with the unimplanted reference oxide layer (E_{BD} =13.4 $MVcm^{-1}$) the breakdown field slightly decreases from 13.0, to 11.7 and 10.5 $MVcm^{-1}$ for fluences of 5, 7 and $9x10^{15}cm^{-2}$, respectively. This indicates that the increasing Si content leads to more imperfections in the SiO_2 network which can form leakage paths under high-field stress. Fig. 5.5b compares the breakdown behavior of Si and Ge implanted SiO_2 films. Compared to the Si^+ implanted layers (Fig. 5.5a), the Ge^+ implanted oxide films exhibit lower breakdown field strengths, although the implantation profile was comparable. The breakdown probability is also strongly enhanced for higher implantation doses in comparison to the Si - case. In principle, one of the main reasons for this different behaviour could be the higher diffusivity of the Ge atoms. These processes may lead to an enhancement of the leakage path formation which is a precursor of beginning device breakdown. The results for the two different energies of the Ge^+ implants do not show large differences. This basically implies that there is no strong influence of the position of the implanted profile, but in order to check this effect in more detail more investigations on samples implanted at various implantation energies are necessary.

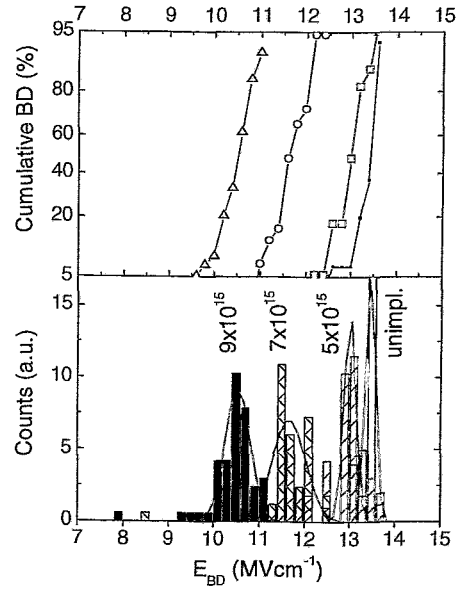


Fig. 5.5a:
"Time-zero"-breakdown measurements on 6 keV Si^+ implanted SiO_2 layers (fluences of 5, 7 and $9x10^{15}cm^{-2}$, respectively). The upper graph shows the cumulative breakdown in a Weibull-plot, the lower plot the distribution of the breakdown events.

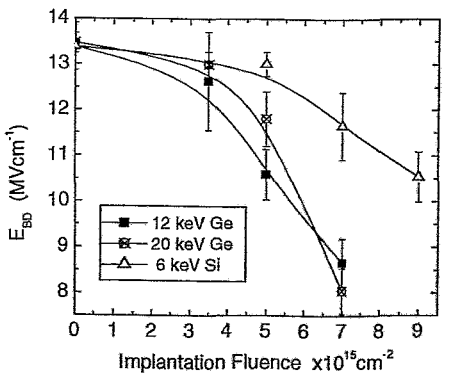


Fig. 5.5b:
Breakdown field E_{BD} of "time-zero"-breakdown investigations for Si and Ge implanted SiO_2-layers (20 nm)

5.1.2. Temperature dependence of the IV – characteristics

Modeling of charge injection, transport and storage is the main issue in order to understand the influence of the nanoclusters in SiO_2 layers on the electrical properties and to distinguish between the different possible conduction mechanisms. The results of the IV investigations (Fig. 5.1 and Fig. 5.3) imply that mainly in the MFR the IV characteristic is influenced by the implanted Ge or Si. Therefore temperature dependent IV measurements were carried out in order to get a better understanding of the influences of the implantation parameters. The following section gives an overview about possible mechanisms and models which help to describe the electrical properties.

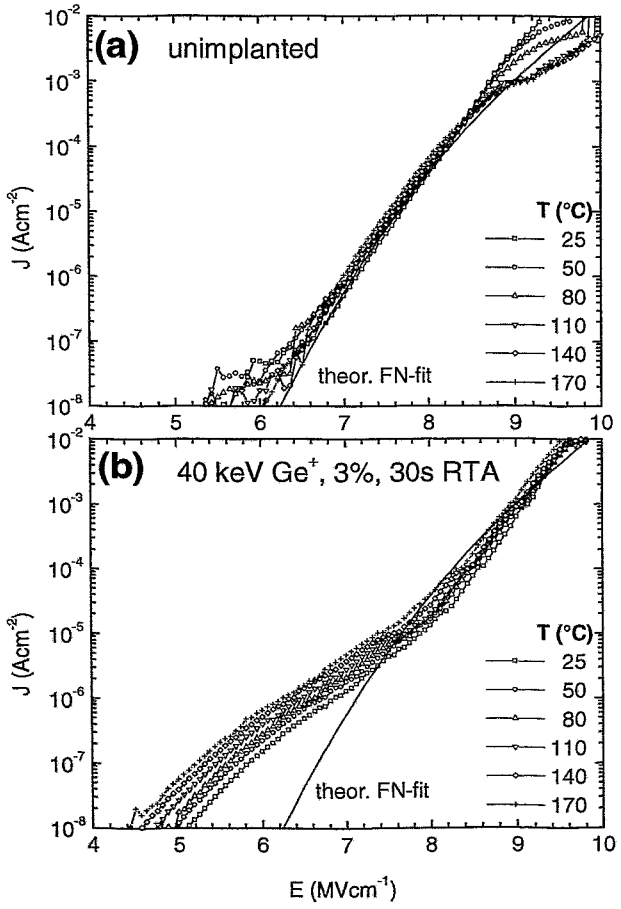


Fig. 5.6a:
IV characteristics of unimplanted SiO_2 layers for different temperatures (RT up to 170°C). The data can be fitted by the FN model according to formula (2.6) with a barrier height Φ_B of 2.95 eV.

Fig. 5.6b:
Ge implanted SiO_2 layers (80 nm) show a strong temperature dependence in the MFR. In the HFR, the data follow the FN curve and exhibit a weaker temperature dependence.

Fig. 5.6 shows the IV characteristics of both, the unimplanted oxide layer (a) and Ge implanted SiO_2 (80 nm SiO_2, implanted with Ge (40 keV, 3%) annealed at 30 s at 1000°C) shown in plot (b). Since the LFR does not show interesting features and is strongly influenced by noise current the plots are focused on the MFR and HFR. In these regions the measurement error is typically of the order of 10 %. In order to improve the quality of the results statistical data evaluation was carried out. Since local variations over the wafer

may occur during the wafer processing always several devices (more than 6) were measured and a median value was calculated.

For the case of the unimplanted oxide (Fig. 5.6a) only a weak temperature dependence is observed. Furthermore one can see that the plot follows a FN-fit. Contrary to that the Ge implanted oxide layer exhibits a stronger temperature dependence, especially in the MFR. In order to show this effect more detailed, in Fig. 5.7a the normalized current density is plotted as a function of the operation temperature. The plot contains data measured at different electric fields. In the LFR no significant temperature dependence could be observed, which is also related to the limit set by the IV measuring equipment because of the low currents. At electric fields of 4 $MVcm^{-1}$ the temperature dependence is only very weak and the relative current varies around a factor of 1. However, with in the MFR suddenly a strong increase occurs, shown here for E=5 $MVcm^{-1}$. For higher electric fields the dependence becomes weaker again which implies that obviously a change in the conduction mechanism occurs.

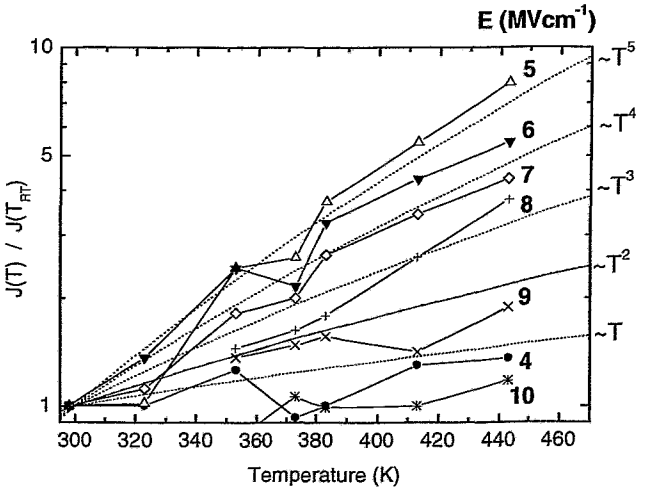


Fig. 5.7a:
Normalized current plotted as a function of temperature for a 80 nm SiO_2 layer implanted with Ge, 40 keV (3%), RTA treated at 1000°C for 30s. The graphs are related to different electric fields (given in bold numbers). In the MFR (starting from 5 $MVcm^{-1}$) the strongest temperature dependence is observed. With increasing electric field the dependence becomes weaker. T^{α} fits are given as a guide to the eye.

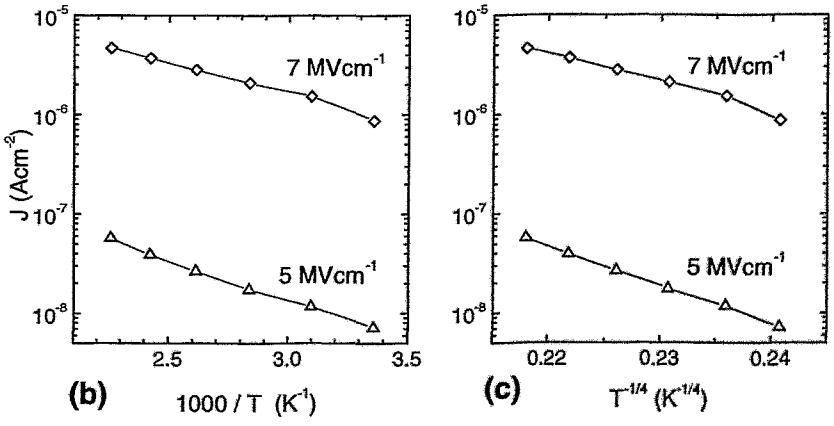


Fig. 5.7b / Fig. 5.7c:
Current density as a function of the operation temperature in the Arrhenius plot (b) and in a $T^{-1/4}$ plot (c) which is used to describe variable range hopping (VRH).

In order to study the conduction mechanism the logarithmic current density was plotted as a function of the inverse temperature (Fig. 5.7b) and $T^{-1/4}$ (Fig. 5.7c). The first graph corresponds to the so called Arrhenius plot which is used to describe processes related to thermal activation. The graph can be fitted linearly. The calculated activation energies are 0.16 eV and 0.13 eV for 5 $MVcm^{-1}$ and 7 $MVcm^{-1}$, respectively. The second plot is used to study the relation to the so called variable range hopping (VRH), which was described for group IV nanocluster rich oxide layers by Fuji et al. [Fuji96]. There, for modified SiO_2 layers containing C, Si or Ge clusters produced by co-sputtering, the conductivity σ shows the dependence $\sigma \sim T^{-1/4}$. It was shown in that paper that increased concentrations of Si, C or Ge cause a decreasing slope of the graph and therewith the activation energy. The reason for that is the larger size and the increased density of clusters at higher concentrations. In another work [Fuji98] a $T^{-1/2}$ dependence of the current is observed. As a general result we find that the conditions of the VRH conduction are also fulfilled by our results. This is in agreement to the statements of Fuji [Fuji96, Fuji98] who found VRH for group IV cluster rich oxide layers.

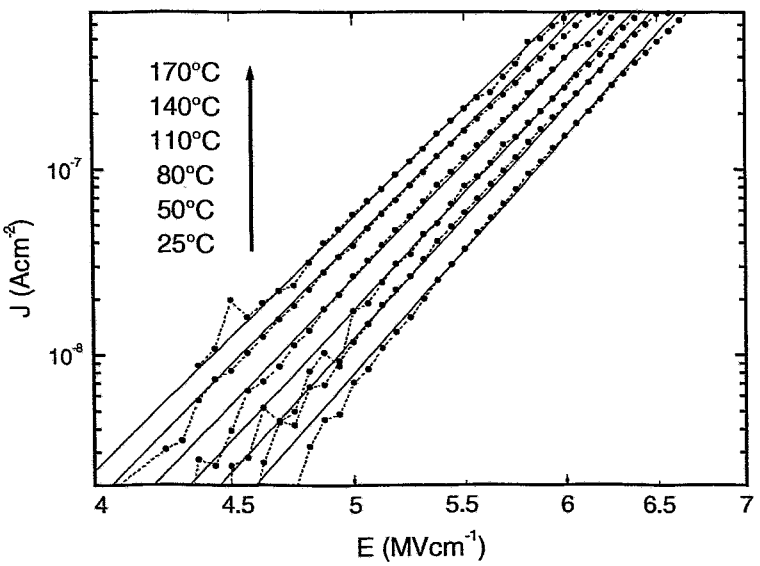


Fig. 5.8a:
Temperature dependent IV characteristics in the MFR for Ge implanted oxides (3% Ge, 80 nm SiO_2, 30 s RTA). Note, that the plot is given in a double logarithmic scale. The data were fitted by a power law dependence $J \sim E^{L+1}$

As known from the formula (2.10) given in section 2.2.3 it is not possible to describe the curves and especially the temperature dependence of the MFR with the models of Fowler-Nordheim tunneling or TAT. However, as shown in Fig. 5.8a. the IV characteristics in the MFR can be modeled very well with a power law dependence $J \sim E^{\alpha}$, with α ranging between 14.1 to 16.5. The electrical conduction in the MFR can be

assumed as bulk limited, which requires an enhanced transparency of the injection barrier in comparison with the non-implanted material. The Ge implantation creates trap states near the interfaces of the SiO_2/Si and SiO_2/gate contacts, which increases the electron injection by a mechanism like in the case of TAT. At the same time the electron transport through the oxide is hindered by implantation induced traps and the build up of space charges by the trapped electrons. As a result the properties of the injecting contact may converge to the properties of an Ohmic contact. If we consider the possibility of SCL conduction, the large exponents in the power law model of Fig. 5.8a could be interpreted using the TFL current injection [Lamp70].

It has to be mentioned that the mechanism of SCL has originally been defined for materials with delocalized electrons, e.g. semiconductors having a band structure. In SiO_2 there is no long range order and therefore one usually cannot think about mobility aspects. The bandgap of silicon dioxide is too large for any thermal activation (9.0eV [Sze81]) and the Boltzmann theory is not valid. This means, that in contrast to the materials the SCL model is used for we have to consider not the mobility but the trapped charge which limits the charge carrier transport. Using the SCL model (see section 2.2.3, eq. 2.14) we can only refer to a effective mobility describing the effect.

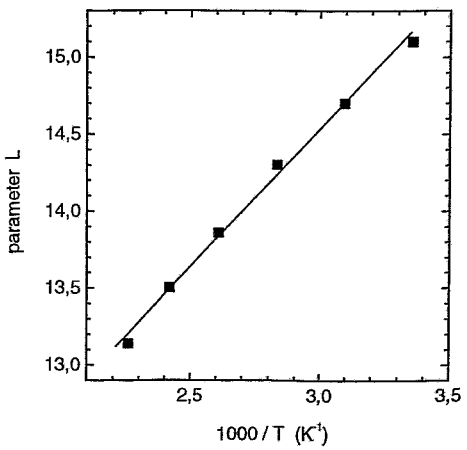


Fig. 5.8b:
Temperature dependence of the parameter L derived from the power law fit $J \sim E^{L+1}$ in Fig. 5.7. The solid line represents a linear fit of L as a function of 1/T.

The sharp increase in the current at a certain critical field is a characteristic feature for an insulator with traps, which occurs when the quasi-Fermi level (whose existence is assumed in the TFL model [Lamp70]) passes across a trap level or narrowly distributed trap levels. In the theory of TFL current, the IV characteristics can be described by the already mentioned power law dependence $J \sim E^{\alpha}$. Especially for an exponential distribution of the traps states in the band gap of SiO_2 [Lamp70], the relation $\alpha = L+1$ is valid. The parameter L is proportional to T_C/T, where T_C corresponds to the width of the trap distribution and T is the operation temperature. Derived from the data in Fig. 5.8a, the parameter L is plotted versus 1000/T in Fig. 5.8b. A linear relation is observed which supports the interpretation of the IV characteristics in the MFR using TFL current. The parameter T_C is derived to be 1811 K corresponding to a distribution width of about 156

meV. Similar values were observed from Ge implanted samples with thicker oxides layers (300 nm), namely 1760 K [Zhao01]. The SCL model is also used in the work of Zhang et al. [Zhan99], who describes temperature dependent measurements on Ge^+ implanted 120 nm thick SiO_2 layers. There, especially for higher implantation doses a strong dependence on the temperature was observed. For lower Ge fluences a weaker temperature dependence was found. This was explained by the domination of tunneling processes which are relatively independent of the temperature.

Another approach for the understanding of the temperature dependence of the IV characteristics is illustrated in Fig. 5.9. The plot shows a fit of the data from Fig. 5.6b using the PF-model. The intention of the fit was to cover the range with the strongest temperature dependence as shown in Fig. 5.7a, namely 5 .. 6 $MVcm^{-1}$. A good agreement was found for a PF-fit assuming Φ_{Trap} = 1.05 eV. By varying Φ_{Trap} it was also possible to fit the range up to 7.5 $MVcm^{-1}$, but in general it was not possible to describe the whole MFR by one single fit. This implies that basically PF-conduction may be a possible mechanism, but it is always accompanied by additional effects, e.g. limitations from the occurrence of trapped charge.

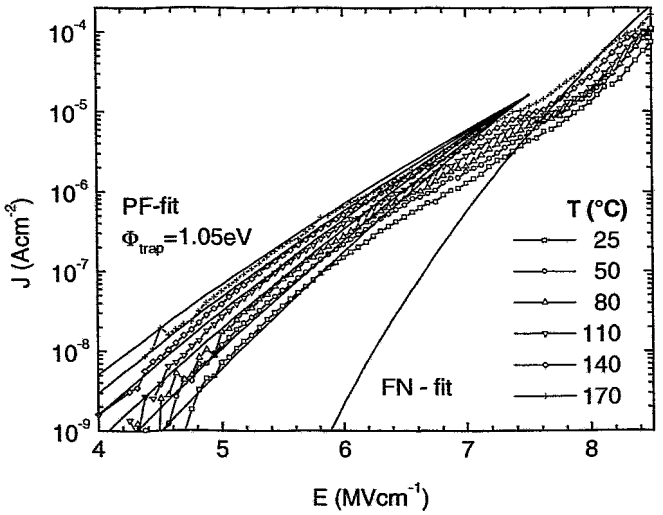


Fig. 5.9:
Ge implanted SiO_2 layers show a strong temperature dependence in the MFR. The data can be fitted by the PF model with Φ_{trap}=1.05eV. In the HFR the curves follow the FN - fit and the temperature dependence is weaker.

The IV characteristics in the HFR show features and a temperature dependent behavior different from those in the MFR (Fig.5.6b and Fig. 5.7a). The weaker temperature dependence in the HFR implies that a different mechanism, namely the FN-tunneling becomes more and more dominant. However, the current is greatly influenced by other effects which occur because of the high electrical field strength. These effects may include: (i) field emission of the trapped carriers under high electric fields, (ii) impact ionization and trap generation by hot carriers, and (iii) compensation of trapped charges lost by field emission and electron-hole recombination.

In conclusion one can say, that several models can be used to describe the charge injection and transport mechanism. The temperature dependence of the IV characteristics in the MFR can be modeled by hopping, VRH, PF conduction and the SCL model. From the relative small temperature range which was used for the investigations here we cannot

clearly distinguish between the different mechanisms. Future investigations with additional investigations in the low temperature range (down to liquid nitrogen or even liquid helium temperature range) could give further hints for the understanding of the charge transport mechanism. Additionally, models based on modified tunneling processes including the possible trapping of charges seem to be promising, but due to the large number of parameters they are of a very complex nature.

5.1.3. Models to describe the injection and conduction mechanism

The basic processes occurring during electron injection and electron transport in SiO_2 layers are schematically drawn in Fig. 5.10. In the case of unimplanted SiO_2 electrons will be injected by Fowler-Nordheim tunneling (process 1). If the oxide is implanted, defects are created in the oxide layer which appear as electron traps in the band gap of SiO_2. Higher implantation doses cause higher trap concentrations. For Ge doses exceeding local concentrations of 3% the formation of Ge nanoclusters was observed. Traps and Ge nanoclusters located close to the injecting interface can support the injection by trap assisted tunneling (process 2) or by direct tunneling from the conduction band of the Si substrate to the Ge nanoclusters. As a result the electric field where tunnel injection starts decreases with increasing trap concentrations and the I-V characteristics shift to lower applied electric fields with increasing Ge concentration (see chapter 4). In that case, structural defects, which are related to deep levels in the SiO_2, enable the TAT current. Referring to ion implanted SiO_2 films, such traps may be generated as a result of the ion irradiation and/or nanocluster formation. Kalnitsky et al. [Kaln90a] describe the charge transport by direct tunneling between (single, amphoteric) traps and both the Si substrate and the poly-Si gate. The assumed trap distribution follows the implantation profile. The model shows excellent agreement with the experimental data and describes the enhanced conductivity in the mid-field region. From the fit of the IV-characteristics the energy level of the trap was calculated to lie about 3 eV below the SiO_2 conduction band edge.

Some insight into the corresponding microstructure has been derived from electron paramagnetic resonance (EPR) measurements. EPR studies of Si implanted SiO_2 films reveal a significant concentration of so called P_b centers (Si dangling bonds, gyromagnetic factor: $g \cong 2.005$) related to excess Si (probably from the surface of nanoclusters) after annealing at $T > 900°C$ [Kaln90b, Lope01]. Its structure is proposed to be $O_3{\equiv}Si^{\bullet}\ldots{}^{+}Si{\bullet}{\equiv}O_3$ [Kaln90b], which is converted into the neutral oxygen vacancy (NOV) $O_3{\equiv}Si\text{-}Si{\equiv}O_3$ upon electron trapping. It has to be mentioned that the characteristic blue/violet luminescence of Si^+ or Ge^+ implanted SiO_2 is widely accepted to be caused by ODC, e.g. the NOV which confirms the existence of these centers in such layers. The TAT model was initially developed and applied for nitrided oxide layers [Chen88, Flei92] and can be also used for the description of the IV characteristics of high-k gate dielectric stacks [Hous00]. It seems to be a suitable tool to the understanding of the charge transport in implanted SiO_2 layers. However, the large number of different parameters for trapping,

detrapping and the influence of trap distributions lead to quite complex models, like for instance in [Kaln90a].

Another description of the IV characteristics of Si - implanted SiO_2 layers using a rather sophisticated model including TAT, FN tunneling and also direct tunneling is given in [Kame99]. The main idea of the work is the focus on one mechanism for a defined electric field range. TAT, first implemented for a triangular barrier, was later expanded to a generalized TAT model. Tunneling trough a trapezoidal barrier was included leading to an extension of the TAT model towards lower electric fields ($E<4MVcm^{-1}$) [Houn99]. Only a few authors discuss the influence of the temperature on the TAT mechanism, since it is - like all tunneling mechanisms - expected to be nearly independent of the temperature. The different filling of traps at different temperature is used to explain this behavior [Yang96], but it seems more promising to consider the interaction between electrons and phonons as the source for the temperature dependence [Pipi99].

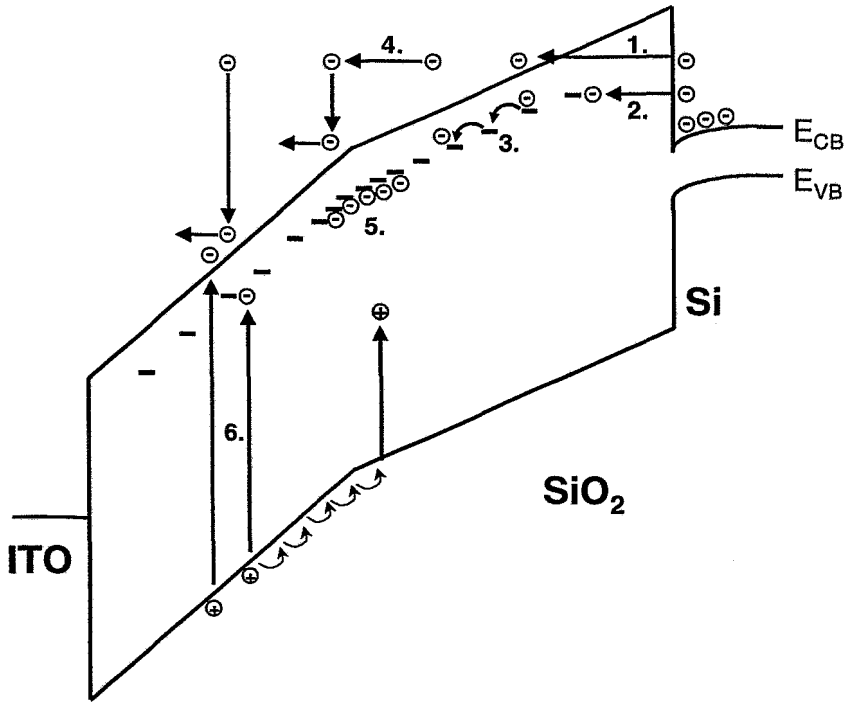


Fig. 5.10.:
Injection and conduction mechanisms in SiO_2.
(1) FN-tunneling, (2) TAT, (3) Hopping or PF conduction, (4) free movement in the SiO_2 conduction band including scattering events, (5) charge trapping, (6) impact ionization / trap assisted impact ionization

If there is a considerable amount of traps within the oxide, the electrons can also be transported between the traps by Hopping or Poole-Frenkel (PF) conduction (process 3). PF-conduction is used to describe the IV characteristics of non-volatile memories based on N-doped amorphous carbon layers [Gers98]. The model of PF-conduction is also applied

in [Buss01] for the case of as-implanted SiO_2 while for an implanted and annealed SiO_2 layer TAT mechanism is observed.

Another possibility is the quasi-free movement of the electrons in the conduction band of SiO_2 (process 4). In the case of thermally grown SiO_2 the electrons will be accelerated by the high electric field, but loose energy by phonon scattering and impact ionization [Naza02]. Whereas phonon scattering is efficient for low kinetic energies, impact ionization occurs only for kinetic energies above the band gap energy of SiO_2 of approximately 9 eV. In steady state the electrons can be characterized by a distinct energy distribution depending on the position in the oxide and the electric field. After a mean path length depending on the electric field the energy distribution will saturate. As a result the mean kinetic energy of the electrons in the conduction band of pure SiO_2 is rather high for high electric fields and amounts to 2...4 eV for electric fields higher than 7 $MVcm^{-1}$ [Arno94, Fisc85]. Also the number of electrons having energies higher than 9 eV becomes non-negligible at 7 $MVcm^{-1}$ and grows rapidly with increasing electric field.

In the case of implanted oxides the model has to be modified. Both the trapping of electrons and the scattering of electrons at defects are efficient processes to decelerate electrons. Furthermore it could be possible that the ionization of LCs requires an energy less than 9 eV, and finally trap assisted ionization (process 6) can occur. All these processes will lead to a reduction of the mean kinetic energy of electrons moving in the SiO_2 conduction band. Indeed, the trapping of electrons will cause additional effects, namely the buildup of a negative space charge (process 5) counteracting the further injection of electrons. As shown in Fig. 5.10 the negative potential of the space charge will lift the SiO_2 conduction band which lowers the local electric field at the SiO_2-Si interface. In contrast to this the local electric field at the metal gate is increased. Corresponding to the increase and decrease of the local electric field the mean kinetic energy of the electrons increases and decreases, respectively.

5.2. CV – Characterization

High-frequency (100 kHz) capacitance voltage investigations (HF-CV) of the Ge implanted samples show a very strong influence of the implantation and annealing conditions on the flatband voltage shift. In Fig. 5.11 a comparison of the samples implanted with different ion energies to doses of 1..6 at% is displayed.

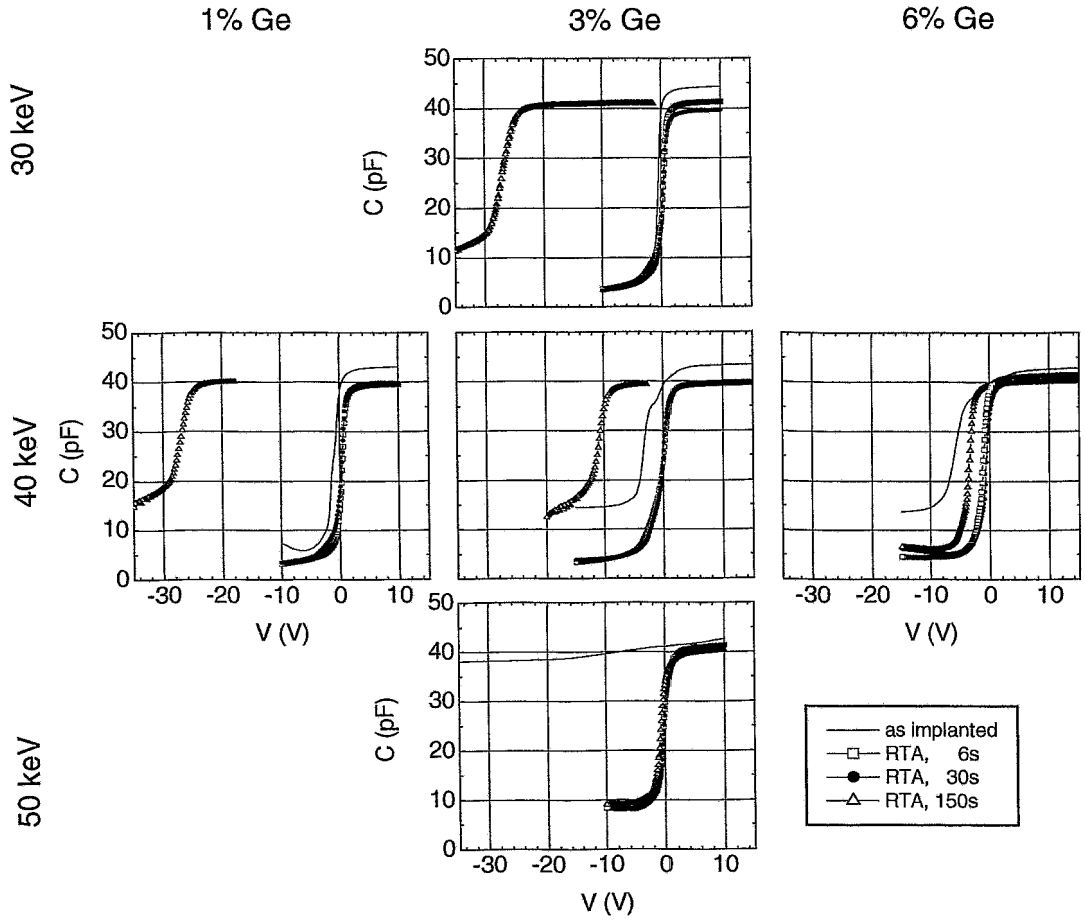


Fig. 5.11:
HF-CV investigations of Ge^+ implanted SiO_2 layers (80 nm) after different annealing procedures (RTA at 1000°C for various times).

With increasing ion energy the as-implanted samples exhibit a strong shift of the CV curves towards negative voltages which implies the accumulation of positive charge. This behavior can be explained by the well known effects of radiation damage occurring when an oxide layer is exposed to radiation (see [Hori97] and references therein). If the energy of the radiation is higher than the SiO_2 bandgap (9 eV) the generation of electron-hole pairs may occur. Some of the generated holes are captured in hole traps. Since these hole traps are mainly distributed around the Si/SiO_2 interface, one can understand the strong

effect of positive charge accumulation which was observed by comparing the CV characteristics of the as implanted samples. Hereby the influence of the implantation energy is much more dominating than that of the implanted ion fluence. The slope of the CV characteristics decreases with increasing ion energy which implies that the amount of interface states increases. The same effect was observed for increasing ion fluences.

For better comparison Fig. 5.12 shows the calculated V_{FB} values of the different samples. Moderate annealing for 6 or 30 s leads to a reduction of the positive charge concentration for all samples which can be observed by the curve shift close to 0 V. However, the 150 s anneal again enhances the accumulation of positive charge. This effect occurs especially for the 30 keV implantation and for the sample containing 1% Ge (40 keV). Samples with the deeper implants (50 keV) and also the 6% implant annealed for 150 s do not show such a strong accumulation of positive charge during annealing. For the 50 keV implant even nearly identical curves were observed for the three annealing times. So the effect of positive charge generation after longer annealing should be related to the loss of Ge from the R_p region. This can be seen in the RBS spectra shown in section 4.2.2, Fig. 4.6 and 4.7. The peak in the bulk region is strongly decreased, e.g. to a Ge content below $5x10^{14}$ cm^{-2} for the 150 s annealed 30 keV implant. Since the Ge in this bulk region is responsible for the trapping of electrons, only the positive charge trapped at the interface contributes to the totally trapped charge.

Comparing the IV (Fig. 5.1) with the CV characteristics (Fig. 5.11) one can also conclude that samples with the 6 s and the 30 s anneal are similar concerning their electric properties. However, MOS devices with the 150 s anneal show a completely different behavior - except for the high Ge-fluence or the high energy implant.

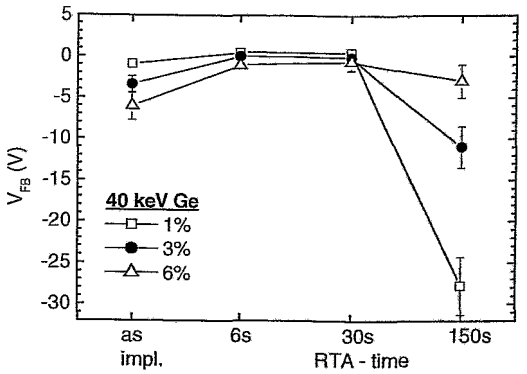


Fig. 5.12a:
Shift of the CV curve after RTA. The amount of positive charges present in the as-implanted state is first reduced after annealing up to 30 s but then it increases again for longer annealing times.

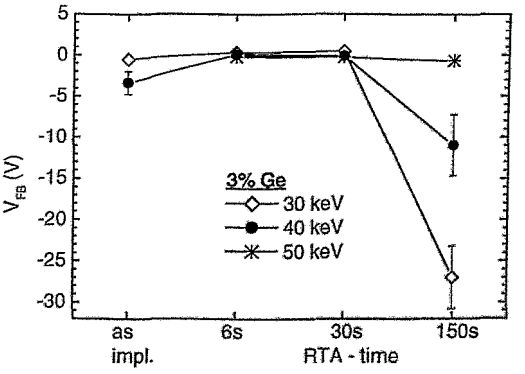


Fig. 5.12b:
CV-results after RTA for different times. Note that V_{FB} could not be determined for the 50 keV as-implanted case. Positive oxide charges increase with implantation energy in the as-implanted state, but decrease after annealing.

5.3. Determination of the charge centroid

The position of the charge centroid was determined by photo-IV measurements (see section 3.3.2 for details). Fig. 5.13 shows the position of the centroid, the RBS peak and the TRIM peak. The RBS data are in good agreement with the TRIM data in Fig. 5.13a. The variation of the ion fluence causes a slight shift of the RBS peak towards deeper regions with increasing Ge concentration (Fig. 5.13b). This behavior is in good agreement with the shift of the Ge - profile during annealing caused by diffusion processes. The diffusion of Ge towards the Si/SiO_2 - interface region is more pronounced for higher Ge concentrations and thus the charge centroid is located closer to the interface.

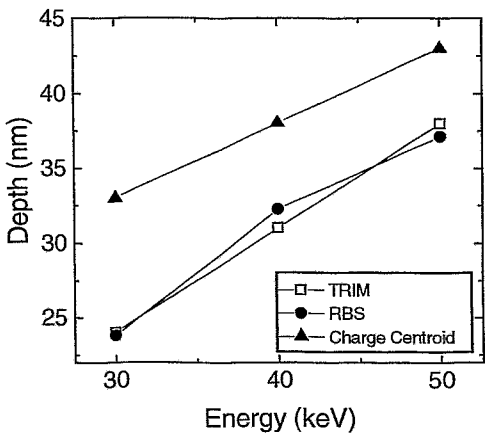


Fig. 5.13a:
Charge centroid and peak position of RBS measurements and TRIM calculations for different implantation energies. The Ge peak concentration is 3%.

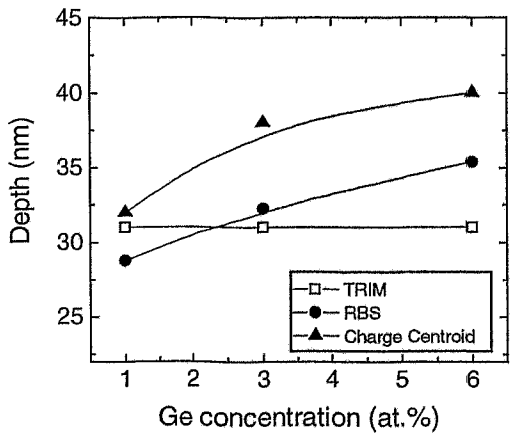


Fig. 5.13b:
Charge centroid and peak position of RBS measurements and TRIM calculations for different Ge concentrations. The implantation was performed at an energy of 40 keV.

In the literature a similar behavior for As^+ implanted SiO_2 layers [DeKe80] was reported. There the centroid of the charge distribution is proportional to the implantation energy. However, a dependence on the implanted ion fluence and also on different annealing regimes was not observed. This indicates a low diffusivity of the As atoms in the SiO_2 matrix. Investigations of the shift of the charge centroid after FN-stress are reported in [Okho98]. The results can be related to the formation of additional traps.

Another method which one could also use to determine the position of the trapped charge in a oxide is the evaluation of changes in the FN-curve after constant current stress. It was described by DiMaria [DiMa76] and improved by Kies [Kies96] et al., considering not only the charges outside of the tunneling region but the whole charge in the oxide. There the FN-curve measured after stress is simulated using different charge densities and charge distributions.

To get information about the energetic position of the traps a method using light for depopulation of the occupied traps is possible. By changing the energy of the photons starting at low energies an increase in the current should be observed when the energy of the photons is sufficient for activation of an electron from a trap. This could be realized by using an intense lamp and a monochromator for adjustment of the wavelength. The amount of charges stored in the oxide could also be determined using the flatband voltage from the CV results. Another method for activation of electrons from trapped states is the depopulation by thermal activation [DeKe80]. This method cannot be used for deeper traps, since the temperatures required for the thermal activation become too high. In the case of SiO_2 layers containing clusters this could lead to changes in the microstructure of the samples.

First investigation of the depopulation of charged traps, which should be discharged when light of a specific wavelength is applied, were also carried out in our investigations. The energy of the photons should give information about the depth of the traps. However, it has to be mentioned that very long measuring times are necessary to observe remarkable detrapping effects since the intensity of the light is strongly reduced due to the use of the monochromator. In order to investigate these effects in more detail a more specific sample preparation with ultrathin, transparent contacts has to be carried out in the future.

5.4. Effects of electrical stress

5.4.1. Charging effects during constant-current operation

The trapping behavior of the modified SiO_2 layers during high-field electron injection from both, the Si substrate and Al gate was investigated by two methods:

(i) using the HF-CV method the shift of the flatband voltage was studied. This shift is a measure for the trapped charge. From the direction of the shift the polarity of the trapped charge can be determined.

(ii) V(t), the change of the applied voltage during the time of constant current injection was detected. From this shift the trapped charge can be calculated.

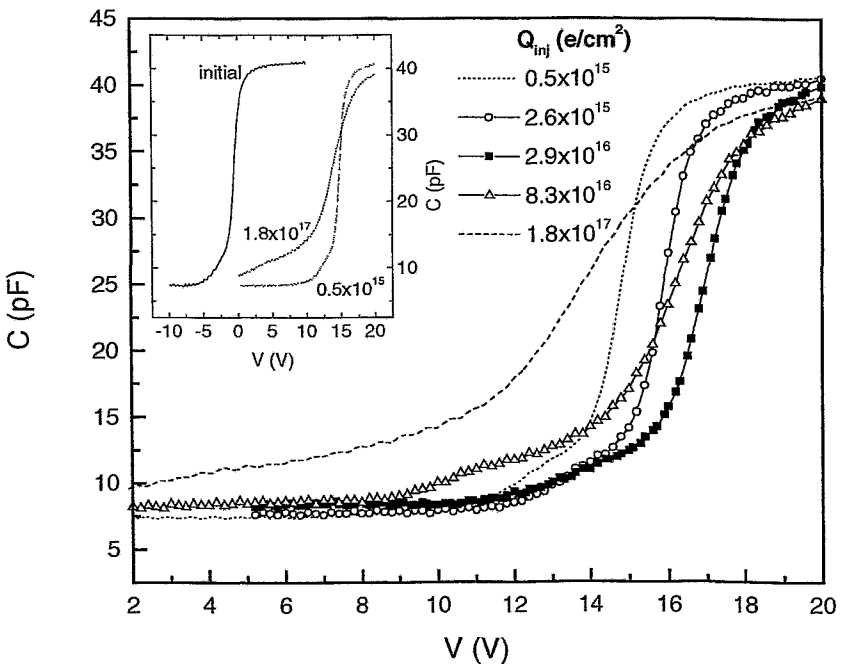


Fig. 5.14:
CV characteristics after electron injection from the Si substrate. Constant current (+2x10^{-5}Acm^{-2}) was applied to the sample implanted with 50 keV Ge (3%, 150 s RTA at 1000°C). The data in the legend describe to amount of injected charge. The inset (different V-scale) shows the initial CV curve beside two curves from the main plot. The injected charge leads first to a shift of the CV curve towards positive voltages, but then the CV curve shifts back.

High-field electron injection was performed in a constant-current regime. The used current density of 2x10^{-5} Acm^{-2} corresponds to the typical EL operation regime of such devices. The amount of injected charge is 1.25x10^{14} e/cm^2 per second. By applying a positive voltage to the gate contact electrons are injected from the Si substrate while negative voltage causes the injection of electrons from the Al electrode. Fig. 5.14 shows the results of CV measurements for electron injection from the Si substrate. The initial CV

characteristics is shifted towards positive voltages due to the trapping of electrons in the oxide up to an injected charge of $2.9x10^{16}$ e/cm^2. Then the curve shifts back towards negative voltages. This means that positive charges are generated. In addition to that the slope of the characteristic decreases indicating that the density of interface states at the Si/SiO_2 interface is increased.

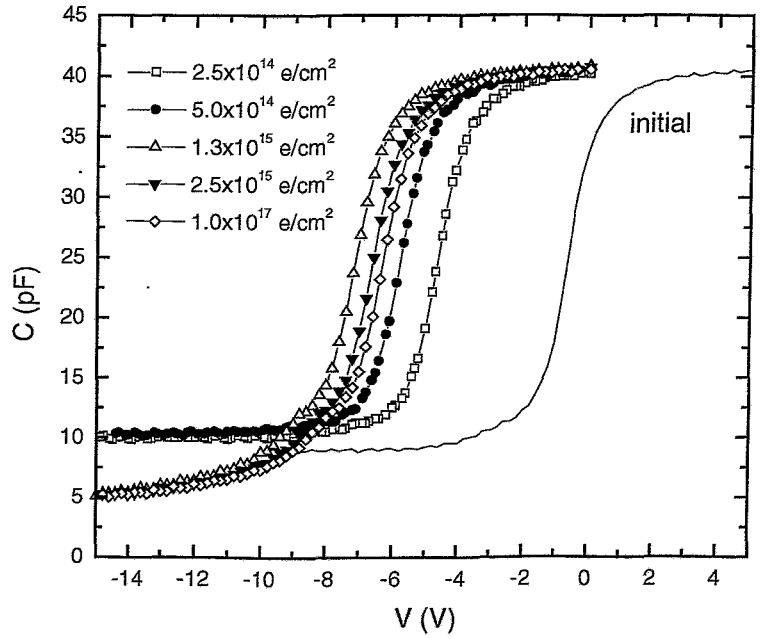


Fig. 5.15:
CV characteristics after injection from the Al gate. Constant current density of $-2x10^{-5}Acm^{-2}$ was applied to the gate of the sample implanted with 50 keV Ge (3%, 150 s RTA at 1000°C).

The results from CV investigations after electron injection from the Al gate are given in Fig. 5.15. First the initial CV curve is shifted into the negative voltage region indicating that trapping of positive charges or detrapping of negative charges occurs. Then the curve shifts back, which means that now negative charges are trapped. The interface state density does obviously not increase significantly since no remarkable changes in the slope of the CV curve can be observed. However, non-equilibrium effects occur in the CV characteristics after injecting a charge of more than $1.25x10^{15}$ e/cm^2 (corresponding to a charging time of 10 s). This behavior can be attributed to induced leakage current.

Results from V(t) measurements for electron injection from both the Si substrate and the Al gate electrode are shown in Fig. 5.16. For injection from Si a monotonic increase of the voltage is observed indicating that negative charges are trapped. For injection from the metal gate a different behavior is found. First, the voltage (plotted as an absolute value) decreases, but then the characteristic is changing into the opposite direction.

For the case of injection from the Si substrate the question arises, how the different results of the V(t) and the CV investigations can be understood. With the V(t) method, only negative charge trapping was detected, while with the CV method an increase of the trapped positive charge for longer injection times was observed. The explanation of this

effect can be given by considering the different oxide regions the two methods are sensitive to. The V(t) method is insensitive to the region close to the injecting interface, since charges in this position do not lead to strong band bending which influences the shape of the whole barrier. This means that for the case of injection from the Si substrate the charges trapped at the Si/SiO_2 interface cannot be detected by this method (Fig. 5.17a). Contrary to that CV investigations give information over the whole layer. It has to be mentioned that charges in the volume give a weaker contribution to the shift of the CV curve than charges trapped at the Si/SiO_2 interface. For the case of injection from the metal gate the V(t) method should be sensitive to the whole amount of trapped charge (Fig. 5.17b).

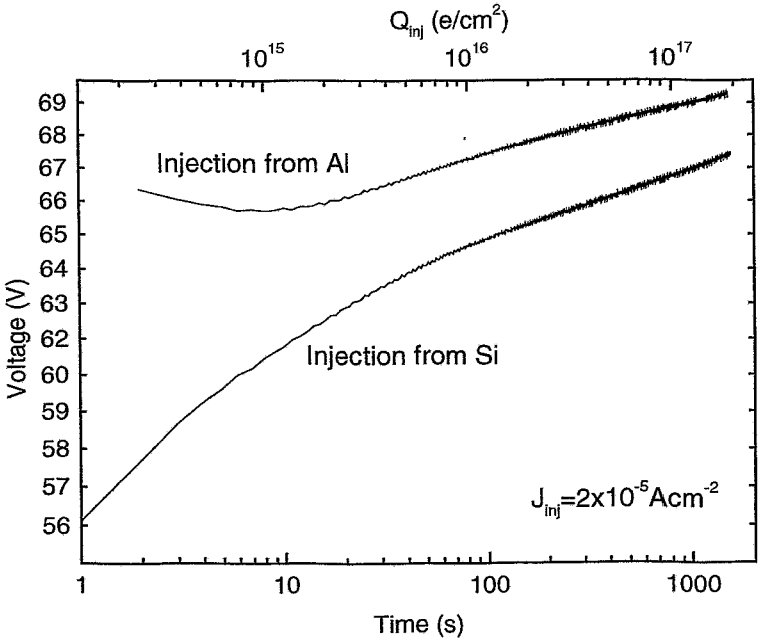


Fig. 5.16:
V(t) investigation during constant current stress for a 50 keV Ge implanted SiO_2 layer, annealed for 150 s. The injection was carried out from both, the Si substrate and the Al electrode.

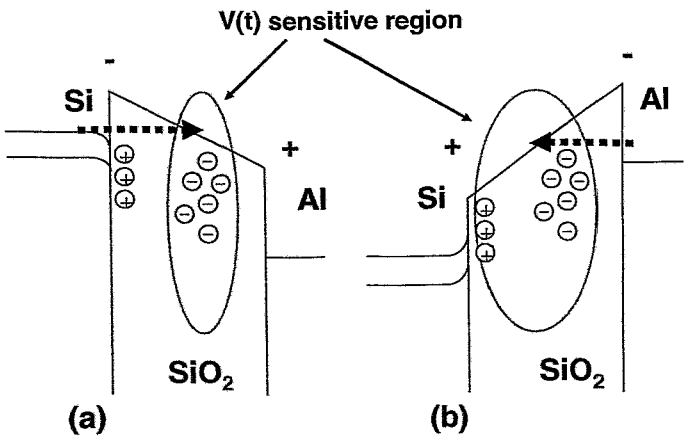


Fig. 5.17:
Schematic band structure for injection from the Si - substrate (a) and the metal gate (b). The V(t) method is not sensitve to the region close to the injecting interface.

The observed effects imply the following: the amount of the trapped charge derived from CV measurements is related to the total net charge, which consists of positive and negative charges in the oxide. Since the V(t) method shows only electron trapping and is not sensitive to the interface region in the case of injection from the Si substrate, there is a strong indication for the trapping of positive charge at the interface. Therefore, by using the two methods, the separation of the different kinds of charge can be carried out – at least for the case of injection from the Si substrate.

To give a more detailed description of the effect, the accumulation of the different charges for injection from the Al electrode and from the Si substrate is shown in Fig. 5.18. The figure (a) on the left hand side displays the case for injection from the Si substrate. Here the charges are related to trapped electrons. The difference of the calculated charges from the CV and the V(t) method is given as Q_{pos} and represents positive charges. The observed characteristics implies the following scenario during the constant current stress: Electrons are trapped in the volume of the SiO_2 layer, but with increasing stress time also positive charges are trapped near the SiO_2/Si interface region. This leads to a decrease of the trapped net charge. The accumulated positive charge is a strong indication for beginning device breakdown due to oxide degradation [Hori97].

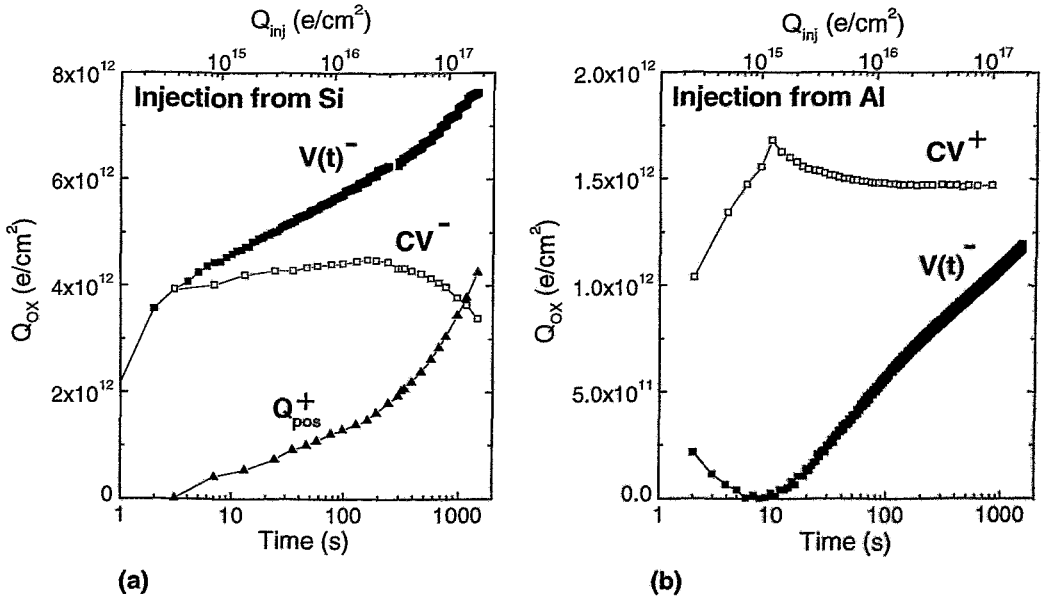


Fig. 5.18:
Trapped charge after constant current stress for oxides implanted with 50 keV Ge (3 %), treated with RTA at 1000°C for 150 s. Injection from the Si substrate (a) was carried out by applying a positive voltage to the gate electrode, injection from the Al electrode by applying a negative voltage (b). The CV and the V(t) method were used. The + or - sign is related to the type of trapped charge. Please note that the vertical scales differ by factor of 4.

For the case of injection from the Al electrode different effects occur. The data in Fig. 5.18b are related to positive and negative trapped charge for the CV and the V(t) investigations, respectively. Both, the CV and the V(t) curve exhibit turning points after the comparable amount of injected charge. This strongly implies a scenario of two competing trapping effects which occur.

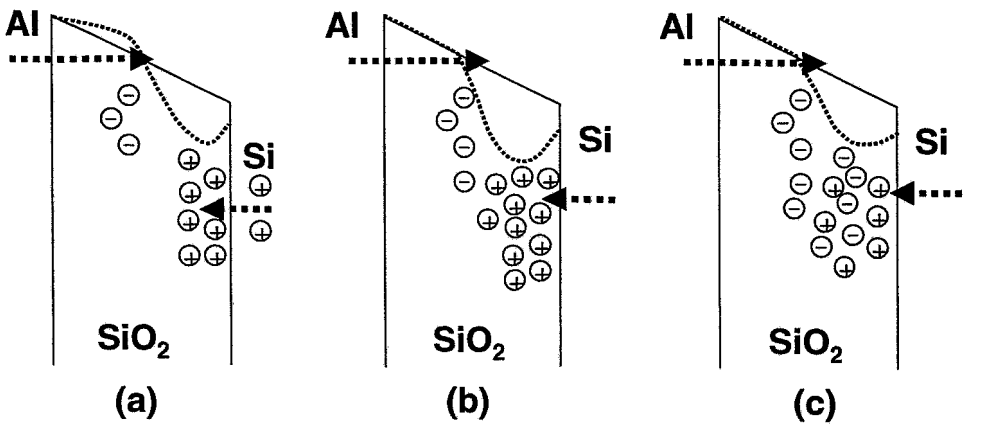


Fig. 5.19:
Injection from the Al electrode. Both, electrons and holes are injected. Three different stages occur: (a) hole trapping dominates, (b) if the amount of trapped positive charge reaches a critical value, the band bending causes a strong increase in the amount of injected electrons. (c) Both types of charge are trapped now, but electron trapping becomes more and more dominating.

First, the trapping of positive charges is dominant (Fig. 5.19a). This leads to an additional band bending making the barrier "thinner" for electrons injected from the Al electrode. At a certain point the bending reaches a value, where the electrons can easily tunnel trough the barrier (Fig. 5.19b). Both processes compete with each other leading to an equilibrium like state as shown for the CV characteristics in Fig. 5.18b. The results of the V(t) measurements indicate that the trapping of electrons is enhanced (Fig. 5.19c). Since in this case the V(t) method should be sensitive to both, the bulk and the Si/SiO_2 interface (see Fig. 5.17b), one cannot simply calculate the trapped positive charge as in the case for injection from the silicon substrate.

5.4.2. Charging effects during high-field stress

While section 5.4.1 was dedicated to charging effects at constant-current operation, now the influence of high-field stress will be discussed. The MOS-devices were stressed using well defined voltage ramps, starting from 0 V up to a target voltage of 20...80 V. After each ramp a CV scan was performed. Fig. 5.20 shows the CV characteristics measured after different voltage ramps. The unimplanted layer shows a trapping of positive charges which increases for higher voltages. The slope of the curve decreases at higher voltages, which indicates the formation of interface traps. Especially for the 0...60 V ramp this effect can be clearly observed.

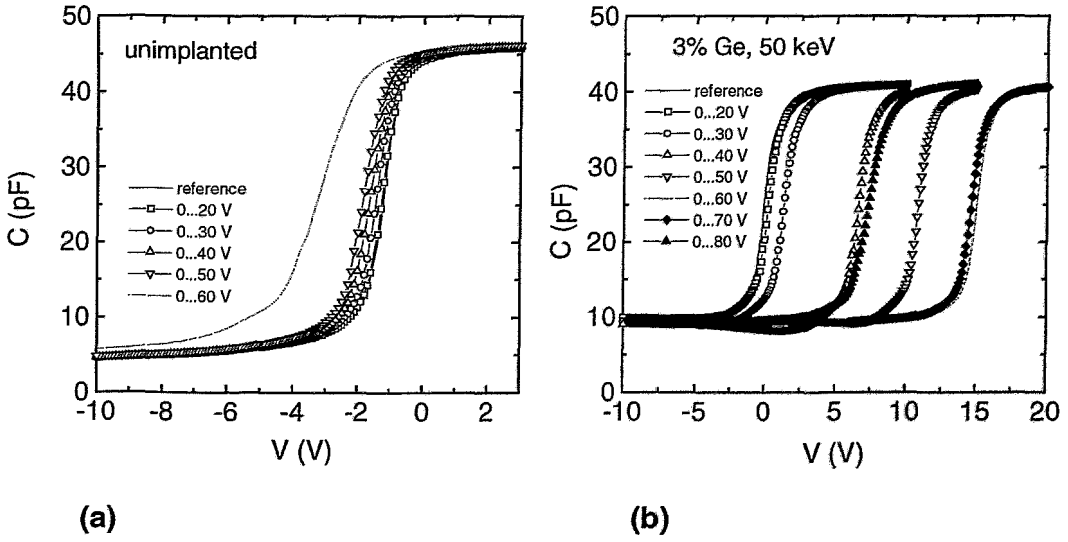


Fig. 5.20:
CV characteristics after high field stress. After a voltage ramp a CV scan was performed. The unimplanted SiO_2 layer (a) shows a shift towards negative voltages for higher electric fields indicating hole trapping. Ge implanted layers (b) exhibit electron trapping (open symbols) up to voltages of 60V (about 7.5 $MVcm^{-1}$). If higher electric fields are applied, positive charges are trapped which leads to a backshift of the CV curve (solid symbols). Note, that the voltage scales of (a) and (b) are different.

For implanted layers the behavior is different as shown in Fig. 5.20b. At moderate electric fields electron trapping is observed, which leads to a shift of the CV curve towards positive voltages (displayed by the open symbols). In the high field region the trapping characteristics is changed. A back-shift of the CV curve is observed which indicates additional trapping of positive charge (solid symbols). The slope of the curve also changes at higher voltages, which can be seen for instance for the voltage ramp from 0...80V.

For the explanation of this behavior several aspects have to be taken into consideration. Electrical stress at high electric fields is known to cause additional defects in the oxide. Hot electrons which are present in the SiO_2 conduction band at high electric fields (E>7$MVcm^{-1}$) [Fisc85, Arno94] may perform impact ionization. If - like in the case of Ge implantation - traps are already initially present, trap-assisted impact ionization can occur. Electron-hole pairs are formed, and because of the high kinetic energy of the

impacting electrons bonds in the SiO_2 structure may be broken. The holes which are produced during the impact events may be trapped, e.g. in NOV [Hori97]. This and additional effects like the so called stress-induced leakage current (SILC) are well known precursors for the oxide degradation and the beginning device breakdown [Mira99].

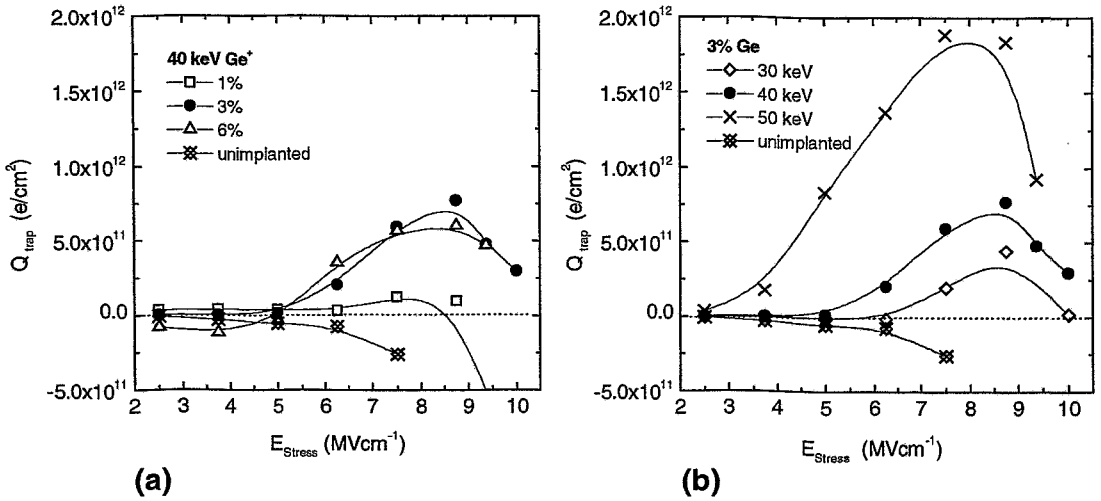


Fig. 5.21:
Trapped charge after different voltage ramps. The sweeps were performed from 0 up to the electric field E_{stress}. The value of Q_{trap} is related to the number of trapped electrons per cm^2.

A comparison of the trapping behavior for different implantation energies and doses is given in Fig. 5.21. The charge is related to trapped electrons, so negative values mean positive trapped charges. For the unimplanted case we observe such a positive charge trapping which should be related to destructive processes leading to oxide degradation. The Ge implanted layers show the trapping of electrons, with a maximum at a Ge concentration of 3% (Fig. 5.21a). For a concentration of 6% Ge no further increase of the trapped charge can be seen. This might be caused by the possible transformation of "trapping" defects into cluster-like structures. These clusters are still a center for defects, e.g. at the surface of the clusters or in the vicinity of the cluster band, but the total number of defects might be decreased. Fig. 5.21b shows the trapped charge as a function of the implantation energy. The strong increase for higher energies indicates the importance of the trap position relative to the Si/SiO_2 interface. In good correlation to the results from RBS (Fig. 4.6) we see that not the total amount of Ge in the volume (integrated RBS results show variations between the three plots with a maximum factor of only 1.5), but the amount of Ge at the interface may explain this behavior.

In order to investigate the influence of the trapped charge on the IV curves, an additional IV scan was performed after the CV characterization used for the determination of the trapped charge described in the previous section. The devices were driven until breakdown. The results of these measurements are plotted for the 50 keV Ge implant in Fig. 5.22. For pure oxide layers no noticeable changes in the IV characteristics were detected after the stress procedures (data not shown here). However, for Ge implanted layers a clear shift of the IV curve towards higher electric fields was observed. At first

sight this seems to be in contradiction to the data known from the literature describing SILC like effects after application of high electric fields [Scar00, DeSa00]. In that cases a shift towards lower electric fields is described which is explained by additional leakage paths caused by the electrical stress. The shift which is observed here cannot be explained by such destructive mechanisms. Obviously, the trapped charge plays the dominating role here, since the effects can be very well correlated to the onset of charge storage as shown in Fig. 5.21b. The trapped charge leads to an increase in the barrier height which means that higher electric fields have to be applied in order to achieve electron transport through the oxide.

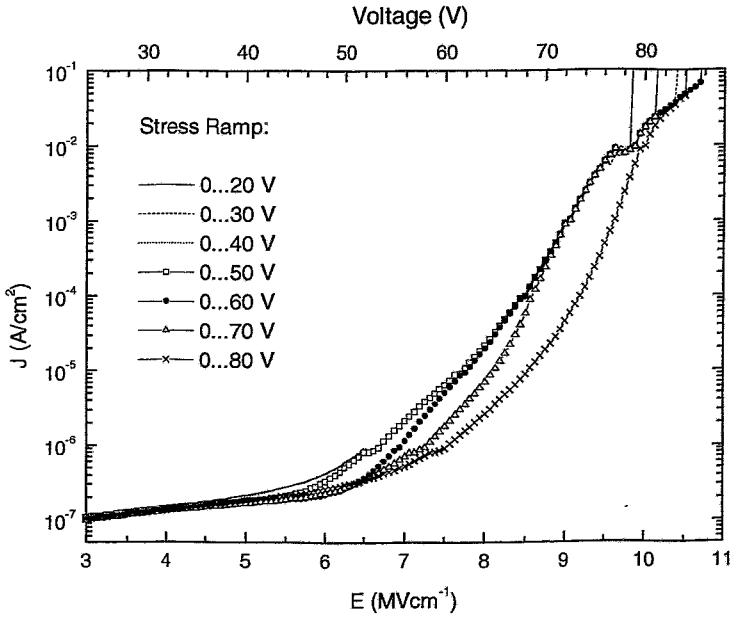


Fig. 5.22:
IV characteristics taken on stressed devices. The stress was performed by an IV scan up to a certain voltage. A shift of the curves towards higher electric fields is observed indicating that charge trapping occurs.

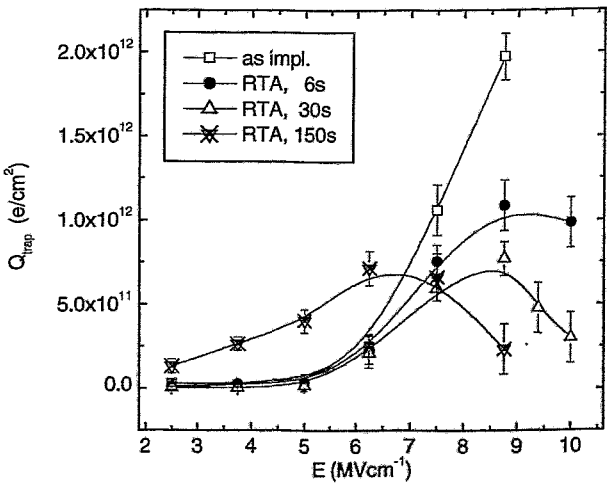


Fig. 5.23:
Trapped charge after a voltage sweep for samples implanted with 40keV Ge^+, 3%. Annealing was performed with RTA, 1000°C for different times. The plot shows the trapping of negative charge. At high electric fields positive charge trapping occurs.

The influence of the annealing time on the trapping properties is shown in Fig. 5.23. Two main effects can be observed. First, the trapping of electrons reduces with annealing time. So obviously the number of electron trapping centers is decreased. Second, the onset of the positive charge trapping occurs earlier. From the RBS results (section 4.2.2) we know that the amount of Ge at the Si/SiO_2 interface increases. This could lead to an easier injection of electrons which give rise to the presence of hot electrons at lower voltages.

5.4.3. Trapping- und detrapping parameters

The charging properties of Ge implanted SiO_2 layers were investigated using constant current injection and a combination of CV and IV-ramp measurements. Fig. 5.24 shows the trapped charge derived from CV measurements as a function of the injected charge. A constant current of $1x10^{-5}Acm^{-2}$ was applied to the gate. The 3% Ge implant exhibits the largest amount of trapped charge. This implies that the 6% Ge implant may lead to the formation of different trapping sites which do not act as efficient trapping centers as for the 3% Ge sample. This is also related to the luminescence properties as will be discussed in detail in chapter 6.1.4.

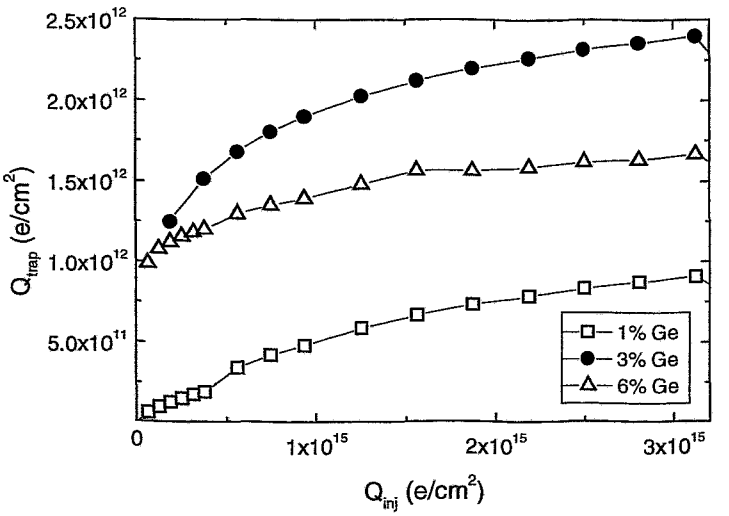


Fig. 5.24:
Trapped charge as a function of injected charge for 40 keV Ge implanted 80 nm thick SiO_2 layers. Constant current was applied ($10^{-5}Acm^{-2}$) for charging.

Using the results of both CV and V(t) measurements the negative and positive charge concentration was calculated. In Fig. 5.25 the total net charge (a) as well as the calculated positive and negative charge concentration (b) after electron injection from the Si substrate are displayed. The total net charge, which is negative and therefore given in the unit e/cm^2 increases very rapidly after beginning injection. Then a saturation level is reached. The sample with 30 s RTA reaches a slightly higher level than for the one with 6 s RTA. After further injection the sample annealed with 150 s RTA shows a decrease in the net charge while the other samples remain in the saturation-like state. This is related to the generation of positive charge. The effect was investigated in more detail by calculating the two different types of charge as shown in Fig. 5.25b. It can be seen that the total amount of

trapped negative charge increases with annealing time. Contrary to the net charge shown in Fig. 5.25 (a) no real saturation, but a continuing increase of the negative charge concentration is observed. Hereby the slope of the negative charge concentration as a function of the injected charge increases with annealing time. As already shown in the IV and CV investigations, the properties of the samples with 6 s and 30 s RTA are quite similar, while the 150 s RTA samples shows a remarkable difference. This is even more pronounced, if compared to the trapped positive charge. While for the sample with 6 s RTA a saturation is reached at about $5x10^{11}$ e/cm^2, the sample annealed with 150 s RTA shows an ongoing increase reaching values of $2.2x10^{12}$ e/cm^2 after injection of $1.9x10^{17}$ e/cm^2.

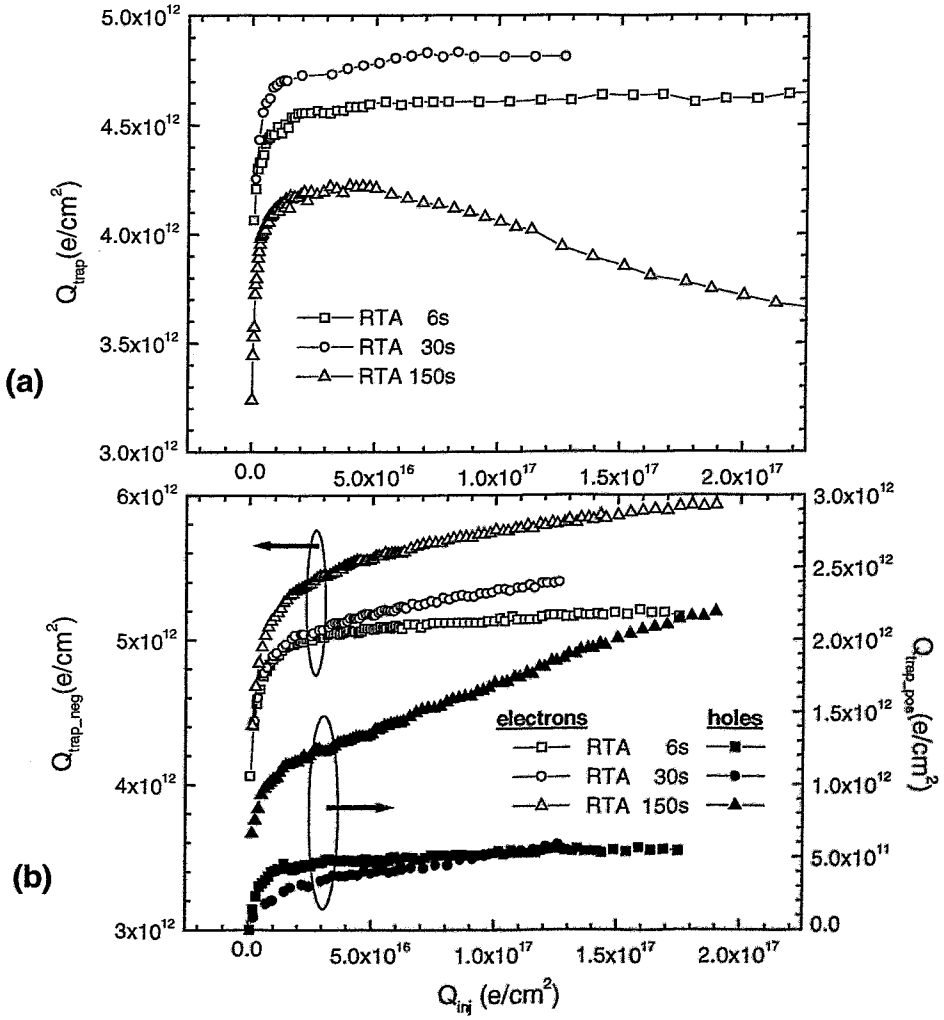


Fig. 5.25:
Trapped charge after electron injection from the Si - substrate for a 50 keV, 3% Ge implanted SiO_2 layer. In (a) the total net charge derived from CV measurements is displayed. Using both, the results from CV and V(t) measurements the trapped positive and negative charge was calculated and plotted in (b). The left scale of the diagram (b) is related to trapped electrons, the scale on the right hand side to trapped holes. Please note that the scales differ by a factor of 2.

To characterize the trapping behavior in more detail, the so called trapping efficiency P_{trap} can be calculated using the equation [Naza02]:

$$P_{Trap} = \frac{dQ_{trap}}{dQ_{inj}} = N_{trap\_eff} \cdot \sigma_i \cdot e^{(-\sigma_i Q_{inj})} \tag{5.1}$$

where

$$N_{trap\_eff} = \frac{x_T}{d_{ox}} N_{trap} \tag{5.2}$$

Here x_T is the location of the charge centroid, d_{ox} is the oxide thickness and σ_i is the capture cross section of the trap. N_{trap_eff} represents the effective and N_{trap} the real trap concentration, respectively. Using formula (5.1) via the plot $\ln(P_{Trap})$ vs. Q_{inj} (plot not shown here) both, the effective trap concentration and the capture cross section of the trap can be determined. If several kinds of traps are present, the plot is characterized by different sections with different slopes. A more detailed description of the method is given in [Hori97].

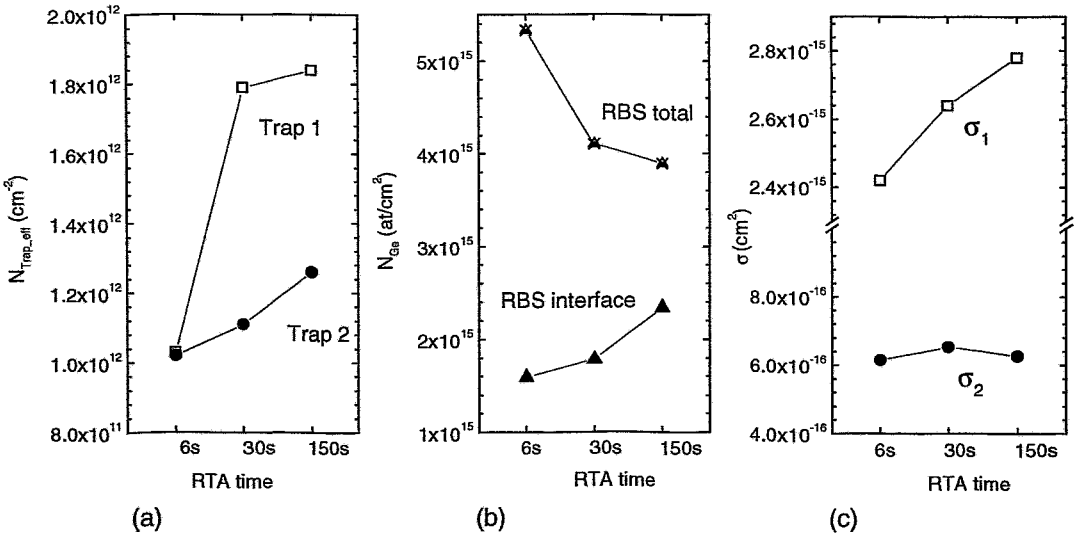


Fig. 5.26:
The effective trap concentration as a function of annealing time is shown in figure (a). The concentration of Ge (total and IF region) derived from RBS is plotted in Figure (b). The right figure (c) displays the capture cross section. (parameters: 80 nm SiO_2, 50 keV Ge, 3%)

For oxide layers with a thickness of 80 nm, implanted with 50 keV Ge^+ ions (3%) two traps were found. The results of electron trapping characteristics (Fig. 5.26a) of the observed types of traps show an increase in the trap concentration for longer annealing times. It has to be mentioned that the calculated trap densities give only a value for the effective trap density according to formula (5.2). So basically, if the traps are distributed in the volume of the oxide layer, this value always underestimates the real trap concentration. The density of both trap types increases for longer annealing times. In order to correlate this to the Ge concentration in the SiO_2 layers, Fig. 5.26b gives the RBS values for both, the total Ge concentration in the layer and the amount in the interface region. Since the total amount of Ge is reduced in the oxide layer during annealing (see Fig. 4.8 in section 4.2.2 for details) the increase of the trap densities for longer annealing has mainly to be attributed to the redistribution of Ge, especially the diffusion of Ge towards the interface region. Of course one also has to take into account the effects of cluster evolution due to Ostwald ripening. Although no clusters were observed in the TEM investigations, the formation of tiny Ge islands should occur under these annealing conditions.
The concentration of trap 1 is significantly larger compared to trap 2 for longer annealing times. Since trap 1 describes the trapping in the very beginning of injection, this could be attributed to a even more dominant effect at the interface. The cross section of trap 1 is about 4 times larger compared to that of trap 2 (Fig. 5.26c) and shows a remarkable increase during annealing which leads to the assumption that, in contrast to trap 2, for trap 1 effects of beginning cluster growth have to be considered. This would also explain the increase in the capture cross section.

Since microstructural and optical investigations did not give a strong indication for cluster related quantum effects, other processes must cause the trapping of charge. The results of the investigations previous sections (5.4.1 and 5.4.2) showed that the implanted Ge which is present in the oxide layer is responsible for the trapping of charge. But how do the trapping centers look like and how can the trapping mechanisms be understood ?

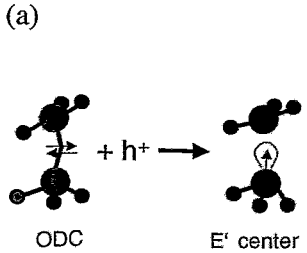


Fig. 5.27a:
Structure of an NOV which is transformed into a E' center after hole trapping (after Hori97]).

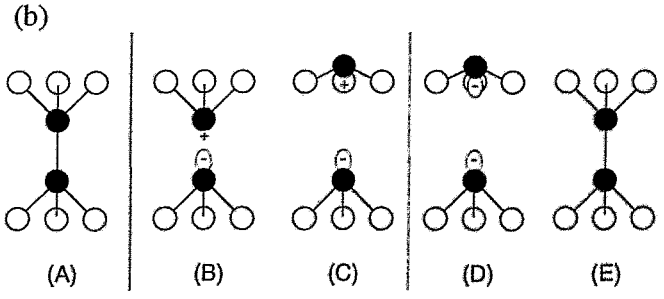


Fig. 5.27b:
Possible trapping mechanisms of NOV and E' centers (after [Kaln90b]). The full symbols represent Si atoms, the open ones oxygen atoms. (A) neutral bonded center, (B) immediately after electron detrapping, (C) after subsequent relaxation, (D) immediately after electron trapping, (E) relaxation and rebonding to the original condition

During the process of ion implantation and the following annealing steps E' centers and ODCs are formed. The basic structure of such an oxygen deficiency center, here in the special case of the NOV, is sketched in Fig. 5.27a. After hole trapping, the Si-Si bond is broken and thus an E' center is formed. In Fig. 5.27b the trapping processes are explained in detail. The neutral bonded center (A) may be broken into a E' center (B) by trapping of a hole and then relax as shown in (C). Hori [Hori97] describes this as an irreversible process being a strong precursor for beginning device breakdown. However, in [Kaln90b] the electron trapping of E' centers is described as an process leading to the formation of a NOV (D,E).

5.5. Investigation of memory properties

5.5.1. Electrical investigations of MOS devices

5.5.1.1. Stored charge

The programming window ΔV_{PW} of the devices is defined as the difference of the shift of the CV-curve under flatband conditions after applying positive or negative voltage pulses to the gate contact which leads to "writing" or "erasing" of the MOS capacitors. Fig. 5.28 shows the programming window as a function of the programming voltage for 20 nm thick oxide layers implanted with Si^+ ions to fluences of 5, 7 and $9x10^{15}cm^{-2}$, respectively. The applied programming voltage pulses with an amplitude of $\pm V_{prog}$ had a pulse length of 100 ms. The size of the programming window increases with V_{prog} and reaches a saturation value. The onset of observable programming windows is shifted towards lower voltages for SiO_2 layers containing a higher amount of implanted Si. This can be explained by the charge injection and transport behavior which was discussed for the IV-characteristics already in Fig. 5.3a. Since samples with higher Si concentration show an enhanced electric current at lower electric fields, the amount of charge which can be trapped increases. The observed programming window for an implantation fluence larger than $7x10^{15}$ cm^{-2} reaches values above 0.5 V, which is of practical relevance [Thee00, Gebe00a].

Germanium implanted samples, which were intensively investigated regarding the microstructure, exhibit much stronger programming effects at low voltages. Fig. 5.29a shows a comparison of 12 and 20 keV Ge implanted 20 nm thick SiO_2 layers. It can be seen that the interface implant (20keV) leads to an enormous increase of the programming window. The 12 keV Ge implant shows a beginning saturation at programming voltages around 6 V. It also has to be mentioned that these samples are very sensitive to the scanning regime used for the determination of the flatband voltage. A direct comparison between Si and Ge implanted gate oxides is given in Fig. 5.29b. Pulses of +/-12.5V for 100 ms were used to perform the "write" and "erase" procedures. It can be seen especially for higher fluences that the 12 keV Ge implant, which is comparable to the Si implant regarding the profile and the dpa value at the interface, results in much weaker trapping effects.

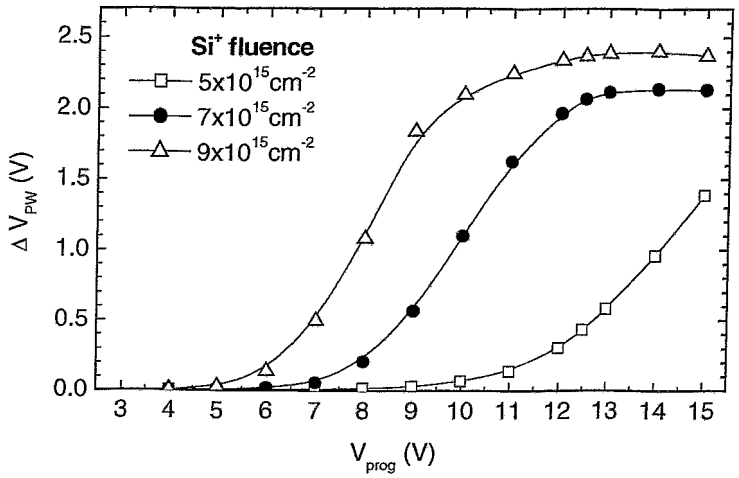


Fig. 5.28:
Programming window ΔV_{PW} as a function of the stress voltage for 20 nm oxide layers implanted with Si^+ ions to fluences of 5, 7 and $9x10^{15}cm^{-2}$, respectively. The applied voltage pulses $\pm V_{prog}$ for programming had a pulse length of 100ms.

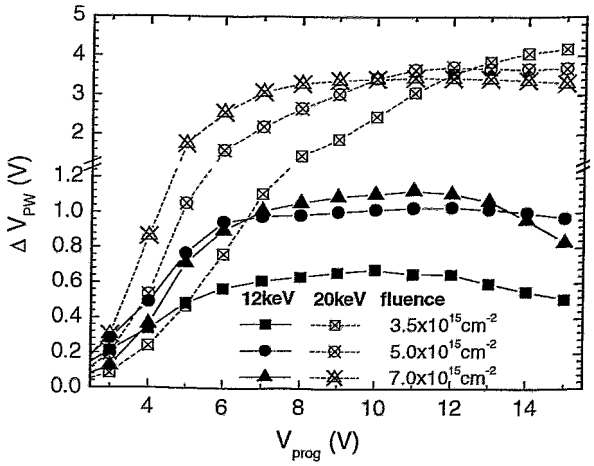


Fig. 5.29a:
Programming window ΔV_{PW} as a function of the programming voltage for Ge^+ implanted SiO_2 layers with a thickness of 20nm

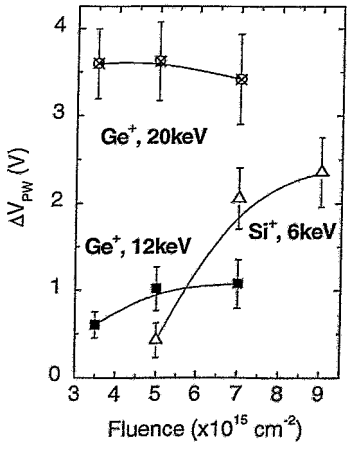


Fig. 5.29b:
ΔV_{PW} as a function of the ion fluence (pulses: ±12.5V, 100 ms)

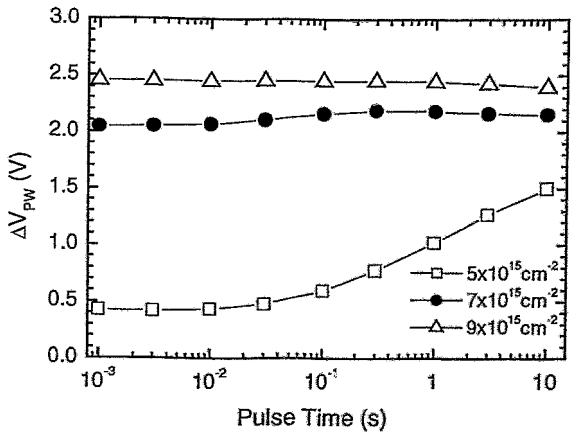


Fig. 5.30:
Programming window ΔV_{PW} of Si^+ implanted SiO_2 layers (20 nm) as a function of the programming pulse length. The applied voltage was ±12.5 V for each pulse.

An interesting parameter related to applications of nv-memories is the programming pulse duration. Fig. 5.30 shows the programming window of Si implanted oxide layers as a function of the pulse duration for a fixed stress voltage of ±12.5 V corresponding to an electric field of 6.25 $MVcm^{-1}$. The pulse length was varied between 1 ms and 10 s. SiO_2 layers implanted with a fluence of $5x10^{15}$ cm^{-2} show an increase in the window size from 0.45 V to 1.5 V, while samples containing a higher amount of Si do not show such a strong dependence on the pulse length.

5.5.1.2. Retention

For retention investigations the samples were charged by applying short positive or negative voltage pulses for writing or erasing, respectively. Subsequently CV measurements were carried out to determine the flatband voltage. Much attention has to be paid, because the influence of the CV measurement on the retention behavior is not negligible. The charging of the samples was performed with 100 ms pulses of 12.5 V, which corresponds to an electrical field of 6.25 $MVcm^{-1}$ for 20 nm thick SiO_2 films and storing the samples at elevated temperature (100°C ... 250°C) up to 1 week without any bias applied to the gate (Fig. 5.31).

For MOS capacitors implanted with Si^+ ions to fluences of $7x10^{15}$ cm^{-2} the programming window remains stable above 0.5 V even during thermal treatment at 250°C for 90h [Gebe01a]. This indicates a good retention behavior. Samples implanted with a higher fluence, however, show a remarkable decrease of the programming window size. The enhanced damage in the interface region leads to more defects influencing both, the conduction behavior and the trapping properties. Our previous investigations of Si-implanted SiO_2 layers showed a strong shift of the onset of a FN-like tunneling characteristic in the IV-curve towards lower electric fields with increasing Si fluence [Gebe00a]. This implies that the defects enhance the charge injection and transport through the oxide layer.

For the sake of comparison Fig. 5.32 gives an overview about the retention investigations of both, Si and Ge implanted SiO_2 layers. Since the size of the programming windows is different, the relative window size β, which is defined as $\Delta V_{PW}(t) / \Delta V_{PW}(t=0)$ is used. Data for the Ge implanted samples were obtained while storing them at room temperature. Si implanted layers did not show noticeable effects at RT and therefore the samples were stored at elevated temperature. The Ge implanted samples show a sharp drop in the programming window already at room temperature. With increasing fluence the retention behavior becomes worse. Especially the samples with the 12 keV implant exhibit only a very short retention of the order of 1000 s. Samples implanted with 20 keV Ge^+ ions show an improved retention behavior. This implies that the damage in the volume leads to a faster detrapping.

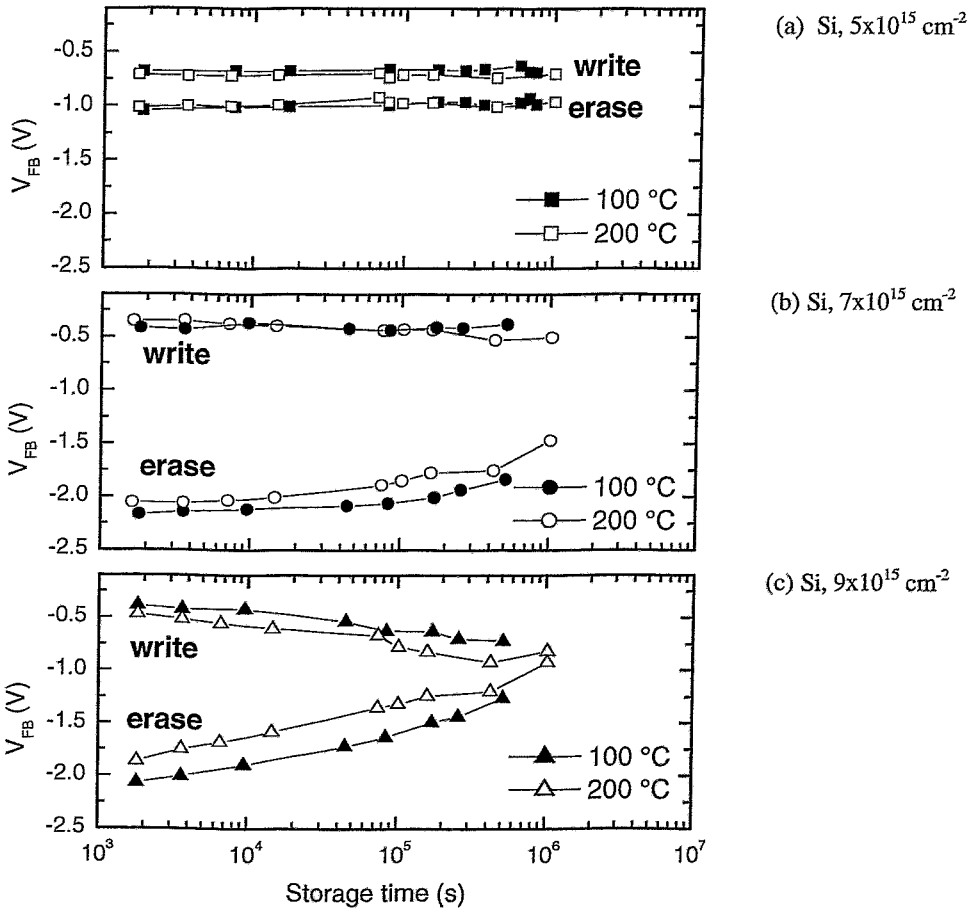


Fig. 5.31:
Retention characteristics of Si^+ implanted SiO_2 (20 nm). After writing or erasing of a device the V_{FB} values were measured as a function of storage time. The wafers were stored at 100 or 200°C and no bias was applied to the gate.

The retention characteristics were also investigated after charging with 10 ms pulses of 10 or 15 V, which corresponds to an electrical field of 5 $MVcm^{-1}$ for 20 or 30 nm thick SiO_2 films, respectively, and storing the samples at 150°C or 250°C up to 90 h without any bias applied to the gate. For MOS capacitors implanted with Si^+ ions to fluences of $7x10^{15}$ cm^{-2} the programming window remains stable above 0.5 V even after thermal treatment at 250°C for 90h. Samples implanted with the higher fluence however show a remarkable decrease of the programming window size. The enhanced damage in the interface region leads to more defects influencing both, the conduction behavior and also the trapping properties [Gebe00a].

In general the Ge-rich oxide layers exhibit only a poor retention behavior while the Si-rich layers show good retention even at high temperature storage. This means that the activation energy is distinctly higher. This may be an indication that for Si-rich layers the principal trapping mechanism is different from Ge-rich oxide layers, probably due to the higher stability of Si-related defects compared to that of the variety of Ge-related defects.

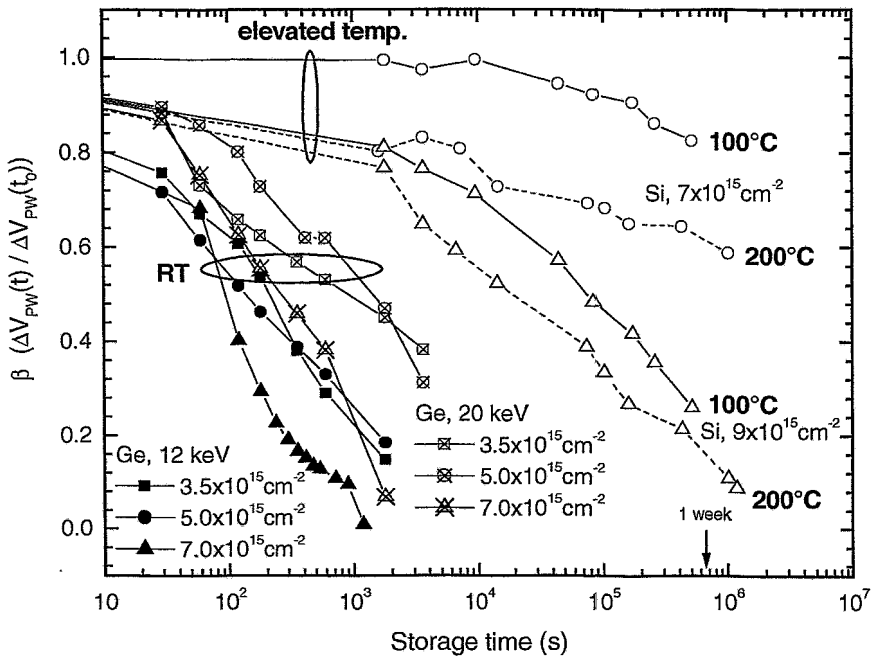


Fig. 5.32:
Retention behavior of Ge and Si implanted samples. The relative programming window size is plotted vs. the time. Ge implanted samples show already at room temperature a sharp drop in the programming window size while Si implanted layers show a long retention even at high temperature storage.

The IV investigations of Si implanted SiO_2 layers showed a strong shift of the onset of a FN - like tunneling characteristic in the IV - curve towards lower electric fields with increasing Si fluence [Gebe00a]. This implies that the defects enhance the charge injection and transport through the oxide layer. Taking into account the increase of the programming window size for higher Si or Ge concentrations (see Fig. 5.28 and 5.29 in section 5.5.1.1) the compromise in the choice of the implantation parameters becomes clear: high fluences are necessary to achieve sufficient sizes of the programming window (>0.5 V) but this will be always accompanied by a decrease in the device stability (see Fig. 5.5 in section 5.1.1) and a worse retention characteristic of the devices.

5.5.1.3. Endurance

One of the most important parameters of nv-memories is the endurance. It gives the information about the possible number of write/erase (W/E) cycles which can be carried out before the programming window is decreased below a size of 0.5 V or before the device breaks. In chapter 2 the typical values of endurance values from the literature are given. The results described here were obtained by using the pulse operation mode of the Keithley 237 SMU. Each cycle consists of a +12.5V pulse with a duration of 50 ms and a negative pulse of –12.5 V for 50 ms. After a defined number of stress-cycles the "final" state (W or E) was set, and then HF-CV measurements were carried out to obtain the flatband voltage V_{FB} for the specified operation mode (write or erase).

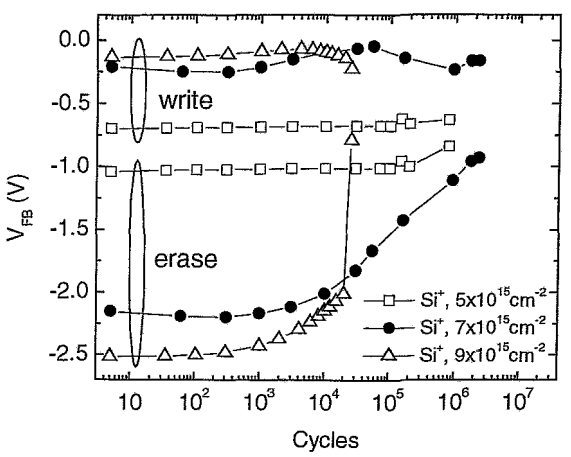


Fig. 5.33:
Endurance characteristics of 6 keV Si^+ implanted SiO_2 layers. Each cycle consists of a positive voltage pulse for the "write" and a negative pulse for the "erase" mode, respectively. Pulses were ±12.5V, 50 ms. After a defined number of cycles V_{FB} was measured by the CV method.

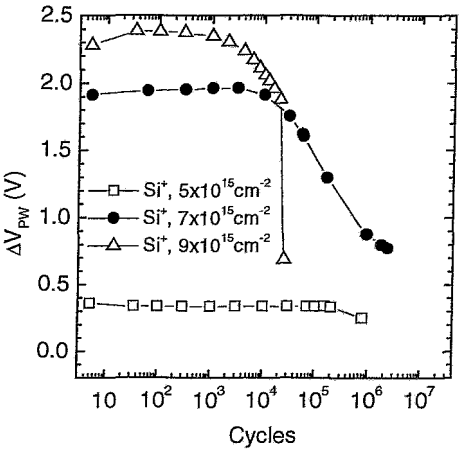


Fig. 5.34:
Programming window of 6 keV Si^+ implanted gate oxides, calculated from the flatband voltage shift after different numbers of cycles (Fig. 5.33). Best endurance results are achieved for a fluence of $7x10^{15}$ cm^{-2}.

Fig. 5.33 shows V_{FB} as a function of the number of cycles. Two characteristics belong to each of the investigated devices, obtained for the write and erase modes, respectively. The curve with the more positive V_{FB} characterizes the behavior after writing. For all samples it remains relatively constant with a slight decrease for higher pulse numbers. However, the negative part of the curve which is related to the erasing mode is only stable up to 1000 pulses and shows a strong increase. This implies that the detrapping of electrons cannot be performed as efficient as in the very first programming cycles. This leads to a closing of the programming window, which is displayed also in Fig. 5.34. For the highest Si fluence, maximum cycle numbers in the range of 10^5 were measured, whereas the samples with a fluence of $7x10^{15}cm^{-2}$ shows a much better endurance behavior. By extrapolation of the data one expects a programming window of more than 0.5 V even after 10^7 cycles.

In comparison to other works [Tiwa95] the endurance values we observed are smaller, but considering the short pulses (writing with 1µs, erasing with ms pulses) in that work the total stress on our devices was much higher. First tests with a shorter pulse duration (1 and 5 ms, respectively) showed an increase in the endurance, as expected. This gives the direct evidence that it is the total amount of injected charge, which limits the memory behavior.

5.5.2. Application of Si-rich oxides in memory cells

Single n-enhancement MOSFET transistors were prepared as a suitable test structure for a memory cell transistor. The threshold voltage V_T for transistors with unimplanted gate oxide is ~ 0.6 V (the ratio gate width/gate length W/L = 20 µm / 0.8 µm). Transistors with Si implanted gate oxide show a stable programming window of ΔV_T ~ 4 V for write/erase pulses of ±10 V / 50 ms (Fig. 5.35). The I_{DS}-V_{GS}-curve runs from the off-state to the on-state and back through the zero point. A current sensing window over nine decades is possible at room temperature. The sub-threshold leakage current is low, which is an indication for a good quality of the implanted gate oxide and the Si/SiO_2 interface.

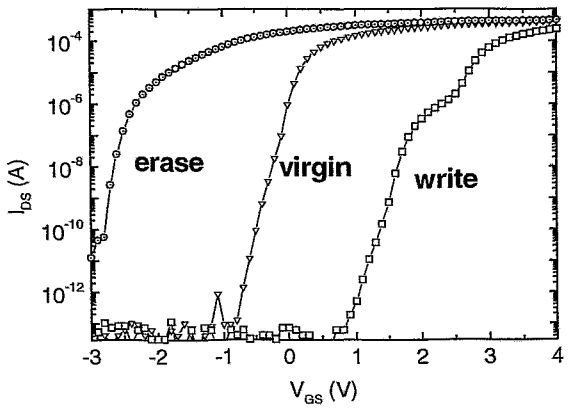


Fig. 5.35:
I_{DS} vs. V_{GS} for an n-channel transistor with implanted (Si, 6 keV; $5x10^{15}cm^{-2}$) gate oxide of 20 nm. The programming was performed with write/erase pulses of +/- 10 V for 50 ms.

Based on the promising results from MOS and single transistor elements, a first 256k-non-volatile Static Random Access Memory (nvSRAM) demonstrator with Si^+ implanted gate oxide was fabricated in cooperation with the ZMD AG Dresden. A nvSRAM has two separate modes of operation - an SRAM mode and a nonvolatile mode. In SRAM mode, the memory operates as an ordinary static Random Access Memory (RAM). In non-volatile operation, data are transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM. Two EEPROM-cells are incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent non-volatile data reside in EEPROM. Data transfer from the SRAM to the EEPROM cells ("store") or back ("recall") take place automatically upon power down or power up, respectively.

As a reference EEPROM configuration a SNOS (silicon-nitride-oxide-silicon)-transistor cell [Mina93, Steg98] made by a 24 nm nitride on a 2 nm tunnel oxide with a poly-Si gate was applied (Fig. 5.36, top). The devices were fabricated by the ZMD AG Dresden. In the modified technology the oxide-nitride stack was replaced by a Si^+ implanted (6 keV, 5...$9x10^{15}$ cm^{-2}) gate oxide of 20 nm thickness (Fig. 5.36, bottom). After rapid thermal annealing a 100 nm poly-Si layer was deposited as a gate contact. Following this ion-beam-synthesis module integration for nanocluster formation, the standard process for contact and metal formation was continued.

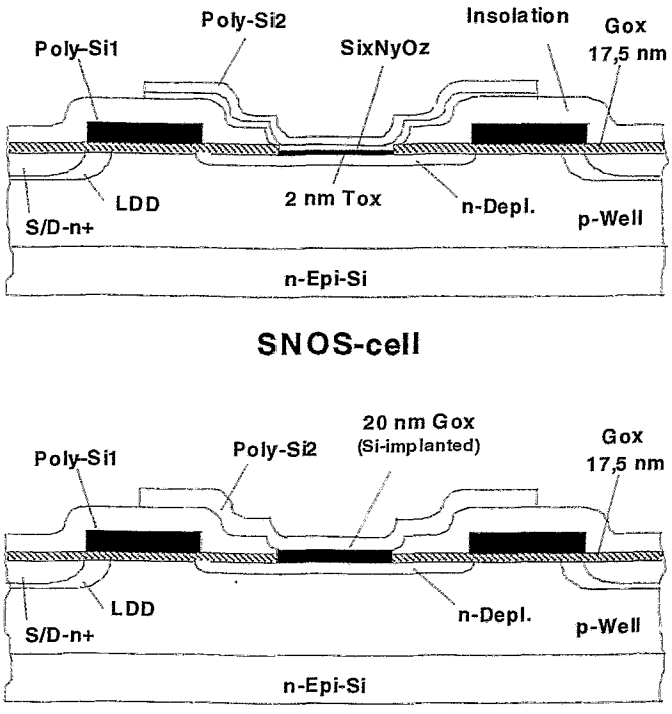


Fig. 5.36:
In the nanocluster memory cell the SNOS stack was replaced by an Si implanted gate oxide

Measurements with the standard wafer test program confirm the full functionality of the 256k-nvSRAMs. In addition, the programming properties of single memory cells of (1.7 μm x 1.4 μm) were investigated and compared with standard SNOS cells of the same size. Programming is typically performed by writing at +14.5V with 8 pulses of 160 μs duration and erasing at –12.5V with one pulse of 6 ms. The relatively high programming voltage (not really necessary for the NC-memory) was used to enable the standard ZMD measuring procedure for nv-SRAM and to have a direct comparison with standard. In Fig. 5.37 the threshold voltage as a function of V_{prog} is plotted for the NC-memory cell in comparison to the SNOS cell.

The achieved programming window of the NC-memory is smaller than that of the SNOS cell, but still >1V. The significant lower ΔV_{PW} value than observed for single transistor elements (see Fig. 5.35) is due to an additional process step. The standard nvSRAM preparation includes a 1050°C RTA forming gas treatment, which obviously leads to a hydrogen related saturation of the defects acting as trap. This influence on the NC-memory device is a further indication that not quantum confinement effects of nanoclusters, but cluster-related molecule-ike defects are responsible for the charge trapping.

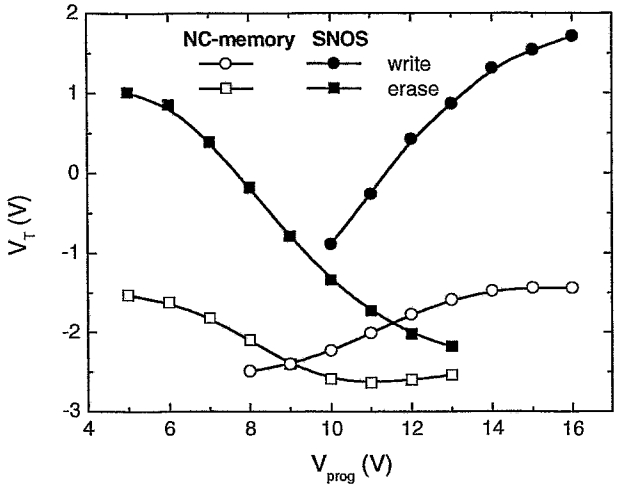


Fig. 5.37:
Threshold voltage V_T of the NC-memory cell (20 nm SiO_2, Si^+: 6 keV, $7x10^{15}cm^{-2}$ Si) in comparison to the reference SNOS cell.
Programming regime:
Write: + 14.5 V, 8 pulses, each 160 µs
Erase: - 12.5 V, 1 x 6 ms

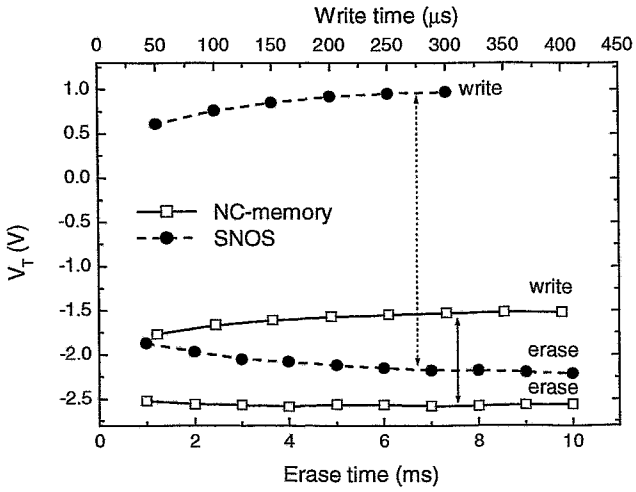


Fig. 5.38:
Threshold voltage of the NC-memory cell in comparison to the reference SNOS cell as a function of write / erase time. Single pulses were applied with voltages of +14.5V (write) and -12.5V (erase).

Fig. 5.38 shows the threshold voltage of the NC-memory cell as a function of write/erase time using single pulses. One can observe a very stable programming window, which is nearly independent of the time for both, write and erase pulses. This is in good agreement with the results measured on the MOS capacitors and promises high endurance values. Further investigations are in progress for the optimization of both, the structures and the operation mode.

Despite our promising results on devices based on Si-implanted SiO_2 layers numerous questions still remain open. So far, the nature of the charge-storage center and charging mechanism is not completely elucidated. It appears that the dominating process is not quantum confinement of the clusters, but trap-assisted charge-storage at cluster-related defect centers as also described by a few other authors [Hao93b, Shi98]. This would be similar to the well-known mechanism in Si-rich Si_3N_4, which is applied in the common SNOS memory technology [Mina93].

5.5.3. Comparison with Ar^+ - implanted SiO_2 layers

Ion-beam-induced defects influence both, microstructure and electrical properties. To check the influence of such defects on the charging properties, SiO_2 layers were implanted with Ar^+ ions to fluences causing similar damage profiles and comparable dpa-values at the Si/SiO_2 interface. Annealing was performed with parameters similar to the Si/Ge implanted devices for memory applications (RTA, 950°C, N_2 atmosphere, 30s). In TEM investigations no nanoclusters could be found in the Ar^+ implanted layers.

The IV-characteristics of Ar^+ implanted oxide layers are displayed in Fig. 5.39. IV-results from an unimplanted oxide layer are given as a reference. In the LFR and MFR the currents are slightly higher for the implanted layers, while in the HFR the curves are nearly identical. This means that the influence of the Ar implantation is much weaker compared to the cases of Ge or Si implantations which were discussed in section 5.1.1.

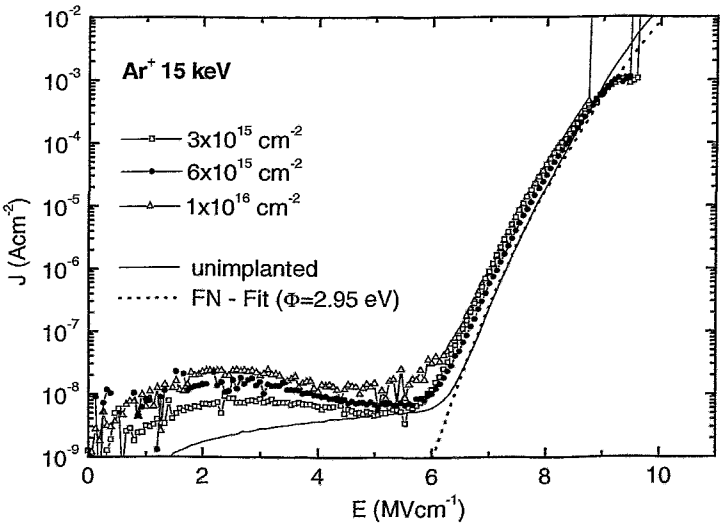


Fig. 5.39:
IV - characteristics of Ar implanted SiO_2 layers. Except for the low field region, no remarkable changes can be observed for the set of samples containing different amounts of Ar in comparison to the unimplanted reference. The J(E) characteristics can be fitted by the FN-model (Φ=2.95eV, m^*=0.4).

Fig. 5.40 shows the programming window after electrical stress with positive / negative voltage pulses (100 ms duration). In comparison to pure oxides which do not show programming effects, the Ar^+ implanted layers exhibit trapping of charge. The windows size shows a good correlation with the implanted ion fluence and reaches up to 0.9 V for a implanted fluence of $1x10^{16}$ cm^{-2}. During the investigations a strong decrease of the programming window was observed after performing several write / erase cycles. After only 10 write and erase cycles (+/-15V, corresponding to an electric field of E=5MVcm^{-1}) the decrease of ΔV_{PW} was 0.07 V, 0.10V and 0.15V for the implanted fluences of 3, 6 and $10x10^{15}$ cm^{-2}, respectively. For write and erase cycles using 20V (E=6.7MVcm^{-2}) the effect was even more pronounced. This implies that the trapping center might be related to an E' center. Some kind of field-annealing effects [Kaln90b] could lead to the decreasing window size during the programming cycles.

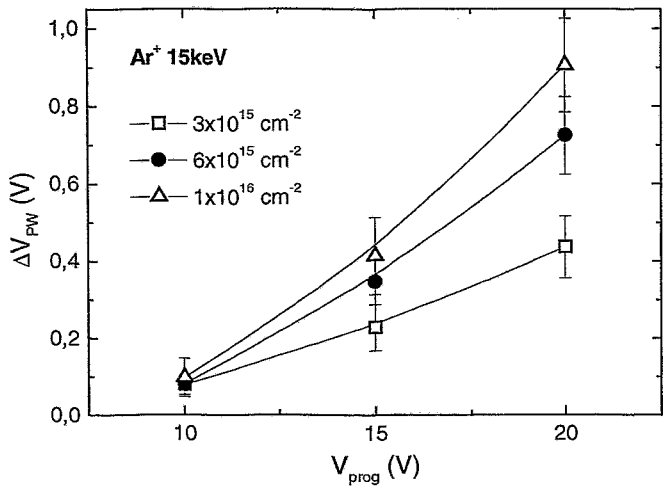


Fig. 5.40:
Programming window of Ar implanted SiO_2 layers (30 nm). The samples were annealed at 950°C for 30 s after the implantation. The windows size shows a good correlation with the implanted ion fluence.

PL investigations on the samples did not show any remarkable luminescence which is a further indication that not NOV but PL-inactive E' centers may be present. This and the investigated memory properties of Si^+ or Ge^+ implanted oxide layers lead to the assumption that for the formation of "stable" charge traps meeting the requirements for memory applications, not only implantation induced defects but also excess group IV atoms are necessary.

6. Luminescence Properties

6.1. Photoluminescence

6.1.1. PL spectra of ion beam synthesized Ge- and Sn-rich SiO_2 layers

PL from thermally grown SiO_2 layers can already be observed from defects caused by the fabrication process. However, the intensity of this PL in the visible and UV range is very weak. PL with a higher intensity can be obtained from SiO_2 layers with additional radiation damage, e.g. after ion implantation. Oxide layers implanted with Ar^+ ions show an enhanced PL in the UV range. However, after annealing at moderate temperatures this PL vanishes [Rebo99]. Contrary to that, oxide layers implanted with group IV elements like Si^+, Ge^+ or Sn^+ ions exhibit PL with an intensity of two to four orders of magnitude higher. After annealing the layers at high temperatures the PL intensity even increases, which implies that the defects caused by the ion implantation are transformed into other types of defects. This may lead to the reduction of defects with non-radiative transition characteristics or to a transformation of defects into luminescence centers, e.g. ODC.

In Fig. 6.1a the spectra of Ge^+ implanted SiO_2 layers (80 nm) with different Ge concentrations are displayed. A maximum peak is observed at an energy of 3.16 eV, corresponding to a wavelength of 392 nm. The PL was excited at an energy of 5.16 eV (240 nm). The spectra do not show any remarkable variation of the shape, but different peak heights for different Ge concentrations. The maximum intensity was achieved for the layer with 3% Ge with a peak slightly higher than that of the 6% Ge layer and about four times of that from the 1% Ge layer. A more detailed description of these concentration effects is given in section 6.1.4. SiO_2 layers with different sizes of nanoclusters in the TEM did not show any variation of the position of the violet PL peak. Furthermore, the blue-violet PL was also observed from implanted layers which did not exhibit clusters in the TEM at all. These observed effects imply that only defect related LC cause the PL. PL spectra (excitation at 4.96 eV) of Sn^+ implanted SiO_2 layers (Fig. 6.1b) display a similar shape with an additional shoulder at an energy of 3.3 eV. The spectrum can be fitted by two peaks where the peak at the lower energy (maximum at 3.15 eV) is dominant. Up to now it is not possible to give a clear statement about the type of defects causing the different peaks. They could be related to defects of a NOV type, namely ≡Si-Sn≡ or ≡Sn-Sn≡.

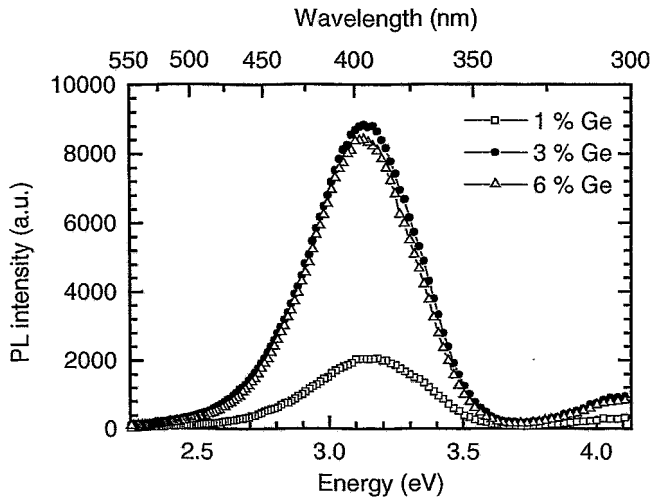


Fig. 6.1a:
PL spectra of Ge^+ implanted SiO_2 layers (thickness 80 nm, RTA 1000°C for 6 s)

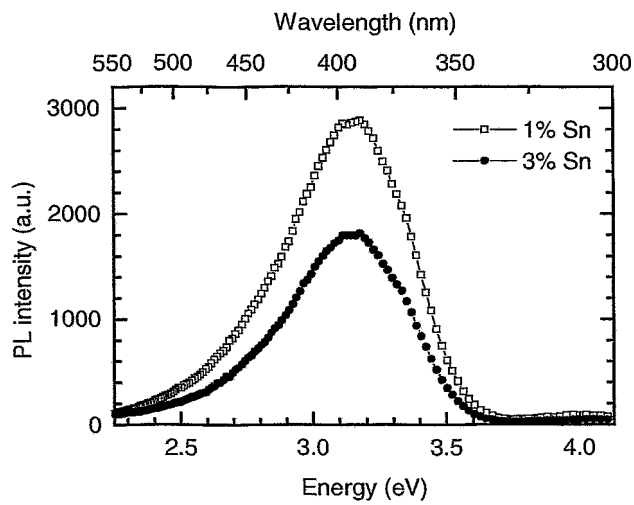


Fig. 6.1b:
PL spectra of Sn^+ implanted SiO_2 layers (thickness 100 nm, RTA 1000°C for 6 s)

6.1.2. PL spectra of Si- and C-rich SiO_2 layers

PL results of Si- and C- co-implanted oxide layers are given in Fig. 6.2. For the sake of comparison, the graph (a) shows the PL spectra of Si-implanted SiO_2 layers (thickness 500 nm) containing 4.5 % Si. In a previous investigation [Rebo00a] it was found that the blue PL around 2.7 eV of such layers is due to a triplet-singlet transition of a molecule-like ODC, either the NOV or the twofold coordinated Si atom. The blue PL peak was already accompanied by a much more intense UV peak at 4.4 eV and was excited by a photon energy around 5 eV. After annealing at 1100°C for 30 min, the blue PL vanished and an red-infrared PL peak around 1.6 eV emerged, which was attributed to Si nanoclusters. In contrast to this, neither a red-infrared nor a UV peak, but a blue PL peak at 2.7...2.8 eV and a yellow PL peak around 2.1 eV are observed in the PL spectra of Si^+- and C^+ - co-implanted SiO_2 layers (Fig. 6.2b).

Although the blue PL peak is excited by a photon energy of 4.7 eV, the origin of the blue PL seems to be different from that of Si-implanted SiO_2 layers as the UV peak is missing. The absence of a red-infrared PL peak indicates that there are no Si nanoclusters with a size in the order of 2...5 nm. Whereas the PL intensity around 2.1 eV remains nearly constant, the intensity of the 2.7 eV peak increases slightly with decreasing Si and C amount and is at the maximum for 5% Si and C.

As is well known, after Si implantation to sufficiently high fluences and subsequent furnace annealing at 1100°C Si nanoclusters should be formed [Rebo00a]. The following C implantation destroys these nanoclusters, and the presence of C seems to hamper the formation of pure Si clusters in the final annealing step, as no PL in the red and infrared spectral region was detected. Due to the small amount of C the formation of C-clusters is not likely. However, the C atoms should be bound to Si. So the nanostructures visible in the TEM are composed predominantly of Si, but contain enough C which introduces imperfections to the Si cluster and quenches the red-infrared PL.

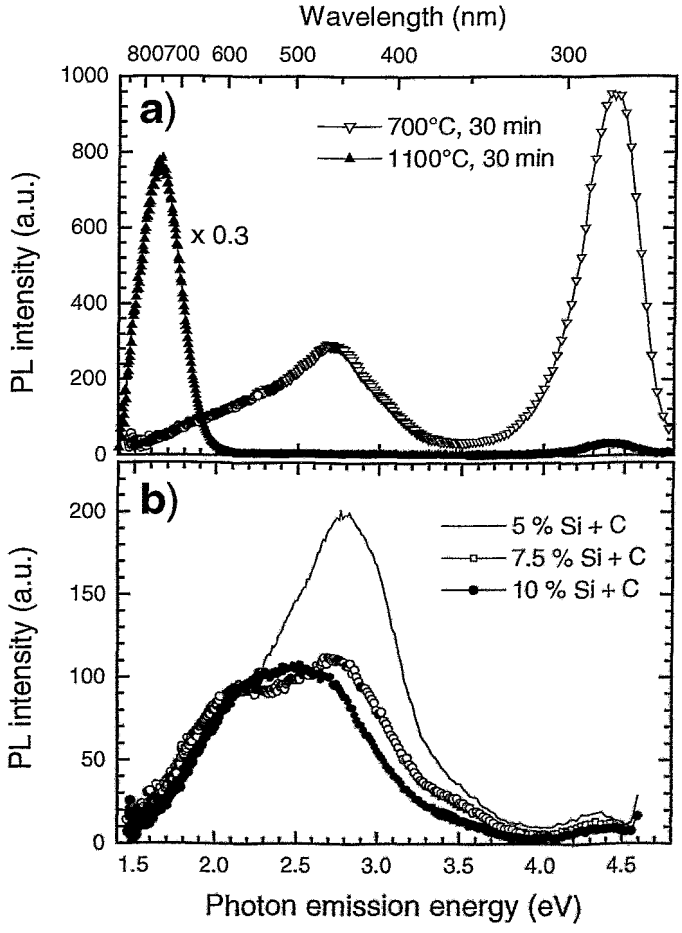


Fig.6.2a:
PL spectra of Si-implanted SiO_2 layers containing 4.5 % Si. The spectra were recorded using an excitation energy of 4.96 eV

Fig.6.2b:
PL from Si- and C-co-implanted SiO_2 layers. Annealing was performed between the Si and the C implants (1100°C, 30 min) and after the complete implantation at 800°C, 60 min + 1100°C, 60 min. The spectra were recorded using an excitation energy of 4.77 eV.

As already mentioned the blue PL peak at 2.7...2.8 eV probably has another origin than the PL peak at 2.7 eV from Si-implanted oxides because of the absence of the UV peak. Furthermore, the blue PL from Si-implanted SiO_2 films vanishes completely after annealing at 1100°C. Finally it was found in a very similar system [Zhao98] that the decay time of this peak is below the nanosecond range, which is definitely too fast for a triplet-singlet transition typically showing decay times in the microsecond range. Therefore the observed blue PL cannot be caused by the neutral oxygen vacancy or the twofold coordinated Si atom. The PLE spectra show relatively narrow excitation peaks and there is only a very small shift of peak positions with the concentration of C and Si, for which reason quantum confinement effects are unlikely. Nevertheless the PL could be caused by an oxygen deficiency center with more than two Si atoms. Based on the previous results the observed PL, at least in the blue spectral region, should be related to $Si_yC_{1-y}O_x$ complexes with $x<2$ and a high Si content. As a PL band at 2.1 eV was previously assigned to amorphous C clusters [Gonza00], such clusters may also cause the yellow PL in the case described here. However, no direct evidence for the existence of such C clusters was found during our microstructural investigations.

6.1.3. The mechanism of the PL – a short overview

The mechanism of the defect related luminescence is explained by the schematic drawing in Fig. 6.3. The energy level scheme of such a LC consists of a ground singlet state S_0, a first excited singlet state S_1 and a first excited triplet state T_1. The excitation $S_0 \rightarrow S_1$ is carried out with light of an energy of ≈5.1eV corresponding to a wavelength of ≈240 nm. This is followed by relaxation and a radiative transition back to S_0 or intersystem crossing to T_1 and a radiative transition back to S_0, which is observed as PL. The radiative transition $T_1 \rightarrow S_0$ is optically forbidden in first order and occurs only because of the spin-orbit coupling. The decay time of this transition is rather long and was estimated to be 100 µs and 7 µs for Ge and Sn, respectively [Rebo00b]. The observed high intensity of the $T_1 \rightarrow S_0$ transition is explained by the heavy-atom effect, which increases the spin orbit coupling if one Si atom of the LC is substituted by a heavier but isoelectronic Ge or Sn atom. The influence of spin orbit coupling leads to an enhancement of the radiative transition rate $T_1 \rightarrow S_0$. Evidence of the effect was demonstrated by comparing the PL results of Si-, Ge- and Sn-implanted oxide layers [Rebo99]. Furthermore intersystem crossing is a very efficient process leading to a much higher population of the T_1 state in comparison to the S_1 state.

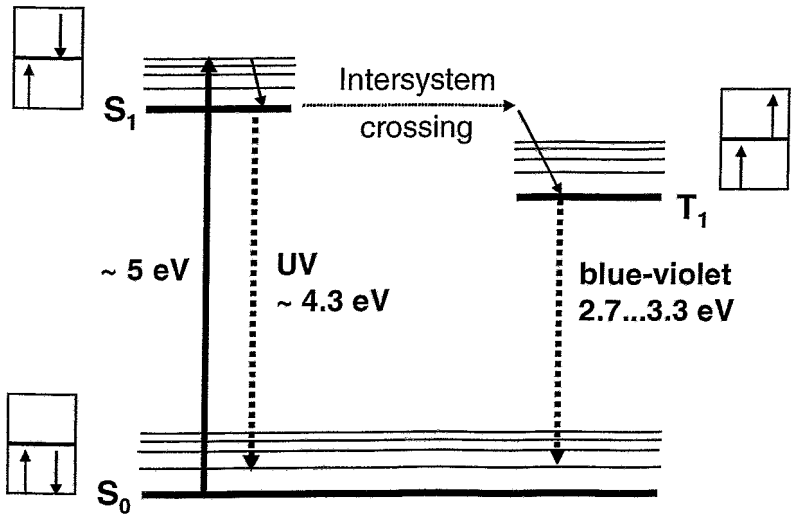


Fig. 6.3:
Energy level diagram of an ODC. After excitation from the ground singlet state S_0 to the first excited singlet state S_1 the LC emits light at 4.3eV and also in the blue-violet range. The latter process belongs to a $T_1 \rightarrow S_0$ transition, which is forbidden in first order.

6.1.4. The influence of implantation parameters and annealing conditions on the PL

This section is dedicated to the influence of the processing parameters on the PL. Since for the Ge rich SiO_2 layers no changes in the shape of the spectra were observed for the different implantation and annealing conditions the comparison is focused on the PL intensity. In order to compare the different measurements the maximum PL value was used to describe the PL intensity.

The influence of the implantation energy on the PL intensity of Ge implanted SiO_2 layers is shown in Fig. 6.4. For unimplanted thermally grown SiO_2 no detectable PL was observed (intensity below 0.1 a.u. in the scale of Fig. 6.4) which means that the measured PL intensity can fully be attributed to effects caused by the implanted Ge. In general the intensity increases with higher implantation energies.

The as-implanted layers show intensities of 260, 620 and 810 a.u. for Ge implants at energies of 30, 40 and 50 keV, respectively. After annealing the PL intensity increases by more than one order of magnitude. The fluences which were implanted to achieve similar maximum peak concentrations of 3 at% were 4.4, 5.5 and 6.5×10^{15} atoms/cm^2 for 30, 40 and 50 keV implants, respectively. However, the increase in the PL intensity cannot fully be explained by the increased amount of Ge caused by the different fluences. Another approach for the understanding of this behavior is the comparison of the dpa values as a measure for the oxide damage. As shown in Fig. 4.3b (section 4.1) the values increase with

the ion energy from maximum dpa values of 13.0, to 16.5 and finally 20.1 dpa. These numbers imply that the oxide structure is completely destroyed and a lot of defects are present. The region with high damage is also widened with increasing implantation energy as shown in the Fig. 4.3b. Therefore this is a further indication that for the formation of LC always the combination of two effects of the ion implantation have to be considered: first, the nuclear energy deposition and second, the overstochiometry of the additionally implanted ion species.

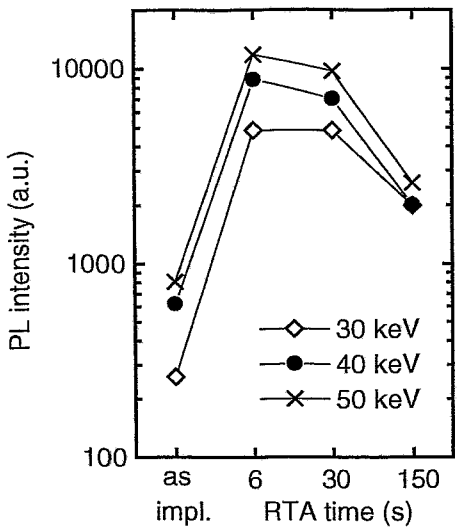


Fig. 6.4:
PL intensity of Ge^+ implanted SiO_2 layers (80 nm) for different annealing times and implantation energies. The maximum Ge peak concentration was 3%.

The PL intensity increases by more than one order of magnitude after RTA annealing (Fig. 6.4). Several processes have to be taken into account to explain this behavior. First, the thermal annealing leads to a diminution of non-radiative E' centers, which are known as precursors of the LC. This behavior was demonstrated by a combination of ESR and PL investigations [Liao96a]. Second, additional LC may be formed during the annealing process. Third, the amount of hydrogen introduced during the post-implantation sample treatment and storage conditions (even at clean room conditions) is strongly reduced during the high temperature treatment due to outdiffusion [Schm02]. This should lead to the decomposition of Ge_xO_yH like defects which might compete with the radiative LC.

After longer annealing times the PL intensity decreases. This can be explained by two effects. First, the LC may be dissolved and the diffusing Ge atoms form clusters. Second, one has to consider the decrease in the Ge content because of Ge outdiffusion for longer annealing times as it was shown in chapter 4, Fig. 4.7. Additionally, the diffusion of Ge towards the Si/SiO_2 interface may lead to a further reduction of radiative LC.
From the investigations carried out in this work one cannot directly distinguish between the different effects. However, the enhanced decrease of the PL intensity for longer annealing times in thin SiO_2 layers (see Fig. 6.5) is a strong indication that the outdiffusion of Ge is the dominating process. Thicker layers do not show such a strong influence of the annealing time.

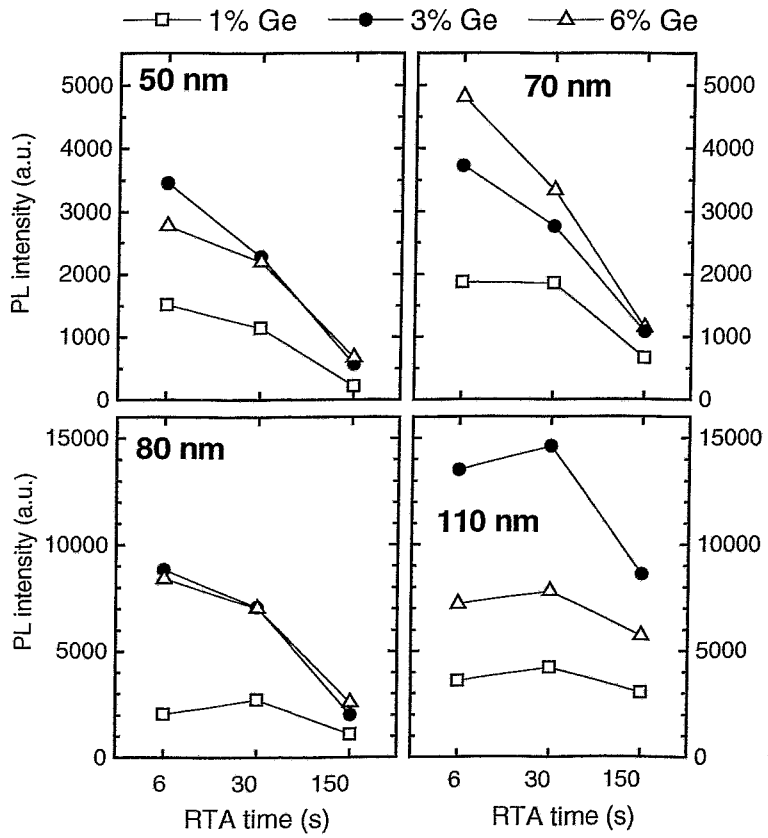


Fig. 6.5:
PL intensity of Ge^+ implanted SiO_2 layers after different annealing times. Please note that the scales for the intensity are different. The PL intensity increases with the layer thickness. A decrease of the intensity was observed for longer annealing times. This effect is most pronounced for thinner oxide layers.

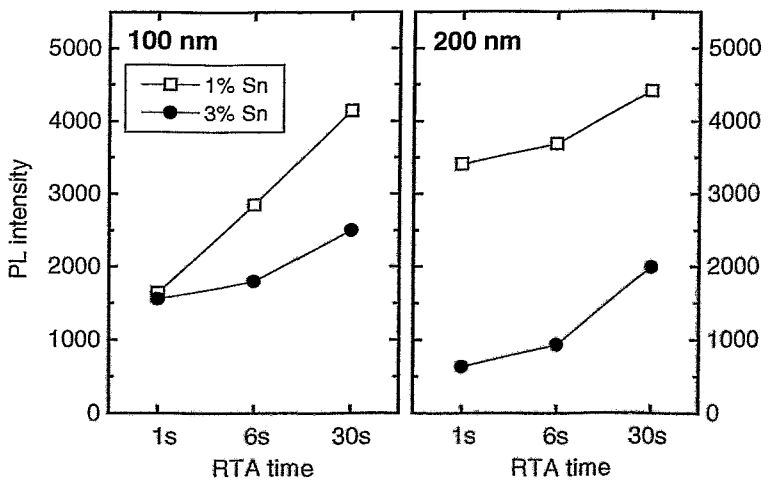


Fig. 6.6:
The PL intensity of Sn implanted oxide layers increases with annealing time (RTA, 1000°C). Layers containing 1% Sn show an enhanced PL intensity compared to samples with 3% Sn.

The PL intensity of Sn^+ implanted SiO_2 layers shows an increase with the RTA time (Fig. 6.6). Furthermore a higher intensity is observed for layers containing 1% Sn. Since the PL is also related to defects caused by the implantation of Sn this behavior leads to two conclusions: first, the annealing enhances the formation of LC from the defects initially produced by the ion implantation. Second, if the amount of Sn is increased, the formation of larger clusters occurs as described in section 4.2.3. Obviously these larger clusters can not form as many defects as a greater amount of smaller clusters does. Thus, for annealing times longer than 30 s the intensity of the PL should decrease again.

The PL results from Ge^+ and Sn^+ implanted SiO_2 layers lead to the following conclusions for the IBS method: the implanted ion fluence has to be chosen in such a way, that peak concentrations of about 3% for Ge and about 1% for Sn are achieved. For higher amounts of the implanted ion species the formation of nanoclusters is enhanced leading to a smaller amount of LC. The implantation energy plays also an important role, since implants close to the surface of the SiO_2 layer are strongly influenced by outdiffusion during the annealing. The annealing conditions have to be selected in such a way that the implantation induced defects are annealed, but the outdiffusion or the enhanced diffusion of the implanted ion species towards the interface is prevented. Also, the formation and the processes related to the Ostwald-ripening of clusters should be reduced in order to keep a sufficient number of radiative LCs.

6.2. Electroluminescence

6.2.1. EL from Ge-rich oxide layers

Fig. 6.7 displays the EL and PL spectrum of a 200 nm thick Ge-implanted SiO_2-layer containing 3% Ge after RTA for 30s. Both spectra show a peak at 3.18 eV (390 nm) and their shape is almost identical. Furthermore, the shape of the EL spectrum changes neither with the injection current (magnitude and polarity), nor with different anneal procedures, and the EL intensity shows a linear dependence on the injection current. This implies that the luminescence for both PL and EL is caused by the same luminescence center and that the deexcitation mechanism is identical [Rebo00a].

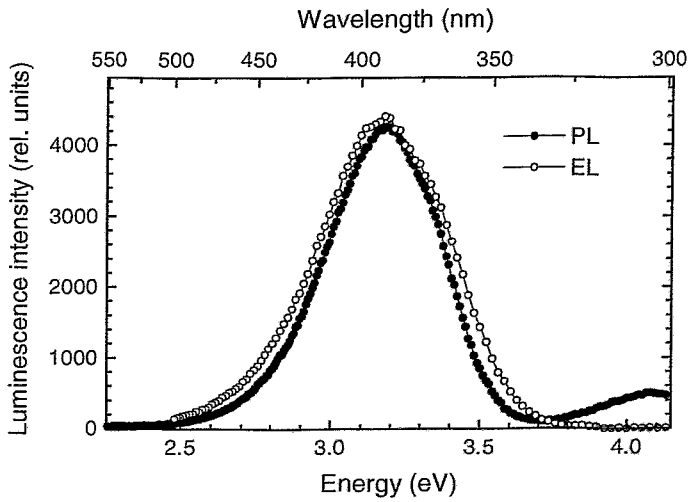


Fig. 6.7:
PL and EL spectra of a 200 nm SiO_2 layer containing 3 % Ge, annealed at 1000°C, 30 s. The spectra are normalized to the same peak value. Both curves are in good agreement, indicating that the same defect center is causing the luminescence.

The dependence of the optical output power on the electrical input power is displayed in Fig. 6.8 for EL devices with an oxide thickness between 130 and 500 nm. Every single data point in the graph represents one recorded EL spectrum. The devices were operated under forward bias in a constant current regime. The straight lines are plotted in the figure to guide the eye and represent different power efficiencies which are defined as the ratio between optical output and electrical input power. From the graph three tendencies can be seen: First, the slope of the optical output vs. electrical input power for each thickness is quite linear with a weak tendency towards lower efficiencies for higher input powers. Secondly, the EL efficiency increases with decreasing oxide thickness. A record efficiency value of 0.5% is achieved for samples with an oxide thickness of 130 nm. Thirdly, the maximum electrical input power which can be applied before breakdown of the oxide seems to lower with decreasing oxide thickness.

Up to now the dependence of the power efficiency on the oxide thickness cannot be explained in a satisfactory manner. One could argue that the reduced voltage for thinner oxides is the dominating effect for the increasing efficiency. Because of the similar electric

fields necessary for EL excitation for the same current one obtains different voltages depending on the oxide thickness and therefore a lower input power for thinner oxides. This lower input power causes a higher efficiency if we assume similar numbers of EL centers in the oxide layers. However, this fact cannot explain an increase of the efficiency of more than one order of magnitude if we compare 500 nm and 130 nm oxides. For devices with an oxide thickness <130 nm the trend of increasing EL efficiency does not persist. Since preparation-related problems become more and more dominant, larger fluctuations in the efficiency were observed. While samples with an oxide thickness between 80 and 100 nm show maximum efficiencies between 0.1 and 0.2%, thinner layers of 70 and 50 nm reach only values up to 0.1 and 0.04%, respectively. The stability of the devices is also reduced.

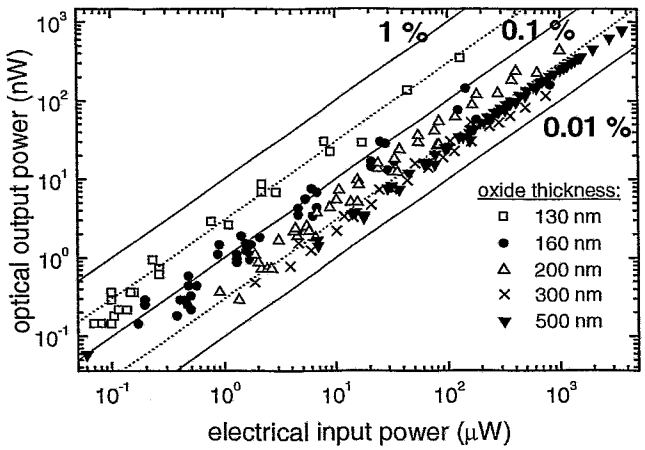


Fig. 6.8:
Optical output vs. electrical input power. Each data point represents one EL measurement.
Decreasing oxide thicknesses lead to higher power efficiencies. A maximum value of 0.5 % is observed for 130 nm SiO_2 layers.

One has to consider several aspects which influence this behavior. First, from the RBS results discussed in chapter 4, one can conclude that the loss of the originally implanted Ge should increase with decreasing oxide thickness because of the smaller distance between the R_p and the surface of the SiO_2 layer. This should lead to a smaller amount of Ge which is present at the interface. Second, it is known from nuclear reaction analysis (NRA) investigations that the region close to the surface contains a large amount of hydrogen [Schm02] which may also diminish the amount of LC. Third, the amount of Ge located too close to the interface becomes higher for small oxide thicknesses. As the electrons need a certain acceleration distance to gain enough kinetic energy, this will influence the energy distribution of the electrons and mainly the high energy tail of the distribution will be decreased. Fourth, one should also consider interference effects. A first phenomenological explanation helps to get an idea about the interference effects in our system: For PL the excitation depends mainly on the standing wave in the SiO_2 with the wavelength $\lambda_{ex}/2n$ (about 80 nm). If the distribution of the LC is broad enough (>40 nm), the difference between the maxima and the minima of the standing wave lead to an average value. However, for narrower distributions of the LC it becomes more important, whether they are located in the minimum or maximum of the standing wave. For the EL the situation is

different. The devices contain an additional layer, the ITO electrode. The transmission of this ITO layer is about 80%, so additional reflection and also absorption effects occur. Moreover, in the case of EL the excitation of the LC is more uniform than in the case of PL. However, since similar spectra for PL and EL were observed for different oxide thicknesses, interference effects do not appear to play a significant role in our experiments.

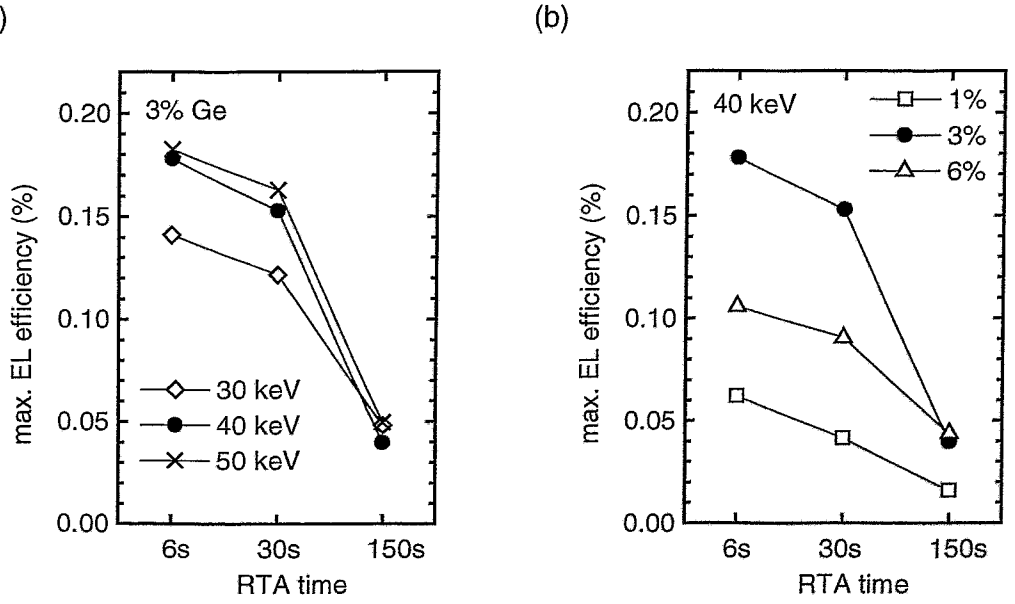


Fig. 6.9:
EL efficiency of Ge-rich 80 nm SiO_2 layers as a function of the annealing time (RTA, 1000°C). The devices were operated under forward bias at a constant current density of $5x10^{-5}$ Acm^{-2}. A strong decrease can be observed for longer RTA times. The left graph shows plots for different implantation energies (conc. 3 %), the right one the data for layers with different peak concentrations (energy 40 keV).

Fig. 6.9 shows the maximum EL efficiency as a function of the annealing time (RTA, 1000°C). The thickness of the oxide layer was 80 nm and the devices were operated under forward bias at a constant current density of $5x10^{-5}$ Acm^{-2}. With higher ion energies the power efficiency increases as shown in Fig. 6.9a. Hereby, only a small difference between the 40 and 50 keV implant was observed. Interestingly, the efficiencies for the layers with the 150 s RTA anneal are comparable.

The principal behavior showing a decrease of the efficiency with increasing annealing time is in good agreement with the results from the PL investigations (see Fig. 6.4 and 6.5). Since the LC causing the EL are the same which cause the PL, the explanation of this effect is similar as for the PL described in section 6.1.4. However, not only the microstructure of the LC (as for the PL) but also the electric properties of the layer have to be considered. Here two effects play a dominant role: The amount of defects which enhance TAT, PF or hopping conduction leads to an increase of the electric current in the MFR and in the HFR. The electric fields which are necessary to achieve a specific current density are reduced. This means that the amount of highly energetic electrons which are

necessary for the excitation of the EL decreases. Furthermore, not only the number of defects but also their position in the oxide layer with respect to the interface Si/SiO_2 should influence the probability of EL excitation events. If the LC are located too close to the IF, the distance is not large enough to accelerate the e^- to the energy which is required to excite the LC. On the other hand, if the position of the LC is too far from the interface other scattering events on non-radiative defects may occur before the LC rich region is reached by the electron.

The dependence of the efficiency on the electric input power is shown in Fig. 6.10 for SiO_2 layers with a thickness of 200 nm containing 0.3, 1.0 and 3.0 % of Germanium. The efficiency increases with higher Ge concentrations. A comparison between the 3% Ge and 1% Ge samples gives a factor of about 3 in the efficiency indicating that the number of the luminescence centers increases proportional to the Ge concentration assuming constant excitation cross sections. For 0.3% Ge however, large fluctuations occur and the measured values at lower input powers are comparable to the 1 % Ge samples. For higher input powers the oxide layer containing 0.3% Ge shows a bad stability.

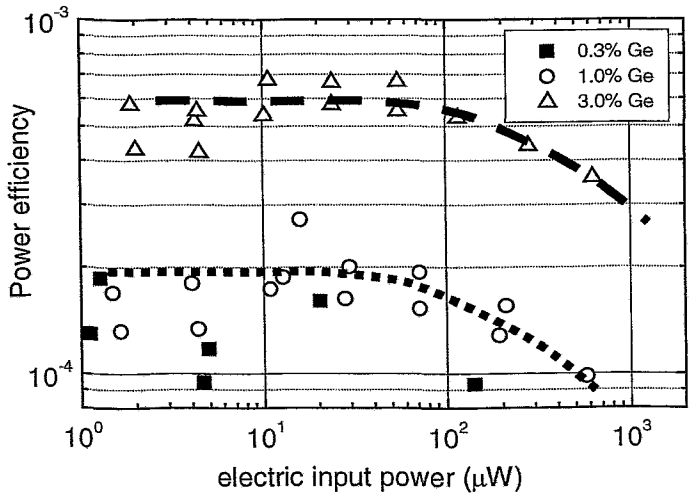


Fig. 6.10:
Power efficiency as a function of the electric input power for a 200 nm SiO_2 layer with different Ge concentrations. A decrease of the efficiency is observed for higher electrical input powers.

Reliability and long-term stability are among the strongest requirements in the market for every application of optoelectronic and microelectronic devices. A standard often used is the 10000 h operation guarantee, which is for instance relevant for all display applications [MelA00]. The investigation of the devices described in this work gives the charge to breakdown Q_{BD} as a measure for long-term stability. It describes the amount of charges which can be transported through the device before the breakdown occurs and it is determined by multiplying the device operation time (until breakdown) by the used constant current density. The normalized PL and EL intensity and Q_{BD} of Ge implanted SiO_2 layers with a thickness of 200 nm are given in Fig. 6.11. Both the PL and EL intensities show an increase with longer annealing times, which implies that either the excitation cross-section or the number of these luminescence centers increases during the

annealing process. It can also be seen that for longer RTA times the luminescence intensity begins to saturate for both PL and EL. This could be explained by the formation of LC from a "reservoir" of implantation induced defects during annealing.

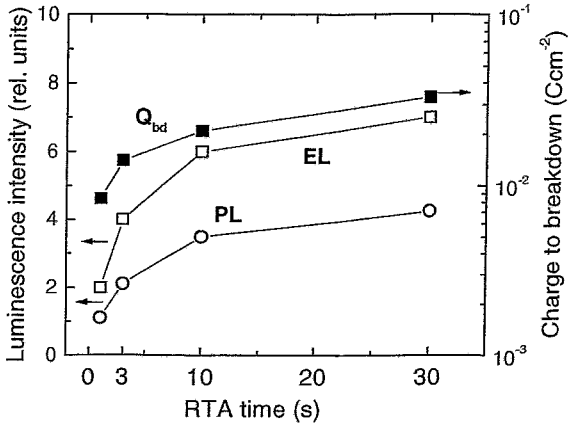


Fig. 6.11:
Luminescence intensity and Q_{BD} for 200 nm SiO_2 layers containing 3% of Ge. The annealing (RTA) was performed at 1000°C under N_2 ambient.

As depicted in Fig. 6.11, Q_{BD} also increases with annealing time, indicating that the amount of defects responsible for device breakdown decreases. The conversion of these defects into luminescence centers could be one reason for this. Since the most common defects caused by ion implantation are the E' center, the NBOH center and ODCs - the latter causing the luminescence - one possible mechanism for this conversion could be the transformation of E' centers into ODCs during annealing.

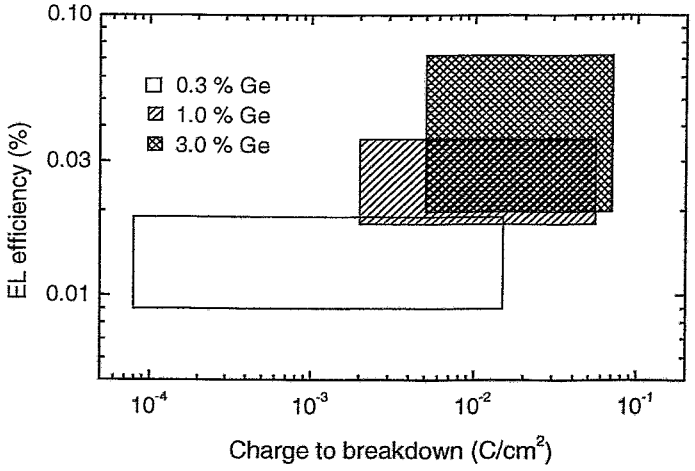


Fig. 6.12:
EL efficiency as a function of charge to breakdown for 200 nm thick, Ge-implanted SiO_2 layers. From the position of the rectangles it can be seen that the EL efficiency and the stability of the devices increases with Ge concentration.

Fig. 6.12 shows the efficiency and Q_{BD} in dependence on the Ge concentration of implanted SiO_2 layers with a thickness of 200 nm. Each device with a distinct Ge content and anneal procedure can be characterized by an average EL efficiency as well as a value for Q_{BD} and can be represented by one point. The different anneal variants for a fixed Ge

concentration accumulate in a region which is approximated by a rectangle. From the position of these rectangles it can be seen that the EL efficiency and the stability of the devices increases with Ge concentration. The increase in the device stability is in good agreement with the work of Lin et al. [Lin93]. The attempt to explain the increase of the EL efficiency faces the same problems as in the case of the thickness dependence. Assuming constant excitation cross sections, the number of luminescence centers increases with the Ge concentration. This leads to more scattering processes of the hot electrons and thus to a reduction of the energy of the hot electrons. So destructive impact ionization events which may lead to a device breakdown occur less frequently. However, for Ge concentrations higher than 3% one should expect a decrease in the EL efficiency as it was also observed in the case of 80 nm oxides (see Fig. 6.9b). Two effects should play a role in this process: first, the formation of clusters leading to a decrease in the number of LC and second, higher currents at lower electric fields which do not allow the device operation in the HFR. This means that the number of hot electrons which are necessary for the excitation of the EL is decreases.

6.2.2. EL from Sn-rich oxide layers

The EL from Sn rich oxide layers shows a different behavior in comparison to that from Ge rich layers. Fig. 6.13 compares the normalized PL spectra of Sn-implanted oxide with the corresponding EL spectra. All spectra show a main emission peak around 3.2 eV implying that the emission is caused by one and the same luminescence center. In the PL spectrum the shoulder in the high energy region (peak around 3.3 eV, see also Fig. 6.1b) is increased with the excitation energy. For both, PL and EL, the luminescence is accompanied by a shoulder on the low energy side. For PL, it increases for higher excitation energies as shown in Fig. 6.13a, while for EL it is present for low injection current densities (Fig. 6.13b). The shoulder disappears upon increasing the injection current density. A peak fit analysis using two Gaussian peaks reveal that the area fraction of the low-energy peak increases from 45 % for E_{ex}<5.06 eV up to 65 % for E_{ex}=5.39 eV in the case of PL. For EL, the area fraction of this shoulder decreases from 45 to 40 % with increasing current density.

To get a better understanding of this behavior, the PL excitation spectra of the different peaks will be discussed. For the PL of Sn^+ implanted SiO_2 a fixed excitation energy around 5.1 eV and fixed emission energies around 3.1 and 4.2 eV were reported [Rebo00a]. In an amorphous solid, especially in thermally grown SiO_2, there is a random distribution of bond angles, atomic distances, local chemical environments etc., which results in a random distribution of microstructures of the luminescence centers. This in turn leads to a distribution of excitation and emission energies, which is described by a Gaussian distribution only in a rough approximation. So the separation between the two observed luminescence peaks in Fig. 6.13a is possibly not too precise. However, the PL excitation spectra (Fig. 6.14) of these two PL peaks in Fig. 6.13a reveal that the emission at 3.2 eV is excited by the well-known excitation peak at 5.1 eV, whereas the emission at 2.6 eV shows a featureless PL excitation spectrum between 2.8 and 6.2 eV. The emission

at 2.6 eV is obviously caused by a different luminescence center. The specific microstructure of this LC is not clear. It could be similar to the structure of the NOV, the twofold coordinate Sn-atom or structures with more than one or two Sn atoms.

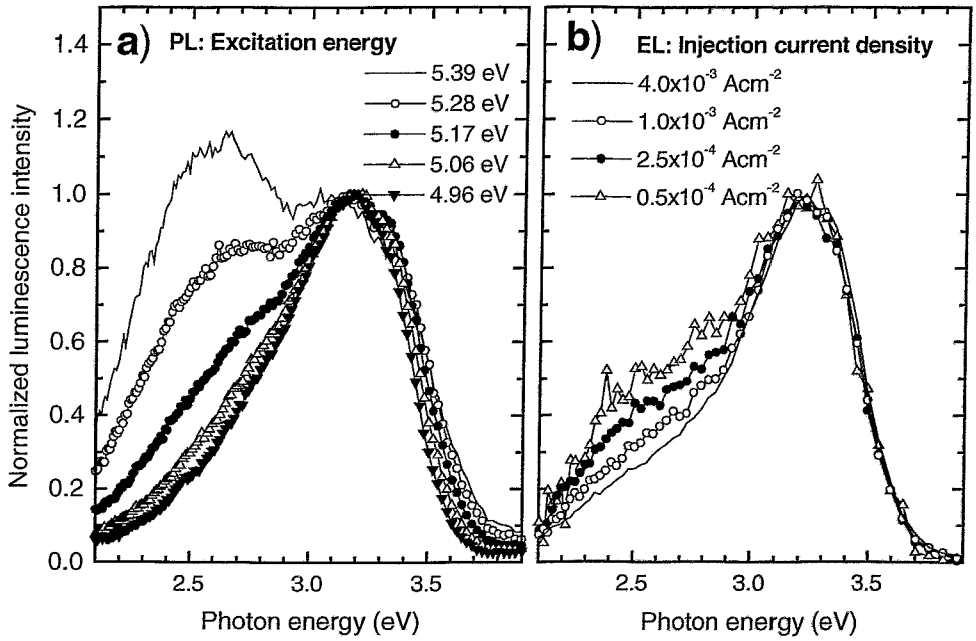


Fig. 6.13:
PL and EL spectra of Sn (1%) implanted 200 nm SiO_2 layers, annealed at 1000°C for 1s. The graphs are normalized for better comparison of the shape of the spectra. For PL the low energy peak increases with the excitation energy (a), while for the EL the low energy part decreases for higher excitation currents (b).

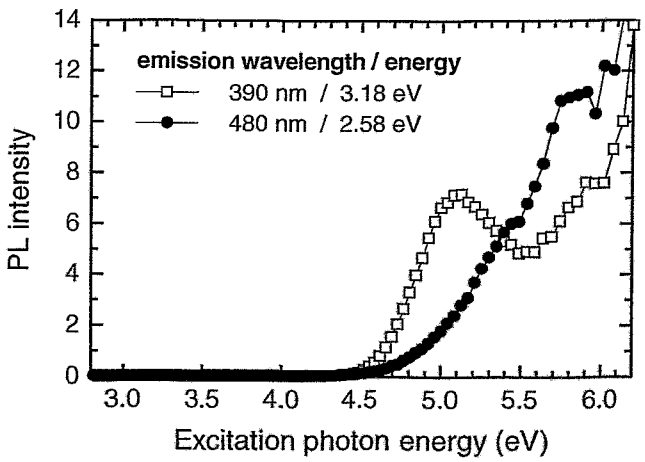


Fig. 6.14:
PL excitation spectra for the two PL peaks of a 200 nm SiO_2 layer implanted with 1% Sn.

From the results of the PL investigations one would in principle expect a similar behavior for the EL, namely an increase of the low-energy peak around 2.6 ... 2.8 eV for higher electric fields used for EL excitation. The increase of the high energetic tail of the

electron distribution [Arno94, Fisc85] should enhance the excitation of this low energy EL peak. However, exactly the opposite was found as displayed in Fig. 6.13b, where a slight decrease of the low-energy peak fraction was observed. One could argue that the differences in the excitation mechanism of PL and EL cause this behavior. In a more convincing explanation the number of LC causing this low energy luminescence is reduced during operation at high electric fields. From section 5.4.2 we know that due to impact ionization caused by hot electrons holes may be present in the oxide layer. The trapping of these holes in ODC or other defects may lead to changes in the microstructure of these defects. Thereby former LC may be transformed into non-radiative defects. Probably the LC causing the low-energy shoulder in the EL spectrum exhibit a higher capture cross section for holes than the LC causing the 3.15 eV luminescence. In order to clarify this behavior in more detail in the future, detailed electrical and additional microstructural investigations, e.g. ESR measurements, have to be carried out. For the electrical measurements it is essential to replace the EL devices containing ITO gate electrodes by MOS devices with Al contacts.

If one compares the EL results of Sn implanted oxide layers with Ge rich oxides, the following conclusion can be drawn. The EL of 200 nm thick Sn-implanted oxide layers is caused by at least two considerably different types of luminescence centers, whereas the EL spectrum of 200 nm thick Ge-implanted SiO_2 films seems to be dominated by only one type of Ge-related oxygen deficiency centers. Due to the larger atomic radius the integration of Sn atoms (1.51 Å [Schu67]) in the SiO_2 network is more difficult and causes more severe imperfections than the integration of Ge (atomic radius: 1.22 Å [Schu67]). This implies that the amorphous structure of the thermally grown SiO_2 with its random distribution of bond angles, atomic distances, local chemical environments etc., is even more disturbed than in the case of Ge, resulting in a broader distribution of different microstructures of the luminescence centers. This in turn leads to a broader distribution of excitation and emission energies, but cannot really explain the separation into two peaks in the case of Sn.

From TEM investigations it is known [Rebo00a] that the redistribution of the implanted ions and the formation of clusters are much faster in the case of Sn than in the case of Ge. To obtain an efficient light emitting device, a compromise between a high number of luminescence centers and a minimum number of imperfections vitiating the oxide quality and lifetime has to be found. As the change of the SiO_2 network is more severe for the integration of Sn it is assumed that the optimum for Sn-implanted oxides lies, in comparison to Ge-implanted SiO_2 films, at lower Sn concentrations and lower thermal budgets.

In the case of EL, the excitation mechanism is strongly linked to the injection and transport mechanism of charge carriers. As with our equipment the EL is not detectable for current densities below ~ $2x10^{-6}$ Acm^{-2}, it occurs only for fields higher than 6...7 $MVcm^{-1}$. If a sufficiently high electric field is applied, electrons can enter the oxide layer via FN-tunneling. In the case of implanted oxides, this tunneling will be assisted by traps close to the Si/SiO_2 interface, and the local electric field at the interface will be modified by a space-charge build-up in the oxide during injection. The existence of traps close to the injecting interface will result in an earlier onset of tunnel injection in Sn-implanted oxide

layers compared to the unimplanted oxide. It is also assumed that a higher incorporation of Sn leads to a higher trap concentration, which is why the tunnel injection in the case of 3 % Sn starts at lower fields than in the case of 1 % Sn.

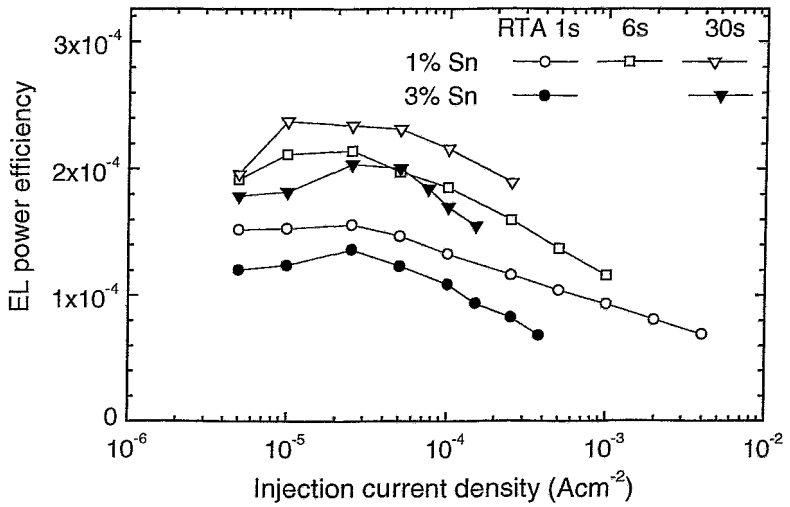


Fig. 6.15:
EL power efficiency of Sn^+ implanted 200 nm SiO_2 layers

Fig. 6.15 shows the EL power efficiency of the Sn^+ implanted devices plotted as a function of the injection current density. Every data point represents one measured EL spectrum. All measured power efficiencies are in the range between $0.5x10^{-4}$ and $2.5x10^{-4}$. The devices containing only 1% Sn are slightly more efficient than those containing 3% Sn. Furthermore, higher injection current densities can be applied to devices with 1% Sn until breakdown, which implies a higher electric stability. In contrast to the case of Ge-implanted oxide layers, the absolute EL intensity increases linearly with the injection current density only for current densities below ~ $5x10^{-5}$ Acm^{-2}. For higher current densities, the increase of the EL is sublinear, resulting in a smooth but continuous decline of the EL efficiency. This sublinear dependence can be well described with a power law: EL-intensity ~ $J^{0.8\pm0.1}$. The observed behavior might also be related to hot-electron impact processes leading to a transformation of former LC into other types of defects and starting degradation processes of the oxide.

6.2.3. EL from Si- and C- co-implanted SiO_2 layers

The EL spectra from Si and C co-implanted oxide layers are relatively broad and consist of several peaks (Fig. 6.16) which will be discussed in the following section. The devices were operated in a constant current regime at a current density of $2.5x10^{-4}$ Acm^{-2}.

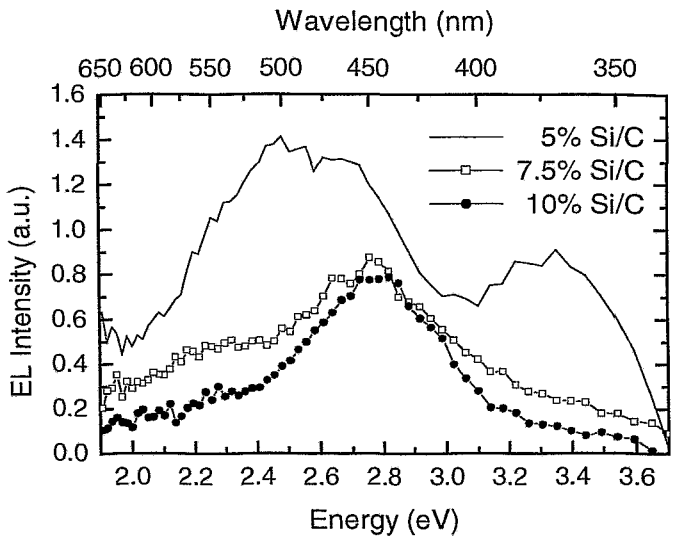


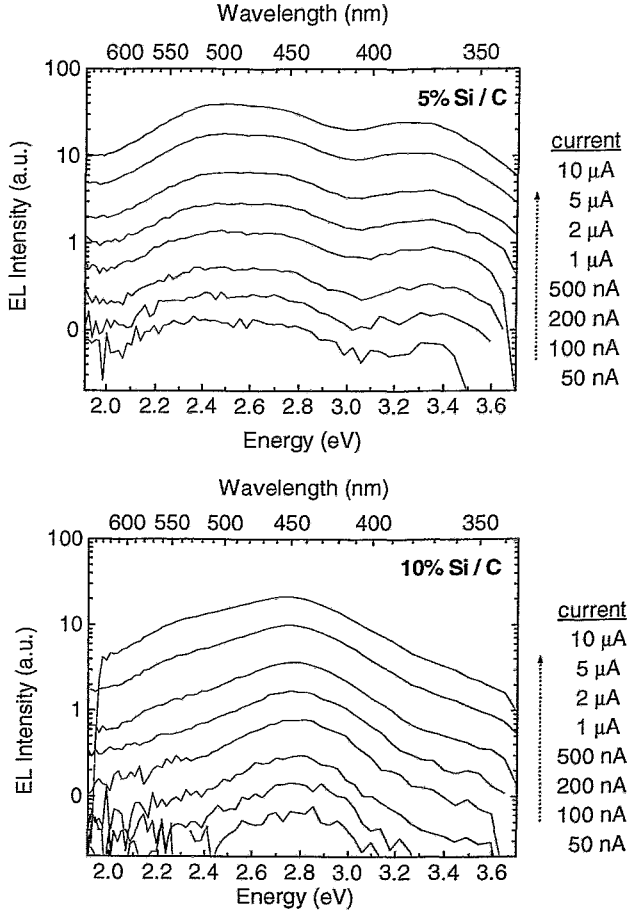
Fig. 6.16:
EL spectra of Si^+/ C^+ co-implanted SiO_2 layers. The used current density was $2.5x10^{-4}Acm^{-2}$.

For the lowest concentration (5%) a clear double-peak structure is observed. The two maxima are around 3.3 eV and 2.45 eV. The latter maximum belongs to a relatively broad peak which may consist of several sub-peaks. In the PL spectra (see Fig. 6.2b in section 6.1.2) the 2.7 eV peak was dominating but the asymmetry in the peak with a shoulder in the low energy region give also a hint to for peaks between 2.1 and 2.5 eV. However, it is interesting to note that those peaks dominate the EL spectra while the peak at 2.7 eV is reduced. The EL peak around 3.3 eV is non visible in the PL spectrum. Obviously the electrical excitation of these original sub-peaks of the PL spectrum is more efficient.

For the concentrations of 7.5 and 10% only one peak at 2.75 eV occurs. Additionally, sub-peaks in the shoulders are observed around 2.3 and 3.4 eV. These sub-peaks decrease for higher concentrations while the 2.75 eV peak remains stable. The shape of the spectra is somewhat different from that of the PL (see Fig. 6.2b in section 6.1.2), where a broad peak ranging from about 2.1...3.0 eV was observed. However, the typical characteristics showing a decrease of the high energy tail (3.0 ... 3.6 eV) for higher Si/C concentrations is similar for both, PL and EL.

Additional measurements were carried out in order to investigate the influence of the injection current density on the shape of the EL spectrum (Fig. 6.17). Panel (a) shows the case for 5% and (b) for 10% of Si/C concentration. Basically one can say that no remarkable changes in the spectrum occur with increasing current density and therefore also with increasing electric field. This means that the difference in the shape of the spectra

for the different Si/C concentrations is only related to the different microstructure and not to the distribution of hot electrons. It has also to be mentioned that the Si/C rich oxide layers showed an improved stability compared to the Ge or Sn implanted devices. This may be caused by the different types of defects capturing hot electrons during the high field operation.



(a) ... 5% Si / C

(b) ... 10% Si / C

Fig. 6.17:
EL spectra of Si^+/ C^+ co-implanted SiO_2 layers operated at different currents (dot area: 0.2 mm^2).

The power efficiency of Si/C co-implanted SiO_2 layers is depicted in Fig. 6.18. The solid symbols belong to the samples implanted to concentrations of 5%, the open and the crossed symbols to 7.5 and 10%, respectively. Different shapes of the symbols are symbolizing samples with different annealing times. No remarkable difference was observed with respect to the different tempering procedures, but one can clearly see an increase of the power efficiency with decreasing Si / C concentration. One reason might be the enhancement of non-radiative transitions with increasing Si / C concentration or the transformation of defects acting as LC into clusters. From the layers investigated here one should expect a further increase of the efficiency for even smaller concentrations. This could also be related to the results from Ge or Sn implanted layers, where optimum conditions were found in a concentration range of 1...3%.

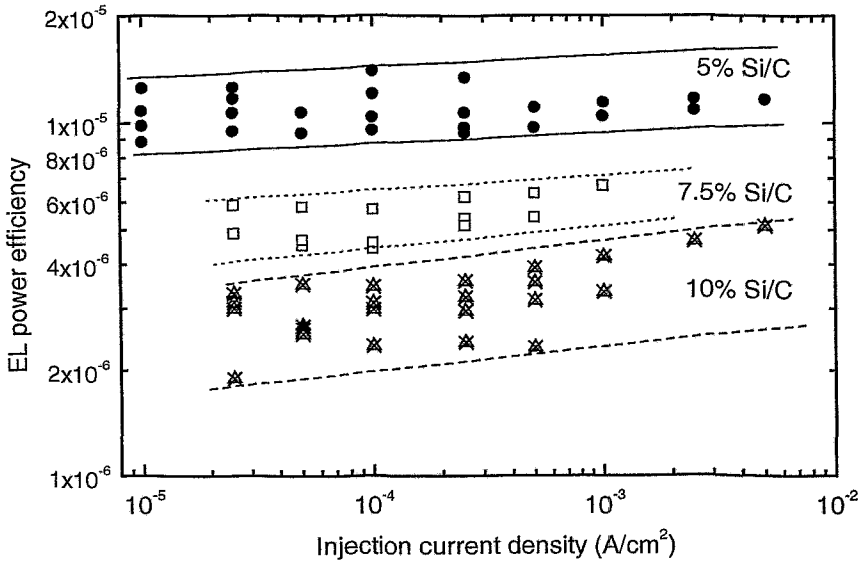


Fig. 6.18:
EL - power efficiency of Si^+ and C^+ coimplanted 360 nm SiO_2 layers. The data represent measurements on different devices for each sample.

6.2.4. The excitation mechanism of the EL

6.2.4.1. Correlation between EL and electrical properties

The understanding of the luminescence mechanism is of great importance for the optimization of the EL devices. Since the devices are operated at very high electric fields close to breakdown, the device degradation and the stability become the major issues for the device performance. IV measurements have been carried out in combination with EL investigations. Since the spectra do not change for different excitation fields in the case of Ge implanted samples, the EL intensity can be characterized by the height of the main emission peak at 390 nm. Fig. 6.19a shows the EL intensity in arbitrary units as a function of the applied electric field for Ge^+ implanted 80 nm thick SiO_2 layers. The background was estimated to be 5 a.u.. For each energy the plots of the three different annealing procedures are shown. The onset of the EL appears to be independent on both the implantation energy and the annealing conditions. This implies that the electric field has to reach a critical level before the onset of the EL occurs. It has to be mentioned that the background signal and the noise which was at a constant level up to the observed onset do not allow a clear statement for lower electric fields. But obviously after passing the onset level hot electrons with energies sufficient for impact excitation are present.

In the HFR with E >9.5 $MVcm^{-1}$ the curves show differences. With increasing annealing time higher EL intensities at the same electric field are achieved. This can be explained by the IV characteristics described in chapter 4, which showed a shift of the IV

curves towards lower electrical fields with increasing annealing time. This means that more electrons are injected leading to a higher EL intensity. In Fig. 6.19b the EL intensity is plotted as a function of the current density. Regarding the annealing times, no remarkable differences can be observed between the 6 s and 30 s RTA treated samples. However, the 150 s RTA treatment leads to a decrease of the EL intensity and higher currents have to be applied. This is even better visible in Fig. 6.19c, where the ratio of the EL intensity divided by the current density is plotted versus the electric field. The characteristics show changes in the slope at electric fields between 9.5 .. 10.5 $MVcm^{-1}$ (a) or in a corresponding way at a current density of $3x10^{-5}$ Acm^{-2} (b). This effect is more clearly visible in plot (c) where a clear peak of the efficiency can be observed. The position of this peak shifts towards lower electric fields with increasing annealing time but with increasing implantation energy towards higher electric fields. One can also see that the maximum efficiency increases with the implantation energy.

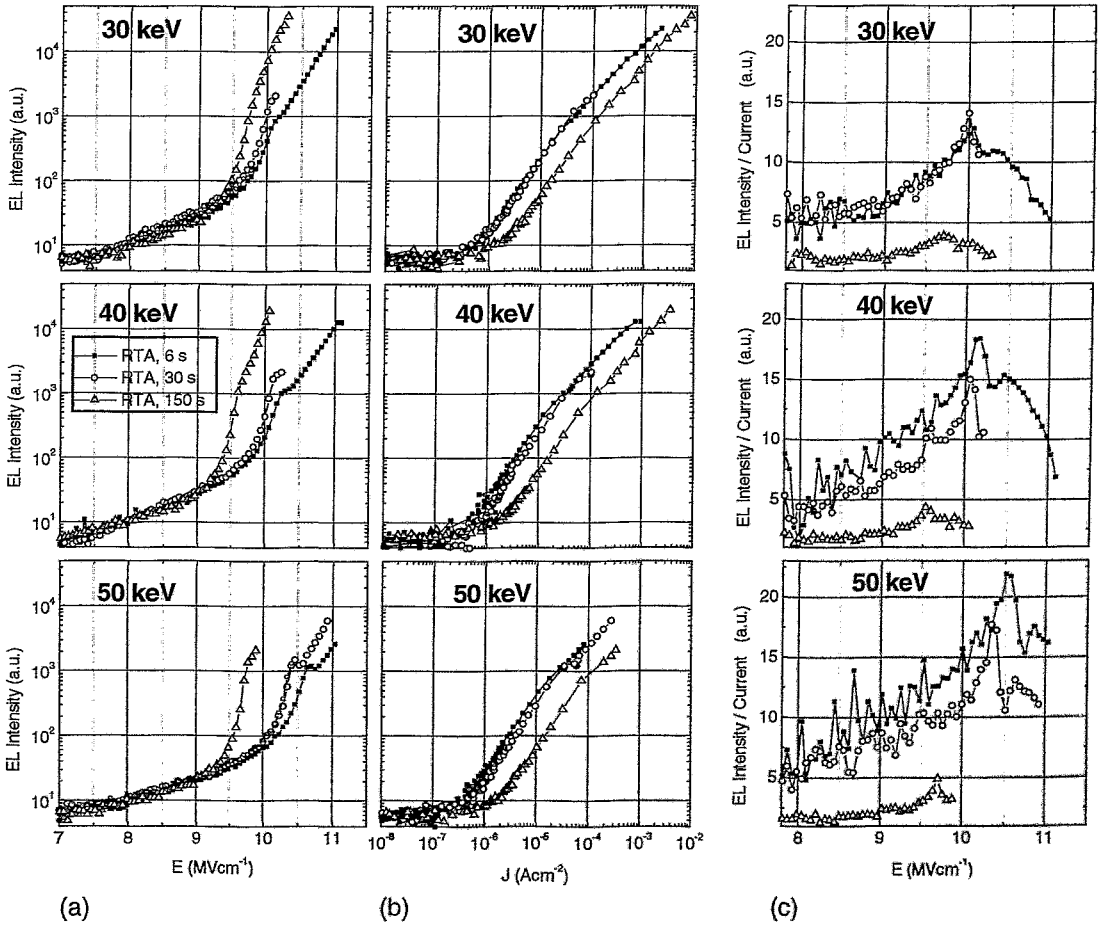


Fig. 6.19: Combined IV and EL measurements on 80 nm thick SiO_2 layers implanted with Ge^+ ions at various energies. The column (a) shows the EL intensity as a function of the applied electric field, (b) on the injection current density. On the right hand side (c) the EL intensity divided by the current is plotted in arbitrary units as a measure of EL efficiency. This value increases with the implantation energy.

6.2.4.2. Injection and conduction mechanism

As already stated before, the good correspondence between the PL and EL spectrum implies that in both cases the luminescence is caused by the same LC, and that the radiative deexcitation is identical. However, in the case of EL the excitation of the LC to the T_1 state is more complex. Electrons have to be injected into the oxide, they have to be transported through the oxide, and finally an interaction between the electrons and the LCs must take place in order to excite the LCs. The basic processes occurring during electron injection, electron transport and EL excitation are schematically drawn in Fig. 6.20. In the case of the pure oxide and high electric fields electrons can be injected into the oxide layer via Fowler Nordheim tunneling (process 1). The implantation creates defects in the oxide layer which appear as electron traps in the band gap of the SiO_2. Higher implantation doses will cause higher trap concentrations, and for very high doses the formation of Ge or Sn nanoclusters is possible. Traps and nanoclusters located close to the injecting interface can support the injection by trap-assisted tunneling (process 2) or by direct tunneling from the conduction band of the Si substrate to the nanoclusters (process 3). As a result, the electric field, where tunnel injection starts, decreases with increasing trap concentration and the I-V characteristics shift to lower applied electric fields with increasing Ge or Sn concentration.

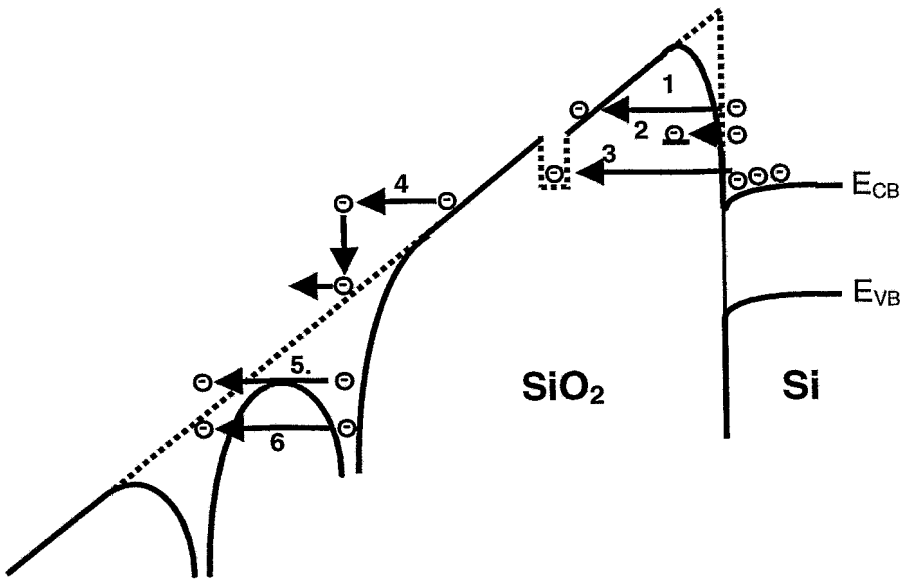


Fig. 6.20:
Injection and conduction processes in SiO_2. (1) Fowler-Nordheim (FN) tunneling, (2) direct tunneling into traps, (3) trap-assisted tunneling (TAT), (4) quasi-free movement in the SiO_2 conduction band, (5) Poole-Frenkel conduction, (6) Hopping conduction

One mechanism to describe the charge carrier transport is the quasi-free movement of electrons within the conduction band of SiO_2 (process 4). In equilibrium the electrons can be characterized by a energy distribution depending on the position in the oxide layer. In

the case of unimplanted SiO_2 films the energy distribution of the electrons is mainly determined by phonon scattering and it was shown that, under high field conditions ($\geq$ 5 $MVcm^{-1}$), even the average electron energy can reach a value of 3...5 eV [Arno94, Fisc85]. Adapting these findings to the case of implanted oxide, we expect a slight reduction of the electron energies due to the additional scattering at implantation-induced defects. Electrons having a sufficiently high energy can be scattered at luminescence centers being in the ground state S_0, and the transferred energy is used to excite the luminescence centers to a intermediate state i.

Another possibility is the charge carrier transport via traps by Poole-Frenkel conduction (process 5) or hopping conduction (process 6). In this scenario luminescence centers will be ionized by the high applied electric field, which can be regarded as an excitation from the ground state S_0 to an „ionized state''. The electrons move toward the metal electrode and leave the luminescence centers positively charged. If these centers trap an electron, they can relax – in most cases – back to the ground state. However, with a certain probability the centers can relax to the T_1 state, too. Both excitation mechanisms are schematically drawn on the right side of Fig. 6.23.

6.2.4.3. Time resolved EL measurements

For time resolved EL measurements the setup described in section 3.4.2 was used. Fig. 6.21 shows the applied voltage composed of a 150 V constant voltage and a 9 ms long voltage pulse with an amplitude of 30 V. The rise and decay time of the pulse is about 3 µs.

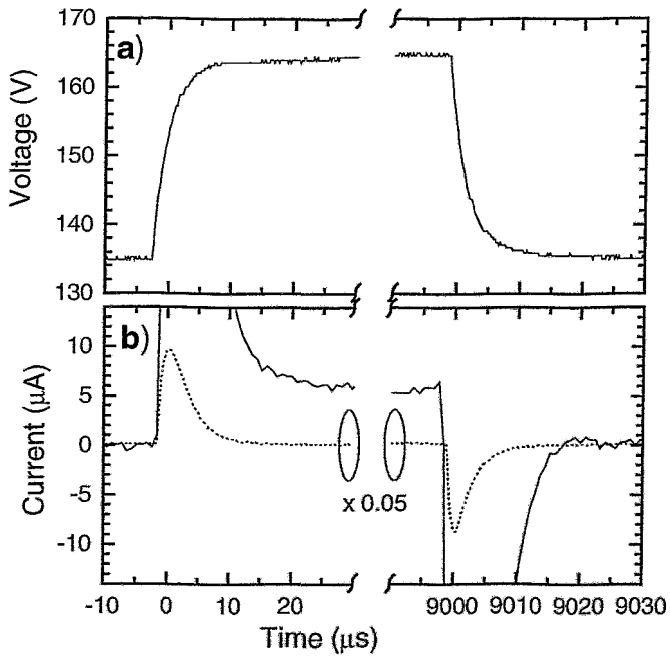


Fig. 6.21:
For time resolved EL investigation a 9 ms voltage pulse was applied to the gate contact (see also Fig. 6.22, where the full pulse is given). During switching a current spike with a time constant of 3µs is observed. This spike is caused by the capacity of the MOS structure. In panel (a) and (b) the voltage and the current are displayed, respectively. Note, that the dotted line in panel (b) is just the current multiplied by 0.05 in order to give an impression of the shape of the total spike.

The capacity of the MOS device differentiates the edges of the voltage pulse and causes a current spike with an amplitude of 200 μA and a time constant of again 3 μs (Fig. 6.21b). Apart from these spikes the tunnel resistance of the MOS device leads to a rectangular current pulse with an amplitude of 6..7 μA which really passes the oxide layer. This current flow causes the EL whose rising and falling edge is shown in Fig. 6.22 in comparison with the edges of the corresponding voltage and current pulse. For both the rise and decay time of EL a value of about 100 μs was estimated. In contrast to Fig. 6.21 the different time scale of Fig. 6.22 has to be noticed.

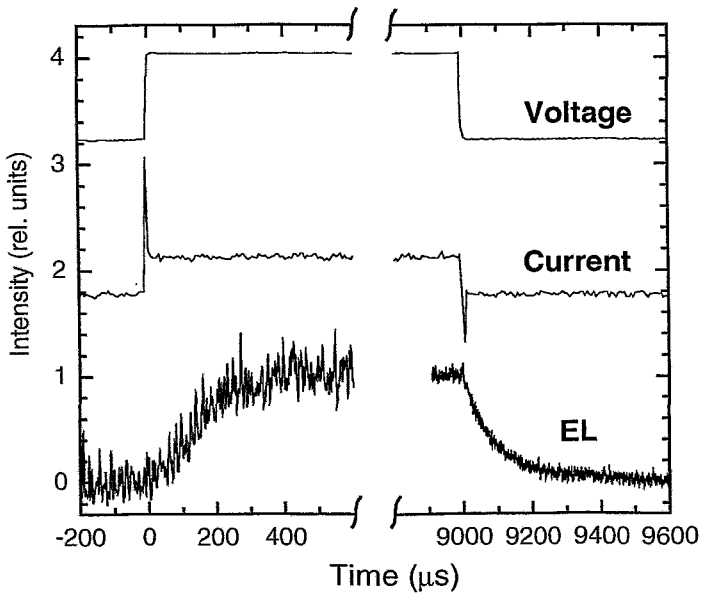


Fig. 6.22:
Transients of voltage, current and EL intensity. A 9 ms voltage pulse was applied to the gate contact.

The observed decay time agrees very well with the decay times known from the PL of these structures [Rebo00a]. In the literature time resolved EL measurements from Si implanted SiO_2 layers (produced in a sol-gel technology) were reported [Lute00]. This group observed a decay time of 8μs for EL and 2 μs for PL. The current pulse used for excitation of the EL had a rectangular shape and the current rise time was determined to be smaller than 0.1 μs which is in contradiction to our results. However, the EL observed in their work occurs in the red spectral range and is attributed to Si-nc and not to defects. Since the EL is observed only in small spots and not over the whole device area like in our case one can also explain the different rise time behavior. In our case the capacitance of the MOS devices causes the 3μs time constant as shown in Fig. 6.21, while in [Lute00] the tiny spots do not show high capacities giving such strong influences on the voltage pulse.

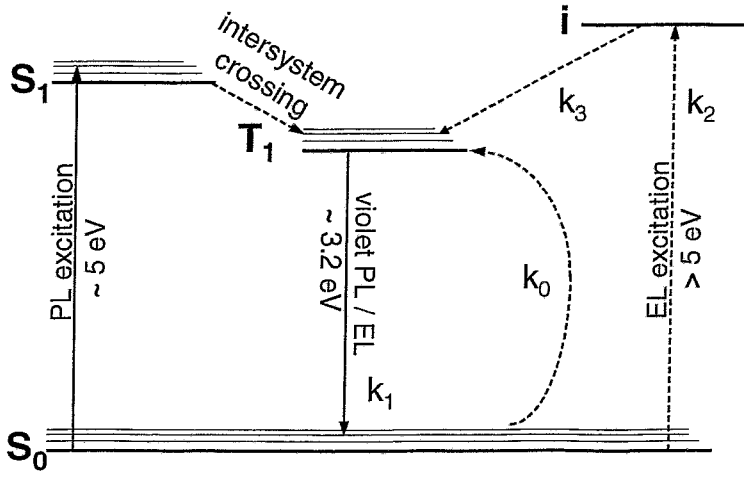


Fig. 6.23:
Schematic energy level system of an ODC consisting of a ground singlet state S_0, a first excited singlet state S_1 and an excited triplet state T_1. Hot electrons cause the excitation of the LC up to an intermediate state i. Radiative transitions are plotted with solid arrows, non-radiative transitions with dashed arrows.

The decay- and rise-time measurement gives additional information about the excitation mechanism. Let us start with the consideration of a general 3-level-system as shown on the right side of Fig. 6.23. The levels are the ground singlet state S_0, the first excited triplet state $T_1$and the intermediate state i. The specific nature of the intermediate state i - whether it is an ionized state, the S_1 state or whatever – cannot be explained in detail, but this is out of interest for the following discussion. The populations of the three levels are N_S, N_T and N_i. The total number of LCs is N_0. With the transition rates k_1: $T_1 \rightarrow S_0$, k_2: $S_0 \rightarrow$ i and k_3: i $\rightarrow T_1$ we get the following rate equations:

$$\dot{N}_T = -k_1 N_T + k_3 N_i \tag{6.1}$$

$$\dot{N}_i = -k_3 N_i + k_2 N_S \tag{6.2}$$

N_S can be substituted by $N_S=N_0-N_T-N_i$, and so we get:

$$\dot{N}_i = -k_3 N_i + k_2 \left(N_0 - N_T - N_i\right) \tag{6.3}$$

From (6.1) we get:

$$N_i = \frac{1}{k_3}\left(\dot{N}_T + k_1 N_T\right) \quad \text{and} \quad \dot{N}_i = \frac{1}{k_3}\left(\ddot{N}_T + k_1 \dot{N}_T\right)$$

and inserting this in (6.3) gives:

$$\frac{1}{k_3}\left(\ddot{N}_T + k_1\dot{N}_T\right) = -\dot{N}_T - k_1 N_T + k_2 N_0 - k_2 N_T - \frac{k_2}{k_3}\left(\dot{N}_T + k_1 N_T\right)$$

$$\ddot{N}_T + k_1\dot{N}_T + k_3\dot{N}_T + k_1k_3 N_T + k_2k_3 N_T + k_2\dot{N}_T + k_1k_2 N_T = k_2k_3 N_0$$

$$\ddot{N}_T + \left(k_1 + k_2 + k_3\right)\dot{N}_T + \left(k_1k_2 + k_1k_3 + k_2k_3\right)N_T = k_2k_3 N_0 \tag{6.4}$$

With:

$$\begin{aligned} K_1 &= k_1 + k_2 + k_3 \\ K_0 &= k_1k_2 + k_1k_3 + k_2k_3 \\ K_C &= k_2k_3N_0 \end{aligned} \tag{6.5}$$

we get:

$$\ddot{N}_T + K_1\dot{N}_T + K_0 N_T = K_C \tag{6.6}$$

This is an inhomogeneous linear differential equation with constant coefficients. Since the inhomogeneous part is constant, the general solution is:

$$N_T(t) = C_1e^{r_1t} + C_2e^{r_2t} + C_3 \tag{6.7}$$

and r_1 and r_2 are roots of the characteristic equation:

$$r^2 + K_1r + K_0 = 0 \tag{6.8}$$

From the boundary conditions we get:

$$C_1 = \frac{r_2}{r_1 - r_2}\frac{K_C}{K_0} \tag{6.9}$$

$$C_2 = -\frac{r_1}{r_1 - r_2}\frac{K_C}{K_0} \tag{6.10}$$

$$C_3 = \frac{K_C}{K_0} \tag{6.11}$$

In this general case the decay will be biexponential as shown in equation (6.7). Let us now assume the case $k_3 >> k_1, k_2$. Then (6.5) becomes:

$$\begin{aligned} K_1 &\approx k_3 \\ K_0 &\approx k_3\left(k_1 + k_2\right) \end{aligned} \tag{6.12}$$

Under this condition we find $K_1^2 >> K_0$. To avoid that one of the roots r of equation (6.8) becomes zero, the Taylor-expansion is used. Finally the coefficients (given in 6.9-6.11) can be described as:

$$C_1 = \frac{-k_1 - k_2}{2k_1 + 2k_2 - k_3} C_3 \approx \frac{k_1 + k_2}{k_3} C_3 = \frac{k_2}{k_3} N_0$$
$$C_2 = -\frac{k_1 + k_2 - k_3}{2k_1 + 2k_2 - k_3} C_3 \approx -C_3 = -\frac{k_2}{k_1 + k_2} N_0 \qquad (6.13)$$
$$C_3 = \frac{k_2}{k_1 + k_2} N_0$$

It is obvious that C_1 vanishes for $k_3 >> k_2$. So the equation (6.7) can be written as:

$$N_T(t) = \frac{k_2}{k_1 + k_2} N_0 \left(1 - e^{-(k_1 + k_2)t}\right) \approx \frac{k_0}{k_1 + k_0} N_0 \left(1 - e^{-(k_1 + k_0)t}\right) \qquad (6.14)$$

This is exactly the solution of a 2-level-system consisting only of the states S_0 and T_1. For better understanding the $S_0 \rightarrow T_1$ transition rate of such a simplified systems is given as k_0, which is in principal a combination of k_2 and k_3 (see Fig. 6.23).

In the experiments (Fig. 6.22) a monoexponential decay with a decay constant of 100 µs – which is identical with the PL decay time – was measured, which shows that k_3 has to be very large. If a LC is excited to the intermediate state i, it relaxes in a very short time to the T_1 state. As a rise time of 100 µs was measured, k_0 must be small compared to k_1.

At this point the different physical meaning of k_0 and k_1 has to be mentioned. Whereas the transition rate k_1 gives an information of the time scale of relaxation, k_0 depends on geometrical parameters, namely the interaction cross section σ between an electron and a given ensemble of LCs and the injection current density J. As the absolute EL intensity increases linearly with J, k_0 should also be proportional to J and can be expressed as

$$k_0 = \frac{1}{|e|} \sigma \cdot J \qquad (6.15)$$

with e being the electron charge. With the experimental results it is now possible to assess an upper limit for the excitation cross section. If we assume $k_0 \leq 0.1 k_1$, $k_1 \approx 10^3\ s^{-1}$ and $J \approx 10^{-3}\ Acm^{-2}$ a maximum value of $1.6 \times 10^{-13}\ cm^{-2}$ is deduced. It should be noted that, in spite of the use of a 2-level-system, it cannot be distinguished, whether the LCs are excited directly or via an intermediate state with a fast transition rate to T_1. The EL transient measurements only exclude the case of a 3-level-system with a slow k_3 value.

Based on these results the inelastic scattering of electrons at LC is favored as the dominant excitation process because of the following reasons. If the LC is ionized, the internal structure of the LC will be rearranged, and the recapture of an electron could result in a structure different from the initial one. So the probability that the ionization of a LC

followed by electron recapture results in the same structure, can be low. A similar phenomenon is known from silica, where the ionization of the neutral oxygen vacancy is regarded to be an irreversible and destructive process [Hori97]. Due to the decay-time measurement the electron recapture would have to be a fast process. However, the recapture of electrons depends on the capture cross section and the injection current density, and for low injection currents a small transition rate to T_1 is expected. Finally the energy to ionize a LC will be higher than the energy to excite it, and therefore only a very small fraction of electrons will have sufficient energy to ionize a LC. This implies that the process of impact ionization followed by electron recapture is not likely to explain the experimental results.

If the LC is excited by inelastic scattering of electrons, the excitation cross section will be linked to the specific energy distribution of the electrons. As already mentioned the buildup of space charges causes local deviations of the electric field. The excitation cross section will vary in the same manner leading to an inhomogeneous excitation of the LCs depending on their position in the oxide layer. More specifically, most of the EL will come from LCs located closer to the gate. Furthermore, after injection the electrons need a certain acceleration distance to approach the saturated energy distribution. According to this there should be a dark zone close to the Si-SiO_2 interface where the kinetic energy of the electrons is not high enough to excite a LC.

6.3. Monolithically integrated Optocoupler

6.3.1. Parameters and basic properties

Using the features of the nanocluster-based light emitter a monolithically integrated optocoupler was designed [Gebe00b]. Fig. 6.24 shows a schematic of this device, which includes the emitter and a detector based on a pin - diode. The luminescence element basically consists of the MOS structure describe in section 3.1 where a positive voltage is applied to the ITO contact for excitation of the EL. The voltage V_{prim} depends on the thickness of the oxide layer, while the pin-diode is operated at the voltage V_{sec} which is in the range of 0..5V. Both elements are separated by a SiO_2 layer for galvanic isolation. By changing the thickness of the insulating SiO_2 layer the appropriate voltage protection for the potential difference between the emitter and detector device can be selected. For the demonstration device described in this work the thickness of the oxide is 500 nm.

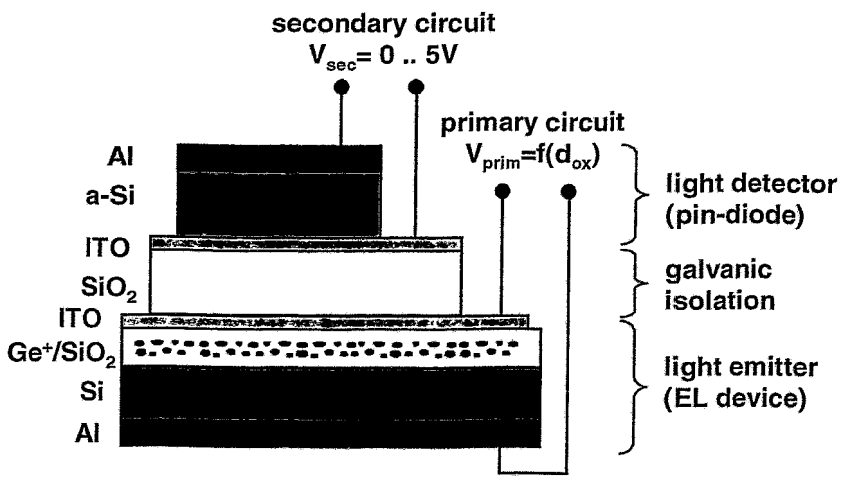


Fig. 6.24:
Schematic of a monolithically integrated optocoupler in Si-technology. The device consists of an emitter, a SiO_2 layer for galvanic isolation and a pin-diode for signal detection.

6.3.2. Transfer characteristics

The transfer characteristic I_{sec} vs. I_{prim} of the optocoupler device is shown in Fig. 6.25. The secondary current I_{sec} is measured at the photodiode at 0 V bias. The constant current I_{prim} is applied to the gate electrode of the emitter. The area of the emitter and the pin-diode was varied between 0.03 .. 1.0 mm^2. The dark current of the diode is $<2x10^{-9}$ Acm^{-2} and its sensitivity is about 0.18 A/W at a wavelength of 400 nm [Borc00].

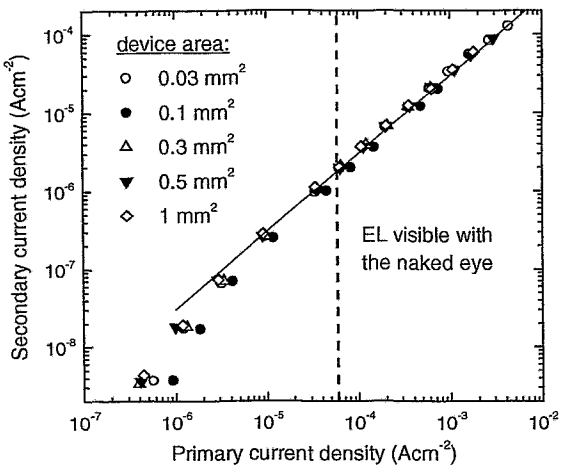


Fig. 6.25:
Transfer characteristics of a monolithically integrated optocoupler. A linear dependence of the diode current on the EL excitation current was observed.

After a first superlinear rise a linear dependence between I_{sec} and I_{prim} can be observed. The photocurrent I_{sec} is of the order of nA and thus at least two orders of magnitude larger than the dark current. For excitation current densities > $6x10^{-5}$ Acm^{-2} the blue-violet light becomes visible to the naked eye. Since the detector already works at lower light intensities, the optocoupler device could be operated at much lower excitation currents which should lead to an improvement in the lifetime and stability of the device. An important aspect for future applications is the detector diode optimization for the blue-violet wavelength range.

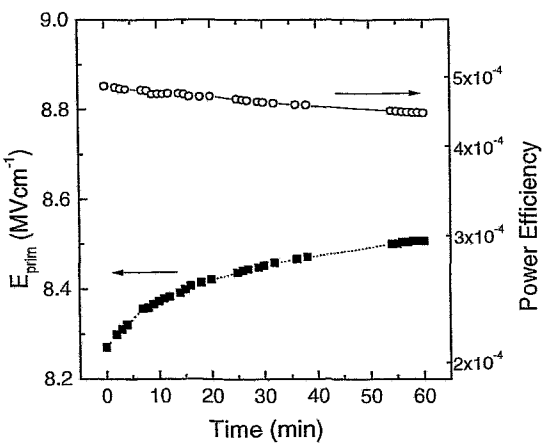


Fig. 6.26:
Time dependence of the EL efficiency and the electric field for an optocoupler operated at constant current density of $5x10^{-5}$ A/cm^2. The efficiency decreases while the electric field shows an increase.

In Fig. 6.26 the time dependence of the power efficiency and the electric field E_{prim} vs. time for an optocoupler device driven with a constant current density of $5x10^{-5}$ A/cm^2 is depicted. The power efficiency remains nearly constant but shows a small decrease while the electric field is increased. The increase in the voltage (about +3%) which causes a higher input power and thus a reduction of the efficiency cannot explain the whole efficiency decrease (about -10%). Other processes such as charging effects, oxide degradation, possible changes in the properties of the bulk of the oxide caused by stress induced traps and the conversion of luminescence centers into other centers could be the reason for this behavior.

7. Conclusion and outlook

The aim of this work was to find a correlation between the electrical, optical and microstructural properties of thin SiO_2 layers containing group IV nanostructures produced by IBS. The investigations were focused on two main topics: The electrical properties of Ge- and Si-rich oxide layers were studied in order to check their suitability for non-volatile memory applications. Secondly, EL results of Si, Ge and Sn rich SiO_2 layers were compared to electrical properties to get a better understanding of the luminescence mechanism.

7.1. Nanostructures for memory applications

Ge^+ and Si^+ implanted SiO_2 layers with a thickness of 20 and 30 nm were investigated regarding their microstructure and their electrical memory properties. In Ge rich oxide layers small Ge nanoclusters were observed with TEM. The size of the nanostructures was in the range of 3...5 nm. Typically, no lattice fringes were observed which implies that the nanoclusters are amorphous. The detailed structure of the clusters is not clear because one cannot clearly distinguish between pure Ge and GeO_x clusters. In order to investigate the redistribution of Ge in the oxide layers RBS analysis was used. An interesting feature from these investigations was the observed formation of two separated clusters bands during annealing, one in the R_p region and a second one near the Si/SiO_2 interface [Bora99a]. This effect is caused by a self-organization process. Dpa values >1 at the Si/SiO_2 interface lead to the dissociation of the SiO_2 network into its elemental components silicon and oxygen. The oxygen diffuses to the Si/SiO_2 interface leaving an oxygen depleted region behind, which now contains an overstoichiometric fraction of silicon. This excess silicon forms small precipitates acting as nucleation centers for the diffusing Ge, which finally leads to the formation of a δ–like second clusterband in a distance of about 3..4 nm from the interface.

For Si implanted devices the investigation of the microstructure is more difficult. Small Si precipitates in a SiO_2 matrix give only a very weak TEM contrast. The only chance for the detection of Si nanoclusters is the occurrence of crystalline clusters which would become visible due to the lattice fringes. In the literature such structures are typically reported for excess Si concentrations >10%. This means that for the devices observed in this work it is very difficult to see such clusters at all. Indeed, only in one case Si clusters were detected in the TEM image (Fig. 4.14). The position of the clusters was near the projected range. In general the diffusivity of the implanted silicon is lower compared to Ge or Sn which should prevent a strong diffusion towards the Si/SiO_2 interface. The depth profiling of the excess Si by RBS could not be applied to our samples. In order to use this method one has to implant the Si isotope ^{29}Si to achieve a mass contrast of the implanted species in comparison to the ^{28}Si from the matrix.

At first sight the unique "double-clusterband" features of the microstructure of Ge implanted oxide layers seem to be very useful for direct tunneling for the charging of the near interface clusters by using low voltages. Indeed, the Ge implanted samples show reasonable programming windows already at programming voltages around 5 V which corresponds to an electric field of 2.5 $MVcm^{-1}$. It was also observed that the onset of programming effects is shifted towards lower voltages with increasing Ge content and with increasing implantation energy. In the case of silicon it appears that programming windows which meet the requirements for device applications can only be achieved if programming pulses corresponding to electric fields > $5MVcm^{-1}$ are applied. This is because of the more or less fixed position of the excess Si in the R_p region. The implanted Ge which diffuses towards the interface allows the charge trapping already at lower voltages because of the decreased tunneling distance for the electrons which are injected from the interface. So these results are basically in good correlation with the effects observed from the microstructure.

Ge implanted devices show large programming windows up to about 4 V, while for the Si implanted devices the programming window reaches a maximum of 2.3 V. In the case of Ge it was also shown that the programming window size is enlarged for higher implantation energies. In order check the influence of the "pure" implantation induced damage against the stochiometry related issues Ar^+ implanted SiO_2 layers were investigated. In comparison to Si^+ or Ge^+ implanted oxides only very small programming windows were observed. After only 10...20 W/E cycles the programming window shrinks. It is assumed that no NOV, but implantation induced E' centers are present in the oxide layer. This and the investigated memory properties of Si^+ or Ge^+ implanted oxide layers lead to the assumption that for "stable" charge trapping not only implantation induced defects, but also excess group IV atoms are necessary.

One of the most important parameters of nv-memories is the data retention. Ge implanted layers with large programming windows exhibit a poor retention, which is of the order of only 10^3 seconds at room temperature. In the course of our investigations it was also realized that the Ge implanted layers are very sensitive to the measurement of the trapped charge itself. This can be easily understood by the fact that the programming effects occur already at low voltages, which means that during a CV scan (which was performed in order to determine the flatband voltage shift) the amount of trapped charge is changed. In principle this poor retention behavior means that Ge^+ implanted oxide layers do not fulfill the requirements of nv-memories. The promising results from the investigations of the microstructure, especially the self-organization processes leading to the formation of the near interface cluster band, do not finish in the main advantage of real quantum size effects. Operation at lower voltages compared to the common EEPROM technology seems possible, but the charge storage mechanism itself is related to traps and not to quantum effects.

In contrast to this SiO_2 layers implanted with low energy Si^+ ions exhibit a remarkably good retention. After high-temperature treatment at 200°C programming windows larger than 0.5 V were observed even after more than 7 days. This excellent retention makes Si implanted oxide layers well suitable for nv-memories. However, the programming voltages necessary for device operation correspond to electric fields of 5 .. 7 $MVcm^{-1}$. Thus, the

principal idea of direct tunneling could not be realized. For oxide thicknesses of 20 nm as used in this work this means that operation voltages of > 10 V are required. The observed endurance is of the order of 10^6, thus meeting the range of the common technology. However, it has to be mentioned that the pulse duration for writing and erasing was as long as 50 ms. For operation with shorter pulses a proportional increase of the number of W/E cycles was observed. Thus it can be concluded, that the main parameter leading to the destruction of the device is the injected charge.

In summary ion beam synthesized nanostructures are promising candidates for the application in novel non-volatile memories. Ge-rich oxides layers show interesting microstructural effects but exhibit poor memory properties. In the case of Si-rich layers the electric properties are excellent but the specific microstructure could not be investigated in detail. However, from the results described in this work one can conclude that the charge storage is not related to quantum confinement effects. In fact, the charge trapping is caused by defect related trapping centers. These defects produced during the IBS process are the NOV or the E' center. The nature of the defects is not fully understood. Further research, especially the correlation of the electrical results with other methods, e.g. ESR and positron annihilation spectroscopy (PAS), is necessary.

7.2. Nanostructures and their application in Si-based optoelectronics

SiO_2 layers implanted with Ge, Sn, and co-implanted with Si and C were investigated regarding their optoelectronic properties. Based on previous investigations regarding the PL of Si and Ge rich oxide layers [Rebo00a] this work was focused on electrical measurements and the EL of these layers. The aim was to find a correlation between microstructure, electrical properties and EL in order to gain a better understanding of the luminescence mechanism.

The EL spectra of Ge rich oxides are very similar to those of the PL indicating that the same defects cause the luminescence. The luminescence shows a peak at 3.16 eV which is attributed to defects of the ODC type. For Ge oxide layers with thicknesses between 500 .. 130 nm an increase of the EL efficiency with decreasing oxide thickness was observed. A maximum power efficiency of 0.5% was achieved for 130 nm SiO_2 layers [Gebe00a]. This is among the highest ever reported values for Si-based light emitters produced in the standard silicon technology. For devices with oxide layers <130 nm the trend of increasing power efficiency is not continued. Typical values are in the order of 10^{-4} .. 10^{-3}. In general one can say that the power efficiencies obtained in this work are higher than known from the literature for similar systems. However, even these efficiencies are significantly lower than the requirements of display technologies (efficiency about 10%). Therefore such Si-based light emitters may only have a future in specific niche applications in integrated optical systems.

PL and EL from Sn implanted layers were also investigated. In contrast to Ge implanted layers the samples show spectra containing an additional peak around 2.6 eV beside the main peak at 3.2 eV. This low-energy peak shows a featureless excitation spectrum with an increase towards higher energies. In the case of EL the intensity of this low-energy peak decreases at high electric fields. As a first hypothesis this effect could be caused by the influence of hot electrons which are present in the HFR leading to destructive changes in the oxide. The values for the EL power efficiency of Sn implanted oxide layers are in the range of $1..2.5x10^{-4}$. These values represent data from first sets of samples without the extensive optimization as done in the case of the Ge rich oxide layers.

The co-implantation of Si and C into thin SiO_2 films followed by thermal annealing leads to the formation of small amorphous nanostructures of Si, C and O. The possibility to extract visible light from these structures was demonstrated. Strong PL in the blue and yellow spectral region was achieved after excitation at 4.77 eV. Based on AES investigations the blue PL is assumed to be caused by $Si_yC_{1-y}O_x$ complexes with $x<2$. The specific microstructure of the defects is not understood so far. The Si- and C-rich oxide layers show relatively broad EL spectra with a peak around 2.7 eV. The maximum EL power efficiency is $1.2x10^{-5}$.

Regarding the electrical properties several investigations using the IV and CV methods were carried out. It was found that the IV characteristics show a strong temperature dependence in the MFR. The charge injection and transport mechanism can be explained by a combination of different models. The TAT model cannot explain the temperature dependence, but partly the IV curves could be fitted with the PF and the SCL model. This implies a complex mechanism including space charge, trapping and detrapping effects. In the HFR the characteristics show a reduced temperature dependence and can be fitted by the FN model. Since the EL occurs in this high field region, the investigations were focused on this operation regime. It was found that the electron trapping, which dominates the MFR, competes with the trapping of positive charge in the HFR. It is assumed that the positive charge trapping can be attributed to ODC – the same centers, causing the luminescence. However, for a direct evidence further investigations are necessary, especially the correlation of trapping effects and high field stress to the results of ESR measurements.

One of the main problems of the described EL devices is the long term stability. Typically the lifetime of devices operated in a regime where the EL can be seen with the naked eye is only in the order of several minutes. However, for a view devices also lifetimes >1h were observed. One of the main problems is related to the material of the gate contact. It is known that ITO tends to dissociate at elevated temperatures. This behavior is not only a critical issue for the production process of the EL devices and their integration into integrated optical systems, it also plays an important role during device operation at high electric fields. During the investigations of several samples we observed sparkling spots on the gate contact shortly before device breakdown. These bright tiny spots occurred mostly at the edges of the devices. Within seconds after beginning of these processes the device broke. One of the tasks for the further improvement of these EL devices will be the comparison of several contact materials and also the use of an edge passivation, e.g. a standard LOCOS process.

The mechanism of the EL is explained by the transport and scattering processes of hot electrons in the SiO_2 conduction band. If a sufficiently high electric field is applied to the EL device, electrons are injected via TAT or FN tunnel injection from the Si substrate. The electrons moving in the conduction band of the SiO_2 can be characterized by an energy distribution which varies with the position in the oxide layer. The majority of the electrons does not have enough energy for the excitation of a luminescence center. However, a small amount of electrons from the high-energy tail of the energy distribution contain enough energy to excite a LC during a scattering process, namely impact excitation. The transferred energy excites the LC from the ground state S_0 to an intermediate state i. Additionally, due to the high electric field the effect of ionization of LC from the ground state S_0 to an ionized state may occur. The released electron moves towards the metal electrode leaving behind a positively charged LC. If the ionized center traps an electron, it can relax with a certain probability to the T_1 triplet state.

The results of transient EL measurements on Ge implanted oxide layers showed a monoexponential decay with a decay constant of 100 µs. This value complies with the decay time of former PL investigations [Rebo00a] and gives additional information about the EL excitation mechanism. If an LC is excited to the intermediate state i, it relaxes in a very short time to the T_1 state, and the physical behavior will be very similar to that of a 2-level-system. The agreement of the decay times for PL and EL gives a further strong indication that the defects causing the luminescence are similar. This means, that there is no chance to use the EL devices for optical data communication because of the limited frequency of 10 kHz.

However, the devices are of interest for other specific applications in the field of novel Si based integrated optical systems. A variety of microsystems require optical sensing techniques, e.g. for the detection of moving actuators or the control of flowing liquids. Since the main part of today's microsystems is based on Si technology, the direct integration of a light emitter in such systems is an advantage for the formation of monolithic structures. The integration of expensive compound semiconductor light emitters could be avoided, leading also to a cost reduction. One interesting application is the so called Lab-on-Chip system, typically consisting of glass substrates or standard silicon chips and combinations with microsystems for liquid handling. The use of light emitters in such systems allows for instance the direct excitation of fluorescence marked substances for biochemical analytics [Gebe01b]. The main advantage of Si based emitters in such an application is the possible scaling of devices allowing the formation of high-density arrays. This is of eminent interest for high-throughput screening, e.g. in the field of pharmaceutical drug screening.

As an application-related issue of this work an integrated optocoupler in Si technology was designed and fabricated as a prototype [Gebe00b]. It basically consists of the EL device, an insulation layer and a pin-diode used for the detection of the emitted light. The fabrication process is, in principle, a continuation of the formation process of the MOS capacitor with a Ge-rich gate oxide and an ITO layer as a gate contact. On top of this EL device a SiO_2 layer was deposited for insulation. With the variation of the thickness of this oxide layer the galvanic protection against high voltage differences can be easily tailored to meet the requirements of the specific application. On top of this layer system an a-Si

pin-diode diode was deposited by means of a multi-step CVD process. The first results of this prototype demonstrated the working principle of the device. Linear transfer characteristics were observed in a range of over 3 orders of magnitude of the applied current. One of the promising results of these investigations is the possible operation of such devices at moderate currents preventing the early device breakdown. This shows also the possible application of the devices for optical sensing in integrated systems. In such a closed system the applied current density can be reduced up to a value causing just enough luminescence for the detector. The a-Si pin-diode used in the prototype had a maximum sensitivity of about 0.3 A/W around 600 nm and of 0.18 A/W at a wavelength of 400 nm. With a diode which would be further optimized to the wavelength of the emitter the performance of the optocoupler could be further increased.

The progress of the past decade concerning Si-based light emission shows that the "simple" system Si/SiO_2 still contains many attractive but hidden features. The ongoing research in this field will produce even more surprising results, like for instance the possible optical gain demonstrated by Pavesi et al. [Pave00]. The improvement of measurement methods and novel fabrication technologies will drive the observation of formation processes, microstructure and electrical properties of nano-structures to a new quality, helping to understand their unique physical properties. It seems, that there is still a future for silicon – a future in the nano-dimension. And even better, this future can be bright.

8. Appendix

8.1. Abbreviations

Abbreviation	Explanation
a.u.	arbitrary units
AES	Auger – electron epectroscopy
AFM	atomic force microscopy
BD	breakdown
CMOS	complementary metal-oxide-semiconductor technology
CV	vapacitance-voltage characterisitic
CVD	chemical capor deposition
EL	electroluminescence
EQE	external quantum efficiency
ESR	electron spin resonance
FET	field effect transistor
FN	Fowler-Nordheim
Ge	germanium
HF-CV	high frequency capacitance-voltage measurements
HFR	high field region ($E > 7$ MVcm^{-1})
IQE	internal quantum efficiency
ITO	indium tin oxide (special kind of TCO, contact material for EL)
IV	current - voltage characterisitic
LC	luminescence center
LOCOS	local oxidation of silicon
LFR	low field region ($E < 4$ MVcm^{-1})
LPCVD	low pressure chemical vapour deposition
L-SEM	lateral single electron memory
MFR	mid field region (4 MVcm$^{-1} < E < 7$ MVcm^{-1})
MOS	metal-oxide-semiconductor
NBOH	non-bridging oxygen hole center
NC	nanocluster
NCM	nanocluster memory
NOV	neutral oxygen vacancy
NRA	nuclear reaction analysis

ODC	oxygen deficiency center
PE	power efficiency
PECVD	plasma enhanced chemical vapor deposition
PF	Poole-Frenkel conduction
PL	photoluminescence
PLE	photoluminescence excitation
PS	porous silicon
PVD	physical vapor deposition
RT	room temperature
RTA	rapid thermal annealing
RTP	rapid thermal processing
SBD	soft breakdown
SEM	scanning electron microscope
SEMD	single electron memory device
SET	single electron transistor
Si	silicon
SILC	stress induced leakage current
Sn	tin
SNOS	silicon-nitride-oxide-silicon
SOI	silicon – on – insultator
SRAM	static random access memory
STM	scanning tunneling microscopy
TAT	trap-assisted-tunneling
TCO	transparent conductive oxide
TDDB	time-dependent-dielectric breakdown
TFL	trap filled limited current
TRIM	software package, transport of ions in matter
ULSI	ultra large scale integration
VLSI	very large scale integration
VRH	variable range hopping
W/E	write/erase cycles
XPS	X-ray induced photoelectron spectroscopy
ZMD	Zentrum Mikroelektronik Dresden

8.2. Symbols

Symbol	Explanation
A	dot area
Å	Ångström, 1Å = 0.1 nm
C	capacitance (total)
C_{OX}	oxide capacitance
C_{SC}	capacitance of the semiconductor
d_{Ox}	thickness of the oxide layer
e	charge of an electron
E	electric field
E_{BD}	electric field at device breakdown
E_{CB}	energetic position of the conduction band
E_{ex}	excitation energy
E_F	Fermi-energy
E_{VB}	energetic position of the valence band
ħ	Planck's constant
I	current
I_{DS}	drain-source current
I_{prim}	primary current (EL excitation current) of the optocoupler device
I_{sec}	secondary current (photocurrent) of the optocoupler device
J	current density
k_r	recombination rate of excitons
m^*	effective electron mass
m_0	mass of electron
N_{trap}	trap concentration
N_{trap_eff}	effective trap concentration
P_{Trap}	trapping efficiency
Q_{bd}	charge to breakdown
Q_f	fixed oxide chare
Q_{inj}	injected charge
Q_{it}	interface trapped charge
Q_m	mobile ionic charge
Q_{ot}	oxide trapped charge
Q_{ox}	total charge trapped in the oxide
Q_{trap}	trapped charge
Q_{trap_neg}	negative trapped charge

Q_{trap_pos}	positive trapped charge
T	temperature
V	voltage
V_{FB}	flatband voltage
V_{GS}	gate-source voltage
V_{prog}	programming voltage
V_T	threshold voltage
x_T	position of the charge centroid
Δk	uncertainty of momentum
ΔV_{FB}	flatband voltage shift
ΔV_T	shift of the threshold voltage
ΔV_{PW}	size of programming window
Δx	uncertainty of space
Φ_B	barrier height
Φ_{Trap}	depth of trap
β	relative programming window
ε_0	dielectric constant
ε_r	specific (relative) dielectric constant
σ	electrical conductivity
σ_i	capture cross section

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Hiermit versichere ich, dass ich die vorliegende Arbeit ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel angefertigt habe. Die aus fremden Quellen direkt oder indirekt übernommenen Gedanken sind als solche kenntlich gemacht. Die Arbeit wurde bisher weder im Inland noch im Ausland in gleicher oder ähnlicher Form einer anderen Prüfungsbehörde vorgelegt.

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Nanocluster-rich SiO_2 layers produced by ion beam synthesis: electrical and optoelectronic properties

by

Thoralf Gebel

Theses

- The aim of this work was to find a correlation between the electrical, optical and microstructural properties of thin SiO_2 layers containing group IV nanostructures produced by ion beam synthesis. The investigations were focused on two main topics: The electrical properties of Ge- and Si-rich oxide layers were studied in order to check their suitability for non-volatile memory applications. Secondly, photo- and electroluminescence (PL and EL) results of Ge-, Si/C- and Sn-rich SiO_2 layers were compared to electrical properties to get a better understanding of the luminescence mechanism.

- In Ge^+ implanted SiO_2 layers with a thickness of 20 and 30 nm small Ge nanoclusters were observed by transmission electron microscopy. The size of the nanostructures was in the range 3...5 nm. Typically, no lattice fringes were observed, which implies that the nanoclusters are amorphous. Two separated clusters bands are formed during annealing, one in the R_p region and a second one near the Si/SiO_2 interface. This effect is caused by a self-organization process. During implantation the SiO_2 network dissociates into its elemental components silicon and oxygen. The oxygen diffuses to the Si/SiO_2 interface leaving an oxygen depleted region behind, which now contains an overstoichiometric fraction of silicon. This excess silicon forms small precipitates acting as nucleation centers for the diffusing Ge, which finally leads to the formation of a δ–like second clusterband in a distance of about 3...4 nm from the SiO_2/Si interface.

- At first sight the unique "double-clusterband" features of the microstructure of Ge implanted oxide layers seem to be very useful for direct tunneling for the charging of the near interface clusters by using low voltages. Indeed, the Ge implanted samples show reasonable programming windows already at programming voltages around 5 V (2.5 $MVcm^{-1}$). However, the devices exhibit a poor retention, which is of the order of only 10^3 seconds at room temperature. This means that Ge^+ implanted oxide layers do not fulfill the requirements of nv-memories. The promising results from the investigations of the microstructure, especially the self-organization processes leading to the formation of the near interface cluster band, do not finish in the main advantage of real quantum size effects. Operation at lower voltages compared to the common EEPROM technology seems possible, but the charge storage mechanism itself is related to traps and not to quantum effects.

- For Si-implanted oxide layers it appears that programming windows which meet the requirements for device applications can only be achieved if programming pulses corresponding to electric fields > 5 $MVcm^{-1}$ are applied. This is because of the more or less fixed position of the excess Si in the R_p region. Thus, the principal idea of direct tunneling could not be realized. The Si-rich SiO_2 layers exhibit a remarkably good retention. After high-temperature storage of the devices at 200°C programming windows larger than 0.5 V were observed even after more than 7 days. This excellent retention makes Si-implanted oxide layers well suitable for nv-memories. The observed endurance is of the order of 10^6, thus meeting the range of the common technology.

- Based on the results of the memory investigations from Si/Ge implanted MOS capacitors MOSFETs and finally also 256k nv-SRAM systems were fabricated in cooperation with ZMD Dresden. A programming window of 1 V was achieved and full functionality of the nv-SRAM was demonstrated. So ion beam synthesized nanostructures are promising candidates for the application in novel non-volatile memories. However, from the results described in this work one can conclude that the charge storage is not related to quantum confinement effects. In fact, the charge trapping is caused by defect related trapping centers.

- SiO_2 layers implanted with Ge, Sn, and co-implanted with Si and C were investigated regarding their optoelectronic properties. The EL spectra of Ge rich oxides are very similar to those of the PL indicating that the same defects cause the luminescence. The EL spectrum shows a peak at 3.16 eV which is attributed to defects, namely oxygen-deficiency centers (ODC). A maximum EL power efficiency of 0.5% was achieved for 130 nm SiO_2 layers. This is among the highest ever reported values for Si-based light emitters produced in standard Si-technology.

- PL and EL spectra from Sn implanted oxides contain an additional peak around 2.6 eV beside the main peak at 3.2 eV. This low-energy peak shows a featureless excitation spectrum with an increase towards higher energies. In the case of EL the intensity of this low-energy peak decreases at high electric fields. As a first hypothesis this effect could be caused by the influence of hot electrons which are present at electric fields > 7 $MVcm^{-1}$ leading to destructive changes in the oxide. The maximum EL power efficiency of Sn implanted oxide layers is $2.5x10^{-4}$.

- The co-implantation of Si and C into thin SiO_2 films followed by thermal annealing leads to the formation of small amorphous nanostructures of Si, C and O. The possibility to extract visible light from these structures was demonstrated. Strong PL in the blue and yellow spectral region was achieved after excitation at 4.77 eV. Based on AES investigations the blue PL is assumed to be caused by $Si_yC_{1-y}O_x$ complexes with $x<2$. The specific microstructure of the defects is not understood so far. The Si- and C-coimplanted oxide layers show relatively broad EL spectra with a peak around 2.7 eV. The maximum EL power efficiency is $1.2x10^{-5}$.

- The current-voltage (IV) characteristics of Ge-rich oxide layers show a strong temperature dependence at electric fields of 5...7 $MVcm^{-1}$. The trap-assissted tunneling (TAT) model cannot explain the temperature dependence, but partly the IV-curves could be fitted with the Poole-Frenkel and the space-charge-limited current (SCL) model. This implies a complex mechanism including space charge, trapping and detrapping effects. At electric fields > 7 $MVcm^{-1}$ the characteristics show a reduced temperature dependence and can be fitted by the FN model. It was found that the electron trapping, which dominates at electric fields of 5...7 $MVcm^{-1}$, competes with the trapping of positive charge at high electric fields. It is assumed that the positive charge trapping can be attributed to ODC – the same centers, causing the luminescence.

- The mechanism of the EL is explained by the transport and scattering processes of hot electrons in the SiO_2 conduction band. If a sufficiently high electric field is applied to the EL device, electrons are injected via TAT or Fowler-Nordheim (FN) injection from the Si-substrate. Electrons from the high-energy tail of the energy distribution contain enough energy to excite a luminescence center during a scattering process, namely impact excitation.

- The results of transient EL measurements on Ge-implanted oxide layers show a monoexponential decay with a decay constant of 100 µs. This value complies with the decay time of former PL investigations and implies that the physical behavior is very similar to that of a 2-level-system. The agreement of the decay times for PL and EL gives a further strong indication that the defects causing the luminescence are similar.

- As an application-related issue of this work an integrated optocoupler in Si-technology was designed and fabricated as a prototype. It basically consists of the EL device, an insulation layer and a pin-diode used for the detection of the emitted light. The results of this prototype demonstrated the working principle of the device. Linear transfer characteristics were observed in a range of over 3 orders of magnitude of the applied current.