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Gerhard Brauer, Wolfgang Skorupa

HeT-SiC-05

International Topical Workshop on
Heteroepitaxy of 3C-SiC on Silicon and
its Application to Sensor Devices

Forschungszentrum
Rossendorf

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International Topical Workshop on Heteroepitaxy of 3C-SiC on Silicon and its Application to Sensor Devices

April 26 to May 1, 2005,
Hotel Erbgericht Krippen / Germany

- Selected Contributions -

Preface

The real danger of growing environmental pollution forces mankind to take action by developing environmentally-friendly products and technologies, and increasing efforts to protect and maintain the wellbeing of humankind which is permanently exposed to that increasingly harmful environment. For these reasons it is a challenging task for areas like microelectronics, biotechnology, or biomedicine to meet the growing demands for high-quality electronic sensors to work at high temperatures and under extreme environmental conditions. At present, silicon carbide (SiC) is the best candidate for such extreme applications – for example, in sensors for the control of exhaust gases to improve environmental conditions, and in sensor-carrying needles and other devices for biomedical applications.

SiC microelectronics technology is currently dominated by wafers of the hexagonal polytypes 4H- and 6H-SiC. However, the market for SiC-based devices remains very small due to (i) the high cost of SiC wafers, and (ii) the deviation of SiC device parameters from theoretical expectations due to the low effective carrier mobility. Cubic 3C-SiC should exhibit the highest mobility of all SiC polytypes, but it is not available in the same wafer size as the hexagonal varieties. However, epitaxially-grown 3C-SiC/Si has the advantage of low cost and larger wafers,

Guided by Forschungszentrum Rossendorf during 2002-2005, the European project "FLASiC" (**F**lash **LA**mp Supported Deposition of 3C-**SiC**) involved collaborative work by eleven partners from Germany, France, UK, Greece and Spain. The goal of the project was the production of large-area epitaxial 3C-SiC layers grown on Si, where in an early stage of SiC deposition the SiC/Si interface is rigorously improved by energetic electromagnetic radiation from purpose-built flash lamp equipment developed at Forschungszentrum Rossendorf. In the frame of the project it was not only necessary to develop further this very special annealing technology but also to improve the flash lamp equipment.

The principal objective of the **International Topical Workshop on Heteroepitaxy of 3C-SiC on Silicon and its Application to Sensor Devices** (HeT-SiC-05), held on April 26 - May 1, 2005, at the Hotel Erbgericht in Krippen, Germany, was to summarize and discuss the most important scientific and technological results achieved. In five sessions, namely "Growth", "Deposition", "Processing and Characterization", "Sensors and Devices", and "Future Directions", 35 specialists from Europe and Japan presented and discussed their results and agreed on further efforts to continue this work – for example, the deposition of topical semiconductor materials like zinc oxide (ZnO) and gallium nitride (GaN) on epitaxial 3C-SiC/Si layers.

This report collects selected outstanding examples of the work performed within the frame of the FLASiC project but also other work performed in adjacent fields. In particular it is remarkable that the contribution *"Luminescence of ZnO thin films grown by pulsed laser deposition on 3C-SiC buffered Si*" is the result of spontaneous co-operation between participants of the workshop who had formerly been strangers! This has to be considered a particularly noteworthy success of the meeting and outcome of the FLASiC project.

We would like to express our thanks to the sponsors, and especially all un-named people at the venue, Erbgericht Krippen, and Forschungszentrum Rossendorf, who were involved in making this workshop so successful. Finally, we hope that this Report will foster and support further activities in this very demanding field of research.

Wolfgang Skorupa
(FLASiC project & HeT-SiC-05 Chairman)

Gerhard Brauer
(for the HeT-SiC-05 Organising Committee)

ABSTRACT

This report collects selected outstanding scientific and technological results obtained within the frame of the European project “FLASiC” (**F**lash **LA**mp Supported Deposition of 3C-**SiC**) but also other work performed in adjacent fields. Goal of the project was the production of large-area epitaxial 3C-SiC layers grown on Si, where in an early stage of SiC deposition the SiC/Si interface is rigorously improved by energetic electromagnetic radiation from purpose-built flash lamp equipment developed at Forschungszentrum Rossendorf. Background of this work is the challenging task for areas like microelectronics, biotechnology, or biomedicine to meet the growing demands for high-quality electronic sensors to work at high temperatures and under extreme environmental conditions. First results in continuation of the project work – for example, the deposition of the topical semiconductor material zinc oxide (ZnO) on epitaxial 3C-SiC/Si layers – are reported too.

KEYWORDS: beta-silicon carbide, biocompatibility, biosensor, doped metal oxide, epitaxy, flash lamp annealing, heterostructure, high-temperature device, hotplate, ion implantation, luminescence, magnetic ion, misfit defect, pulsed laser deposition, resonator, sensor, silicon carbide, simulation, stress, surface melting, zinc oxide

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Selective growth of 3C-SiC on various-patterned Si substrates

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Abstract. Epitaxial growth of 3C-SiC on Si substrates has been studied for many years, however important issue is how to reduce the high density of interfacial defects between them. Channel epitaxy is the growth the film on small channeled window and related to selective growth. Channel epitaxy of 3C-SiC grown on the seed 3C-SiC previously deposited on patterned Si substrates was achieved via CVD using hexamethyldisilane (HMDS). Materials of the mask were also key to archive channel epitaxy. Thermal oxide, silicon nitride and thin SiC mask were tried. Thin SiC was effective mask to achieve the selective growth. Selective growth then was demonstrated at 1350 ˚C. The smooth surface morphology was observed on both the channel regions and the ELOG regions at the growth temperature of 1350 ˚C. Scanning electron microscopy revealed coalescence of the laterally growth in the channel epitaxial growth of 3C-SiC.

INTRODUCTION

Cubic silicon carbide (3C-SiC) on Si substrate is an expected material for high mobility devices because of homogeneous effective mass in any direction. It has been needed to grow high quality of 3C-SiC films using heteroepitaxial growth on foreign substrates. 3C-SiC has been grown epitaxially on Si substrates for many years [1]. However, a large lattice mismatch induced a large number of defects such as misfit dislocations, twins, stacking faults and threading dislocations at the SiC/Si interface. Channel epitaxial growth of 3C-SiC on patterned Si substrates is one way to resolve this problem. This method based on seeded growth in narrow micron size channel and epitaxial lateral overgrowth (ELOG) process by using an appropriate mask material to prevent the propagation of threading dislocations originating from the 3C-SiC/Si interfaces. Therefore, lateral overgrowth of a 3C-SiC layer until coalescence results in a 3C-SiC layer of low defect-density material. Microchannel epitaxy (MCE) followed by ELOG technique for GaAs on Si is reported [2]. The technique has been successfully applied to grow 3C-SiC on Si. The above work was done on Si (100) [3, 4] substrates and Si (111) substrate [5]. One big issue of 3C-SiC on Si(100) is the appearance of APB's (APB=Anti-Phase Boundary). The formation of APB's for heteroepitaxial growth of (100) plane zinc blend structure on the (100) plane of diamond structure is well known. The Si (111) plane is preferable to avoid the APB's in 3C-SiC (111), because (111) substrate is the polar face of 3C-SiC.

This paper reports a promising technique of 3C-SiC on patterned Si substrates by applying microchannel epitaxy. The following sections describe the experimental parameters necessary to achieve a 3C-SiC film via MCE and ELOG. The main factors affecting MCE were temperature of growth, choice of mask material, thickness of mask, orientation of substrate, mask-to-window ratio, influence of an etchant (e.g. HCl), etc. The use of HCl on growth influences the surface morphology.

EXPERIMENTAL PROCEDURES

The MCE of 3C-SiC film on Si substrate was achieved. The substrate used is (111)-oriented silicon, previously patterned by depositing a SiO_2 layer of an approximate thickness of 0.9 μm as the mask followed by conventional photolithography techniques. The windows of ridges oriented mostly along the <110> directions. Figure 1 shows the schematic of the fabrication procedure for MCE. An initial carbonization procedure was performed using 1 sccm propane in 3 slm H_2 carrier gas at 1250 ˚C for 2-3 minutes. The seed 3C-SiC layer on Si exposed through windows was grown using the standard 3C-SiC CVD process as shown Fig. 1(b). The growth temperatures of the seed 3C-SiC layer were 1250 ˚C and 1350 ˚C, respectively. The 3C-SiC layer was grown by a cold-wall, horizontal, atmospheric pressure chemical vapor deposition using hexamethyldisilane (Si2(CH3)6: HMDS). Further details of the CVD growth process have been published earlier [6]. In this CVD process, epitaxial growth starts from the seed in a narrow channel region up to SiO_2 mask as shown in Fig.1(c). Once the epilayer reaches to the top of the SiO_2 layer, epitaxial lateral overgrowth (ELOG) starts as shown in Fig. 1(d). Finally, coalescence of the laterally extended epilayer is completed as is shown in Fig. 1(e).

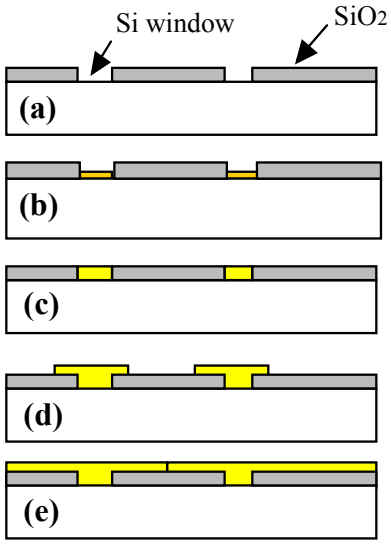

Fig. 1. Schematic procedure of channel epitaxial growth on Si(111) substrates. (a) patterned SiO_2 on the Si substrate, (b) thin SiC seeded region, (c) epitaxial growth on channeled region of Si window, (d) over growth on the SiO_2 mask, and (e) coalescence of the laterally grown layer on the mask.

Another approach is epitaxial growth from the column structures. This approach has many names such as Pendio Epitaxy, Cantilever epitaxial growth, air-gap epitaxy, and so on [7-10]. In our case, a final epilayer was formed on the air-bridge region. Figure 2 shows the schematic of the preparation of the substrate and the growth procedure. The thin seed 3C-SiC layer on Si exposed through windows was formed by carbonization using flows of small amount of C_3H_8 and HCl as shown in Fig. 2(a). In this step, a small amount of HCl flow was

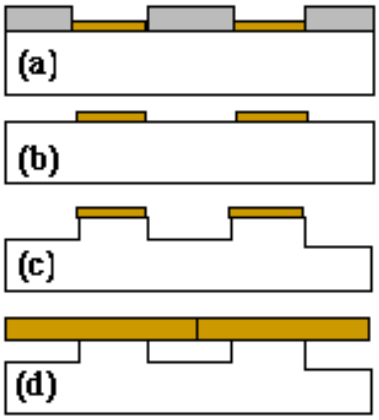

Fig. 2. Schematic procedure of epitaxial lateral overgrowth on Si column structures. (a) thin SiC seed region, (b) removal of SiO2 mask (c) deep etching of peripheral part of SiC mask and (d) coalescence of the laterally oextended layer on the mask.

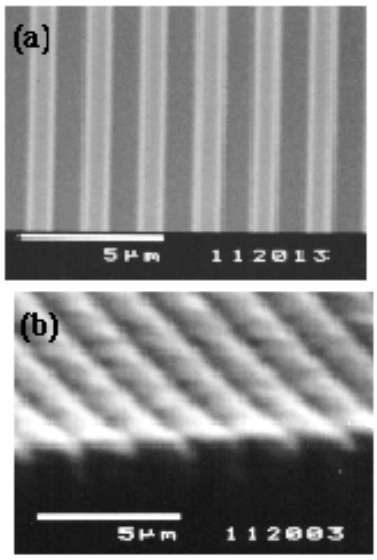

Fig.3 a) original line and space pattern on Si substrate, b) SiC grown layer

used to prevent the unwanted nucleation of SiC on Si. And the seed 3C-SiC layer with 100nm thickness was grown on the initial thin SiC layer at 1250 ˚C and 1350 ˚C, respectively. In this step, a small amount of HCl was also added to prevent unwanted nucleation on the SiO_2 mask. The SiO_2 mask was subsequently removed by dipping in HF as shown in Fig. 2(b). When the seed SiC was thicker, it was difficult to remove the SiO_2 mask. To create Si columns covered with a seed 3C-SiC layer on top, periphery of the seed SiC was deeply etched by an in-situ etching process as shown in Fig. 2(c). Subsequently the re-growth of 3C-SiC was carried out using a 3C-SiC CVD growth process at the growth temperature (~1350 ºC) as is shown in Fig. 2(d). During the growth of SiC, the flow rate of HMDS was 0.2-0.3 sccm. HCl gas, with a flow rate of 1.0-4.0 sccm, was used for in-situ cleaning of the substrate. The flow rate of hydrogen as the carrier gas was 3-7 slm. Each epitaxial 3C-SiC film was deposited for 60 minutes. Nominal growth rate on Si(111) substrate was approximately 3μm/min.The ELOG structure of 3C-SiC was observed using optical microscopy and scanning electron microscopy (SEM) – see Fig. 3. Raman spectroscopy is applied to characterize the stress analysis of the epilayer – for results see Fig. 11.

RESULTS AND DISCUSSION

Microchannel epitaxy

Microchannel epitaxial growth of 3C-SiC on patterned Si was successfully achieved by using HMDS as shown in Fig. 4. Windows of 1 μm width with a periodicity of 1 μm were formed. After the growth, lateral overgrowth on the SiO_2 layer was confirmed as is shown in Fig. 4b. However, it was difficult to obtain single crystalline films at lower temperatures (~1250 ˚C). We have suggested MCE using SiO_2 mask, though the mask caused some unwanted nucleation on its surface and the SiO_2 mask began to peel off at temperatures above ~1250 ˚C [4]. When the Si_3N_4 mask was used, the mask was peeled off during the growth. These factors restricted the experimental conditions of deposition using patterned SiO_2 and Si_3N_4 masks.

On patterns that consisted of closely spaced stripes, highly selective deposition was obtained. Lateral overgrowth was also observed in these patterns. Lateral-to-vertical (L/V) growth rates of up to 2 have been observed. The L/V rate depends on the pattern size and shape. This is controlled by the availability of growth species at the site of growth. For closely spaced stripes, coalescence occurs after a relatively short time of growth. The subsequent growth is vertical. In this case, L/V is rather small (<1). For more widely spaced stripes, L/V is larger as growth species continue to be available at the laterally growing fronts until coalescence occurs at a later stage. An additional feature that is influenced by the stripe spacing is the faceting of stripes. The shape of the faceted crystal depends on the stripe width and the spacing between the stripes which are also seen in Figure 4. For closely spaced stripes, the cross-section of the widely spaced stripes is a trapezium.

Stripe spacing also affects selectivity. For widely spaced stripes (>10 mm), long time growth results in the formation of unwanted nuclei on the mask in-between the windows. Therefore, the spacing between the windows needs to be optimized to give the best selectivity

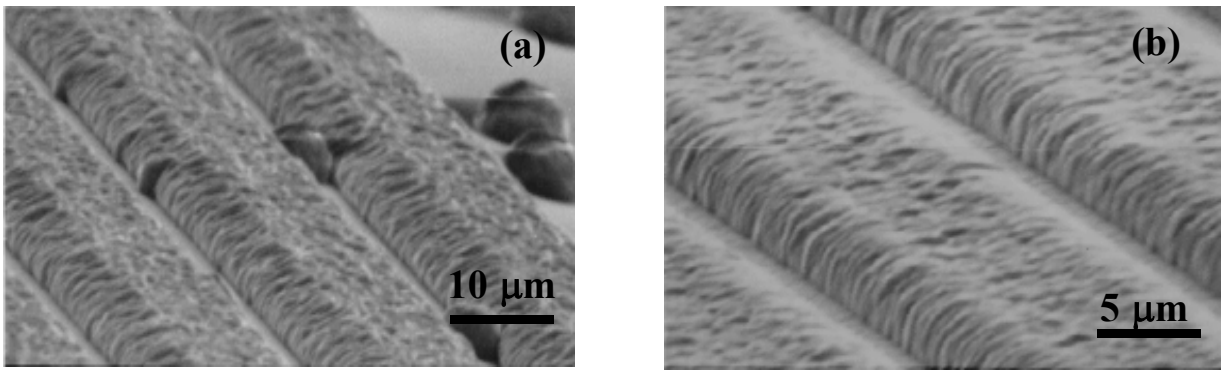

Fig. 4 . Selectively grown SiC stripes at 1150oC: a) 10 μm spacing and 10 μm window width; b) 20 μm spacing and 20 μm window width.

and a high L/V rate. As will be discussed later, the pattern-spacing influences coalescence also. The shape of the window significantly influences the grown crystal. Conventionally, stripes have been used in most experiments. However, the use of circular or square windows leads to a large area of the mask remaining uncovered (Figures 5a and 5b). It was also noted

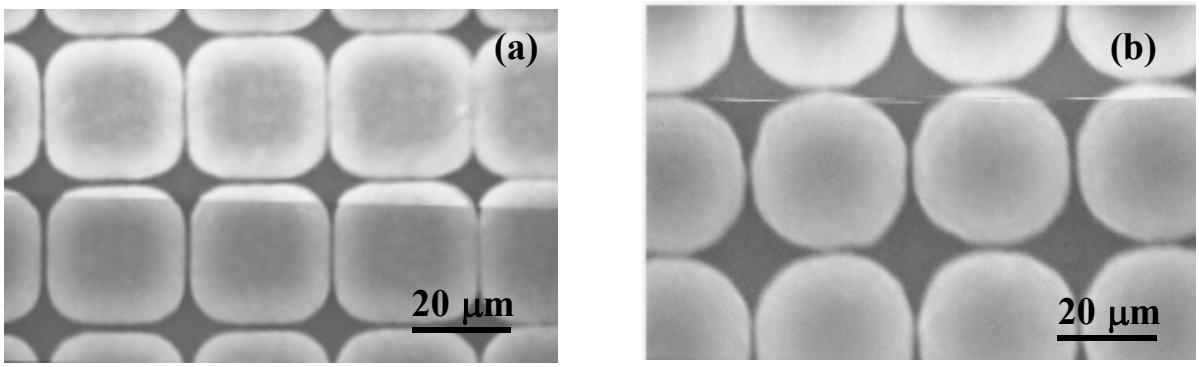

Fig. 5. Growth of SiC on: a) square windows; b) circular windows.

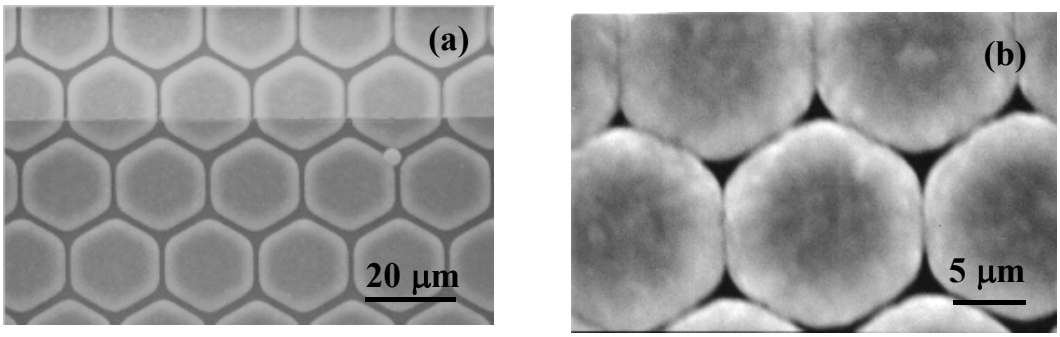

Fig. 6. a) Lateral overgrowth on hexagonal windows with about 10μm sides and spaced 10 μm apart; b) an enlarged view of a sample with hexagonal windows about 5μm sides and spaced five μm apart.

that the square patterns became rounded at the edges as lateral overgrowth progressed and for very small shapes (< 5 mm), there was no difference between square and circular windows after a few hours of growth. In either case, a large area of the mask remained uncovered by the lateral overgrowth. By choosing hexagonal windows, this problem seems to be almost eliminated. Because epilayer grows on Si (111) substrate and the growth rate along <110> direction is faster than the others. The acute corner of hexagonal pattern was aligned to the <110> direction of the substrate. In this configuration of the mask, at the epilayer from a hexagonal patterned area it seems that the advancing growth fronts continue to maintain the easy direction of the growth. By choosing the size and spacing of the hexagonal windows appropriately, the laterally overgrown parts are able to coalesce easily. This behavior is seen in Fig. 6a+b. In these figures, the white areas are the laterally overgrown regions, whereas the darker central regions are the areas growing within the window.

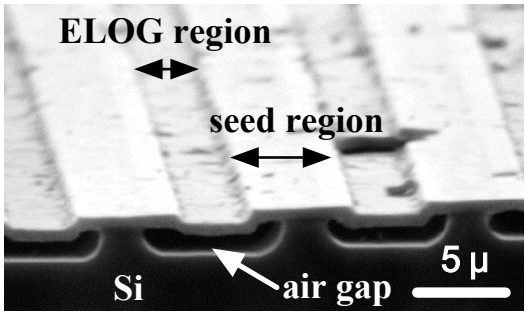

Fig.7 SEM picture of 3C-SiC on air brige

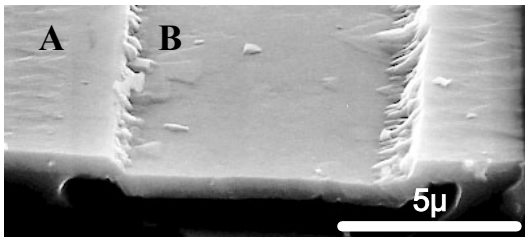

Fig.8 SEM picture of 3C-SiC on air brige.
A) seed region and B) ELOG region.

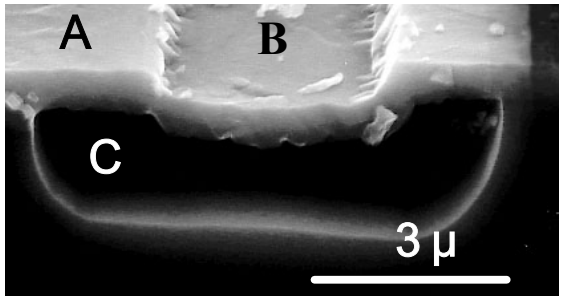

Fig.9 Enlarged SEM picture of air brige region.
A) seed region ,B) ELOG region and C) air-gap.

Epitaxial lateral overgrowth on the air-gap structure

To avoid the SiO_2 layer, the growth from the seed region on top of the column structures was performed at high temperature (~1350 ˚C). Growth rate along <111> seems to be lower than that along <110>. Figure 7 shows the SEM micrographs of epitaxial 3C-SiC on the columnar seed 3C-SiC region at 1350 ˚C on line patterns having a

widths of 5 μm and being coupled with separation distances of 5 μm. It was observed that the ELOG region was lower than the seed region. The lateral growth from the side face of the Si column carbonized under the seed region might compose the lower ELOG region. The surface of the 3C-SiC layer on the seed 3C-SiC grown at 1350 ˚C showed triangular facet morphology as shown in region A in Fig.8. However, the smooth surface morphology was obtained on the ELOG regions at the growth temperature of 1350 ˚C as shown in region B in Fig.8. The triangular facet might be directly related to the Si (111) substrate, however, the smooth morphology of the ELOG region which was extended from the seed region relates to the air gap underneath.

An enlarged air-gap region under the ELOG 3C-SiC layer is shown in Fig. 9. The lateral growth is faster than the vertical growth on the (111) plane. As the flow rate of the H_2 carrier gas increased from 4 slm to 7 slm, the 3C-SiC growth rate in the <111> direction decreased from about 3.4 μm/hr to 0.8 μm/hr. When the flow rate of the H_2 carrier gas was increased during the re-growth to form the ELOG, the surface smoothness of the 3C-SiC epilayer became better. The original Si column was etched during 3C-SiC growth, so the column shrank during growth. The etching rate depends on the orientation of the Si substrates. The etching rate perpendicular to the (111) plane is faster than in other direction. As a result, the air-gap under the ELOG region was formed. By arranging lines and spaces in the original Si (111) substrate, air-bridge supporting 3C-SiC was formed as is shown in Fig.10. Finally free standing 3C-SiC is formed.

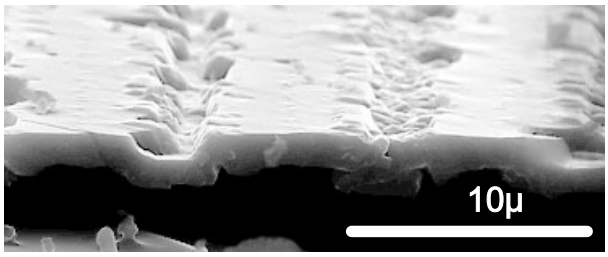

Fig.10. Free-standing 3C-SiC on Si(111).

The surface morphology of epitaxial 3C-SiC depended on the flow rate of HCl on the re-growth as well as the flow rate of H_2 carrier gas. The effect of in-situ etching by HCl during the etching process and the re-growth process can construct the free-standing 3C-SiC layer separated from the Si substrate and shown in Fig. 7. With regard to the surface roughness, the ELOG region was smoother than the seed region in the backside of the free-standing 3C-SiC. The use of such a structure may result in the lower stress of the 3C-SiC

epilayer because of the lower effect of thermal expansion at temperature-fall. Optimization of

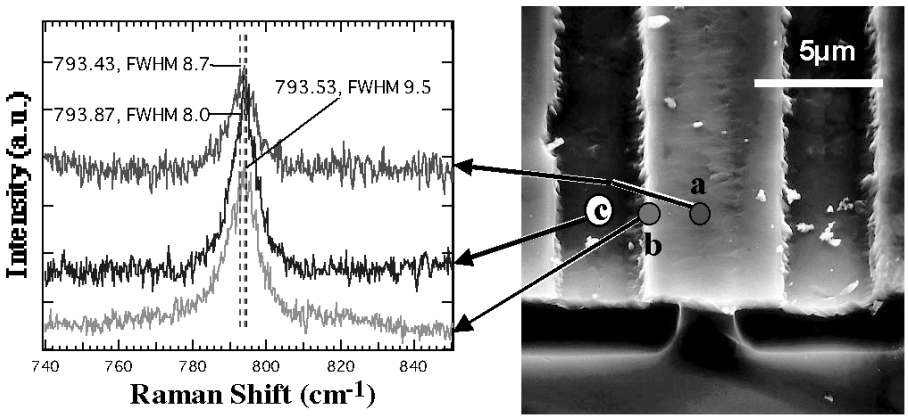

Fig.11 Raman spectra from three regions. a) seed column,b) boundary between column region and ELOG region, and c) ELOG region.

the epitaxial growth of 3C-SiC on air-bridge structure should eliminate any undesirable defects. The full width at half maximum of the TO phonon of Raman spectra at around 793 cm-1 at the ELOG region was less than that at the seed region as shown in Fig.11. This indicates that the crystallinity of the 3C-SiC layer on the ELOG region is superior to that of the seed region. At the ELOG region, the TO phonon peak is shifted to a lower wavenumber, which means that the ELOG region has tensile stress.

CONCLUSION

An investigation of growth conditions of epitaxial lateral overgrowth of 3C-SiC on Si was achieved. The key experimental parameters were the growth temperature of the seed 3C-SiC previously grown on Si substrate and the flow rate of H_2 carrier gas during the re-growth. The seed 3C-SiC layer grown at 1350 ˚C results in the smooth surface of ELOG epitaxial 3C-SiC after re-growth. The increase of the H_2 carrier flow rate during the re-growth improves the surface morphology of ELOG epitaxial 3C-SiC, though the growth rate along the <111> direction decreases on the (111) plane of Si substrate. The crystallinity of the 3C-SiC film on the ELOG region was superior to that on the seed region according to the Raman spectra. In this ELOG approach, 3C-SiC on air-bridge structure was obtained.

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Modelling of flash lamp processing of SiC-on-silicon heterostructures

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Abstract: Flash lamp annealing has been shown to be a promising tool in the preparation of high quality silicon carbide-on-silicon heterostructures and in other applications. As in other steps in the processing of semiconductor materials the specification of processing conditions for a particular substrate is of key importance. In our work we describe the development of a thermal model for flash lamp processing of 3C-SiC and silicon multilayer heterostructures, on silicon substrates and use the results to explain and predict observable phenomenon, including carbon transport and the evolution of thermally induced stress. The model has also been used to predict the effect of carbon implantation for the use of expanding the experimental window. The availability of accurate process models not only avoids the need for repeated experimental determination of process conditions but also allows the optimization of structures and process conditions to be carried out in simulation.

1 Introduction

Silicon carbide substrates are attractive for the fabrication of power and high temperature devices. However, currently available substrates have relatively high defect densities which limits the size of devices that can made, so there is a need to improve substrate quality [1]. Although most attention has been given to the hexagonal (4H and 6H) polytypes, cubic 3C-SiC is attractive as it in principle has the highest mobility of all the SiC polytypes. Epitaxial growth of 3C-SiC on a silicon substrate is a practical method of preparation, but the ultimate layer quality is strongly dependent on the quality of the film during the very early stage of the growth. Flash lamp annealing of 3C-SiC on silicon layers (the FLASiC process) has been shown to improve the crystal quality of a thin SiC on silicon layer to act as a seed for the subsequent growth of a high quality epitaxial SiC layer [2]. The melting of the silicon below the SiC layer has been identified as a key step in the process.

This paper reports the development of a set of tools for the modelling of the flash lamp process. These include a thermal model for flash lamp processing to predict the temperature distribution within the substrate during processing and the extent of melting below the SiC layer. The model is based on solving the heat flow equation with a source term, which includes the mechanism of energy coupling from the flash lamp pulse to the substrate. The model allows virtual experiments to be performed to explore process conditions and is a step towards calculating stresses in the wafer during processing. In addition, the model can be applied to other applications of flash lamp annealing, such as millisecond annealing of ion implants in silicon [3] and the crystallization of amorphous silicon on glass substrates [4].

2 Thermal and optical model

A model has been constructed for heat flow in the wafer during the FLASiC process [5]. The model couples calculation of the spatial absorption of energy from the flash lamp equipment to heat flow analysis. As the process includes melting of the solid silicon below the SiC layer, the model must allow for a change of state. The model is based on the enthalpy equation:

$$\frac{\partial}{\partial t}(\rho h) = \frac{\partial}{\partial x}(K\frac{\partial T}{\partial x}) + S \qquad (1)$$

where T is the temperature, h is enthalpy, ρ is the density, K is the thermal conductivity, x and t are the distance and time coordinates respectively, and S is a source term representing the absorption of energy from the flash lamp. The enthalpy equation (1) has been solved numerically, using a one-dimensional method of finite elements to discretize the process. Taylor expansions were used to develop an explicit discretized enthalpy equation and solved using a combination of an Euler method and a Crank-Nicolson scheme.

Knowledge of the optical system is important in determining the distribution of energy absorption in the wafer during the flash lamp pulse. This distribution forms the source term, S, in the enthalpy equation (1). In the experimental work a pulse of 20 ms FWHM (full width half maximum) has been used for all samples, the characteristics of which have been measured experimentally. The optical system comprises the inert gas atmosphere of argon over the sample, the SiC layer, possibly a liquid silicon layer and the bulk silicon. The optical properties of the layers can be characterized by a complex permittivity which is temperature and wavelength dependent. The optical properties of solid silicon, liquid silicon and SiC are taken from published data [6,7,8].

The optical analysis must take into account the multiple reflections and transmissions in the wafer, which is accomplished using a matrix method [9]. A matrix representing each layer is used and this effectively treats each layer as a single interface. We then can calculate the overall reflectivity and transmission into the solid substrate of the flash lamp as a function of the depth of the molten silicon layer. The results shown in Fig. 1 are for a 35nm SiC layer on a 0.52 mm thick silicon substrate.

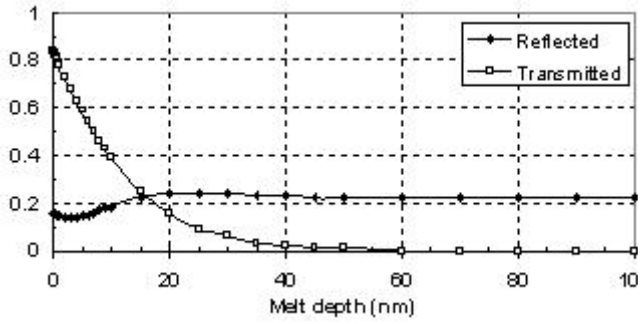

Fig. 1. Reflectivity at the upper surface and transmission into the solid substrate for a typical FLASiC wafer as a function of melt depth.

3 Experimental verification

3.1 Calibration

The energy per unit area delivered by the flash lamp equipment, which depends on the energy stored in the capacitors before the pulse, is not absolutely known so it is necessary to calibrate the FLASiC equipment. This has been done using bare silicon samples for a range of preheats and wafer thicknesses, using the well-defined threshold of the onset of melting as a calibration point. Simulations have confirmed the expected square law dependence of the pulse intensity on the voltage to which the capacitors are charged. The energy density of a 20 ms pulse was found to be:

$$E(J/cm^2) = (12 \pm 1.75) \times (kV^2) \qquad (2)$$

3.2 Results for FLASiC

The model was used to predict the effects of the original FLASiC process on samples with a 35 nm SiC layer and 0.52 mm silicon substrate. In the case considered a preheating of 800°C and a pulse length of 20 ms was used. The thermal profiles in the wafer during an 82.5 J/cm^2 pulse are shown in Fig. 2. There are significant temperature gradients through the thickness of the wafer, with a maximum temperature difference of about 400 ºC under the present conditions. The duration of melt is approximately 4 ms.

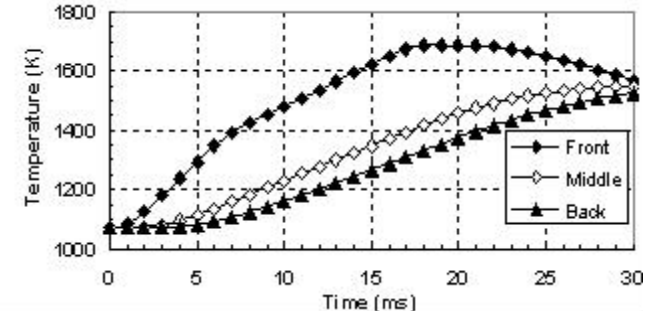

Fig. 2. Thermal profile during a flash pulse showing the temperature at various points through the thickness of the wafer.

A plot of predicted maximum melt depth of silicon against energy density is shown in Fig. 3, along with experimentally obtained values from depth profiles taken from marker experiments with antimony implants. Although the accuracy of the measured melt depths is limited by the depth resolution of the measuring technique and uncertainty about the morphology of the melt interface, the experimental and simulated results for the threshold for the onset of melting and the subsequent growth of the melt zone are consistent. For a 1% increase in pulse energy, the melt depth can increase by several orders of magnitude.

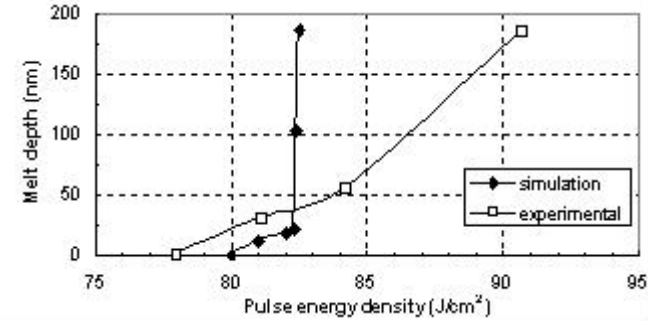

Fig. 3. Predicted melt depth and experimental results using antimony implants.

The melting and re-growth of silicon is an important part of the FLASiC process for annealing SiC layers. The rate of re-growth depends on the degree of undercooling [10]. The regrowth kinetics were incorporated into the model and, as expected, in the time regime under consideration the correction was negligible. Related nucleation rates under typical FLASiC conditions are negligible [11,12]. Consequently, regrowth of the silicon will be epitaxial and of high quality. This is confirmed by the TEM observations, Fig. 4.

Fig. 4. TEM of a processed sample. TP represents trapezoidal protrusion.

From TEM observations, part of the SiC layer in the original structure appears to have dissolved and in certain areas the SiC layer shows an increase in thickness through the growth of trapezoidal structures.

3.3 Results for i-FLASiC

An improved structure, i-FLASiC, has been devised, principally to minimize bending and improve layer uniformity, and involves growing an additional silicon layer on the SiC, followed by a further SiC layer on the silicon [13]. The original aim was to melt the silicon over-layer without any significant melting of the silicon substrate, thus minimizing wafer bending. Simulations have been performed on a typical i-FLASiC structure of 60 nm SiC/200 nm silicon/65 nm SiC/silicon substrate. Calculations shown in Fig. 5 and we also predict that the melt duration is approximately 10 ms. We also see that the process window is impractically small.

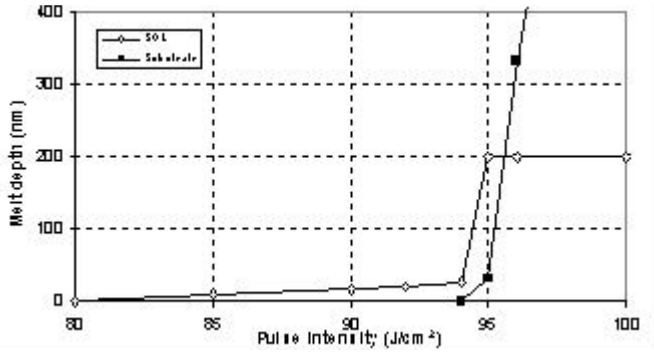

Fig. 5. Predicted melt depths in the silicon-over-layer and bulk silicon substrate.

4 Mechanism of the FLASiC process

The dissolution and regrowth of SiC is central to FLASiC processes. SiC in contact with the liquid silicon will dissolve, increasing the carbon content of the liquid silicon. The extent of the changes in thickness of the SiC layers observed in the TEM micrographs cannot be explained by the temporary transfer of carbon to the liquid silicon due to the very low solubility of carbon in silicon [14]. Carbon is being transported through the liquid silicon from areas where the SiC is dissolving to areas where the SiC is growing. We can describe this movement of carbon quantitatively by solving the solute diffusion equation. We can calculate diffusion of carbon in liquid silicon over a given length and we obtain the rate of growth as a function of the source-sink distance, as shown in Fig. 6 [15].

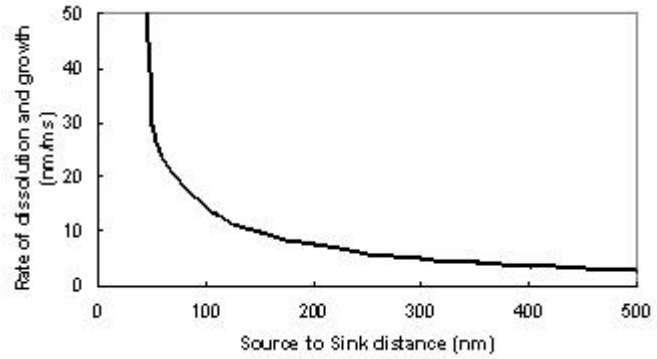

Fig. 6. Rate of dissolution and growth of SiC for different source-sink distances.

For FLASiC, calculations show that the observed size of trapezoidal protrusions is consistent with the lateral distance over which carbon is transported. We believe some areas dissolve due to higher defect density causing supersaturation of carbon and preferential dissolution. The preferential growth on the higher quality regions of SiC is advantageous for overall layer

quality. For the i-FLASiC process, driven by the large thermal gradient, carbon transport is from the upper to the lower SiC layer. Taking the source-sink distance to be 200 nm, a typical thickness for the silicon overlayer, we see that we can grow approximately 74 nm of SiC in 10ms. These results are consistent with the observed TEM data, and that growth is controlled by the carbon transport.

The shape of the trapezoidal protrusion can be explained by the faster growth on particular crystallographic planes, as has been observed in the study of the spontaneous growth of 3C-SiC crystallites in liquid Si under conditions which are similar to those found transiently in FLASiC [16].

5 Melt stop analysis

We have studied a new method of controlling the depth to which silicon will melt into the substrate. From the Si-C phase diagram, implanting carbon into the silicon increases the melting temperature of the silicon. This led to experiments of implanting C into the silicon below the SiC layer for FLASiC and below the embedded layer for i-FLASiC. Implantation increases the melting temperature of the silicon to a depth of around 800 nm. Melting behind the melt stop is inhibited by the lack of a seed from which liquid silicon can grow from. Silicon below the melt stop will require superheating of around 100 ˚C [17] for homogeneous nucleation. This 100 ˚C provides a buffer in which can heat the silicon without further melting.

This has been incorporated into the thermal model. Experimental and simulation results have been compared for a wafer of 18 nm SiC/0.5 mm Si substrate with 850 ºC preheat and a 3 ms pulse. The experimental work was done using an optical microscope. Both are shown in Fig 7. The melt stop has given us a range of flash energies for which melting of silicon occurs to a controlled depth (3.1 kV to 3.5 kV in this case). This is a relative power window of 13 % which is much larger than the lateral variations pulse intensity.

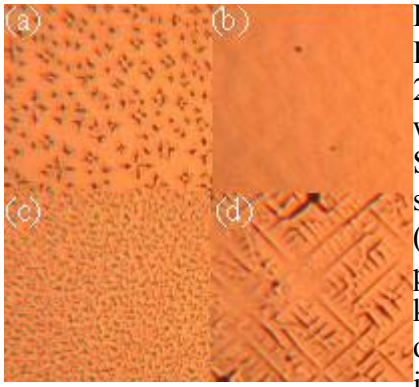

Fig. 7. Optical microscope observations for melt stop in FLASiC sample. Each figure represents a 0.5 mm square. (a) 2.9 kV (Onset of melting). Simulations predict onset of melting will occur at 2.95 kV. (b) 3.4 kV (Uniform melting of silicon). Simulation predicts melting of about 60 nm. Melting increases slowly as temperature is rising, 66 ºC above melt temperature (c) 3.5 kV (Onset of melting of silicon below the implanted profile). Simulation predicts melting of bulk silicon at 3.52 kV. Temperature is now over 100 ºC above the melting point of silicon. (d) 3.1 kV (Non-implanted sample). Deep melting is already occurring in the substrate.

We have performed similar calculations for the melt stop in i-FLASiC. Simulations predict that we will achieve good results in the energy range of 3.25 kV and 3.55 kV, with more energy resulting the deep melting. This closely matches the 3.2 kV and 3.5 kV found experimentally.

Another melt stop was envisaged based on implanting Ge below the SiC layer in FLASiC, thus lowering the melting temperature of silicon. Simulations predicted that the method would be successful for lower implantation energies and was confirmed by experimental data. We also predict that Ge would work well for i-FLASiC structures and could be used in conjunction with the carbon melt stop.

6 Thermo-Stress model

The transient thermal gradients experienced by the FLASiC wafers can cause severe stress in the wafer. Under certain flash lamp conditions wafers can shatter or crack and large stresses can also cause the defect density to increase. The stress analysis is performed using Abaqus finite element using temperature profiles produced by the thermal model. Meshing is used such that bifurcation behaviour can be captured. Bifurcation is when wafers no longer bend in an axis symmetric.

We performed thermal stress and edge deflection calculation using the thermal profiles in Fig. 2. Results shown in Fig. 8 show the deflection of two points on the circumference of the wafer. We observe bifurcation behaviour and that the maximum tensile stress in the wafer is 136 MPa. This is well below the fracture strength of silicon (≈300 MPa [18]) but is well above the yield stress of silicon of 1 MPa [19]. The creation of dislocations deep into the substrate seen by TEM show that yielding can take place.

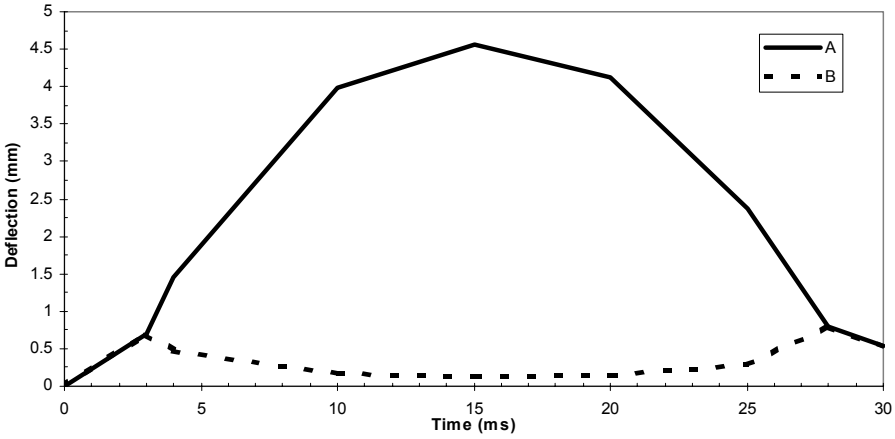

Fig. 8. Deflection of two edge points on the circumference of the wafer

7 Conclusion

This paper reports an approach to modelling the flashlamp irradiation of 3C-SiC on a silicon substrate. The model incorporates an accurate finite element computational scheme, combined with a sophisticated optical model, resulting in predictions in good agreement with experimental data. These results have been used to predict the liquid phase epitaxial regrowth of SiC from a carbon saturated silicon melt. Predictions of morphology are in good agreement with TEM observations. Temperature dependence on the melting point of silicon has been included to model the effect of implantation of carbon into the silicon substrate. The model is able to predict experimental windows of controlled substrate melting which closely agree with observed phenomenon. We have used transient thermal profiles through the thickness of the wafer to predict the stress and curvature evolution of a substrate during annealing.

The flexibility of the simulation tools allows the modelling of alternative material systems and processing cycles. Investigation of the crystallization of thin amorphous silicon films and the processing of plain silicon structures has already produced valuable results.

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Stress design in 3C-SiC/Si heteroepitaxial systems

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Abstract

Germanium modified silicon surfaces in combination with the two step growth technique allows to reduce the internal stress in the SiC/Si heterostructures independent on the substrate orientation and the growth technique, if the SiC/Si structure is tensile stressed if germanium is not used. The developed method can be used as an alternative route for stress reduction and improvement of the crystalline quality in heteroepitaxial systems with extremely large lattice and thermal mismatches.

Introduction

The stress state in heterostructures is one of the important design parameters in the technology of heterostructures. The residual stress affects the manufacturability of the processed wafers as well as the defect densities and, therefore, the device related properties of the grown heterostructures. Generally, different types of defects are generated if the stress in the heterostructure exceeds a critical value. The defects formed during the relaxation of the lattice distortion have a detrimental impact on the material properties. For example, they led to a lowering of the carrier mobility, the diffusion length of the minority carriers and the breakdown voltage. The optical properties are influenced due to the impact of the defects on the band structure and, therefore, on the absorption coefficient as well as on the recombination velocity of the minority carriers in the regions where defect are existing. The mechanical properties are affected by the internal elastic fields formed by the zero (point defects), one dimensional (dislocations), two dimensional (stacking faults surrounded by dislocations) and three dimensional defects (voids or secondary phases). They change the elastic moduli and causes additional losses due to internal friction.

The stress in heterostructures can be reduced by applying the following methods: (1) low deposition temperatures, (2) compliant substrates: for example, thin Si, buffer layers, SOI, porous layers, intentional and unintentional voids; (3) local or selective epitaxy: for example, checkerboard substrates, lateral overgrowth, nanoheteroepitaxy; (4) micro- and nanostructured surfaces in form of undulant surfaces, porous layers, nanostructuring; (5) buffer layer and dislocation filtering; (6) annealing of the heterostructures: for example, thermal and flash lamp annealing.

The aim of the current presentation is to demonstrate that germanium modified silicon substrates are a suitable alternative technique to reduce the internal stress in SiC/Si heterostructures.

Experimental

For the investigation of the influence of surface modification by germanium deposition 3C-SiC was grown on Si(111) and Si(100) p-type boron doped substrates. The wafer resistivity was 10 Ω cm. The 3C-SiC epitaxial layers were grown using four different methods: (1) solid source molecular beam epitaxy (SSMBE) on Si(111) substrates at low temperatures *(method 1)*, (2) chemical vapour deposition at low temperatures in an ultra high vacuum chamber on Si(100) substrates *(method 2)*, (3) atmospheric pressure chemical vapour deposition at high temperatures resulting in compressive stressed layers on non modified Si(100) wafers *(method 3)*, (4) atmospheric pressure chemical vapour deposition at high temperatures leading to tensile stressed layers on non modified Si(100) wafers *(method 4)*. All 3C-SiC layers were grown using a two step method. The first step consists in a carbonization procedure allowing the incorporation of germanium into the SiC/Si heterointerface [1].

Method 1 consists of the following process steps: (1) hydrogen plasma cleaning of the silicon substrates, (2) annealing at 750°C for 1 h in the deposition chamber, (3) 0 to 2 ML Ge deposition on the (7x7)-Si reconstructed Si surface at 325°C by electron beam evaporation (ML with respect to the Si(111) surface), (4) deposition of 6 ML C at 325°C, (5) gradually increase of the substrate temperature in steps of 50 degree up to the final growth temperature for SiC epitaxy, (6) the SiC deposition started at 850 °C with a growth rate of 1 nm/min under Si rich conditions and continuously operating Si and C sources. Growth was carried out at 1000°C up to a thickness of 120 nm and 300 nm.

For the 3C-SiC epitaxial growth by methods 2 to 4 after a RCA cleaning of the substrate with a finishing dip in buffered HF the substrates were transferred into the growth chamber of the molecular beam epitaxy equipment. After an annealing step for 1 h at 400°C and 750°C germanium was deposited on the (2x1)-Si reconstructed surface. The Ge amount was varied between 0 and 4 ML (ML: monolayer with respect to the Si(100) surface). After an annealing step at 325°C for 10 min 1 ML carbon was deposited at 325°C followed by an annealing at the deposition temperature for 10 min. Subsequently to the annealing step the substrate temperature was increased with a ramp of 0.5 K/s up to a final temperature of 850°C. Starting with a substrate temperature of 610°C 5 ML carbon was deposited during 40 s. In the moment were the final temperature was reached the heating was stopped and the substrate was cooled down to room temperature and transferred out. As a result of the carbonization procedure a 2 to 3 nm thick 3C-SiC layer was formed. Subsequently, the sample was transferred to different CVD machines in order to grow the 3C-SiC layers. In the case of method 2 the transfer was carried out under UHV conditions without breaking the vacuum. The growth was carried out at 1.3×10^{-3} mbar by using a ethen-silane mixture. The substrate temperature was 1050°C. The thickness of the 3C-SiC(100) layers was 120 nm. A substrate temperature variation was carried out for methods 1 and 2 in order to study the effect of the predeposition temperature. The Ge coverage was chosen to be constant and 1 ML.

In the case of the APCVD procedures (methods 3 and 4) the samples were transferred to the CVD machines by breaking the vacuum in order to grow thicker 3C-SiC layers with a thickness around 5 µm (compressive stressed) or 2.5 µm (tensile stressed). The growth was carried out at 1350°C by using a propane-silane-hydrogen mixture.

All carbonization processes were controlled by *in situ* RHEED with a Staib EK 35R and *in situ* spectroscopic ellipsometry SE 801 from Sentech. The characterization of the epitaxial layer was carried out by µ-Raman spectroscopy and FTIR-ellipsometry. The µ-Raman measurements were performed with a Jobin Yvon T64000 spectrometer in backscattering geometry with an argon-ion laser operating at 488 nm and a spot size of 1 µm. The FTIR-Ellipsometry measurements were carried out with a SE 900 from Sentech. As a

quality criteria for the grown layers the full width of the half maximum of the phonon peaks (FWHMs) or the I_{LO}/I_{TO} ratio were used. From selected samples high resolution x-ray diffraction (HXRD) and transmission electron microscopy investigations were carried out using a TECNAI 20S-TWIN (FEI) microscope. For the TEM investigations the samples were prepared using a standard procedure. This procedure consists of mechanical thinning and Ar^+ milling in a Gatan Precision Ion Polishing system.

Experimental results and discussion

Method 1

Figs. 1 and 2 displays the strain and the FWHMs versus germanium predeposition prior to the carbonization. The 3C-SiC was epitaxially grown by SSMBE. The average residual lattice strain in the 3C-SiC layers grown on Si(111) substrates were determined by using the equations of [2] and the TO phonon positions extracted from the Raman spectra by using a Lorentzian fit.

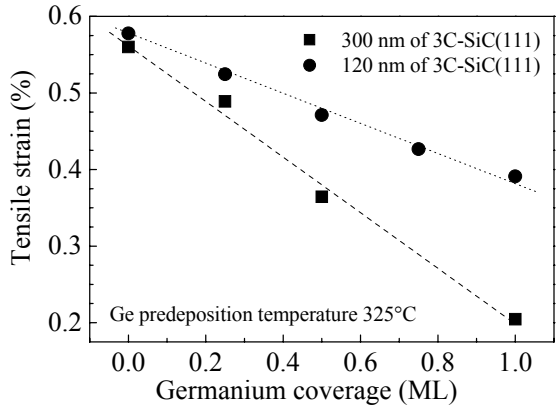

Fig. 1: Tensile strain versus Ge coverage prior to the carbonisation and epitaxial growth on Si(111).

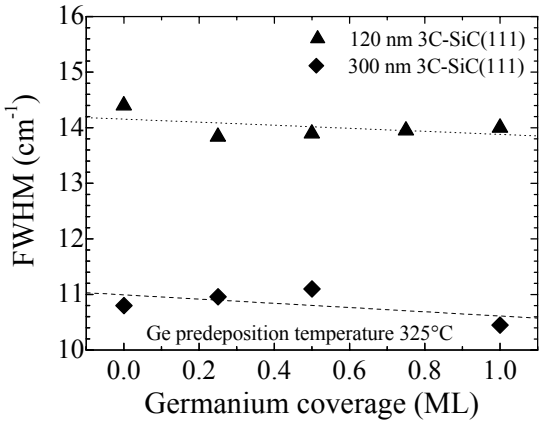

Fig. 2: FWHM of the TO phonon peak versus Ge coverage prior to the carbonization and epitaxial growth on Si(111).

The tensile strain shows a linear decrease in dependence on the Ge coverage prior to the carbonization of the Si(111) substrate. At the same time the FWHMs of the TO phonon peaks decreases with increasing Ge coverage indicating an improvement of the 3C-SiC crystallinity for both thicknesses. Following Figs. 1 and 2 it can be concluded that the modification of the silicon substrate with Ge adds an additional strain relaxation path to the common observed improvement of the 3C-SiC quality with increasing layer thickness. Furthermore, the strain reduction is not associated with a reduction of the crystalline quality caused by an enhanced plastic relaxation by dislocation generation. This is evidenced by the slightly decrease of the FWHMs in Fig. 2. In Fig. 3 the residual lattice strain in dependence on the substrate temperature at a constant Ge precoverage of 1 ML and for a 3C-SiC(111) thickness of 120 nm is displayed. The tensile strain in this graph shows two minima near 400 and 650°C. For high Ge coverages prior to the carbonization, i.e. 2 ML the residual tensile strain approaches the values of the non modified silicon substrate. The FWHMs and therefore the crystalline quality of the grown 3C-SiC layer exhibit a tendency of a linear decrease with increasing Ge precoverages. Consequently, the crystalline quality of the grown layers improves progressively and independent on the residual strain in the epitaxial layer with increasing Ge predeposition. This allows a selection of the optimal predeposition conditions.

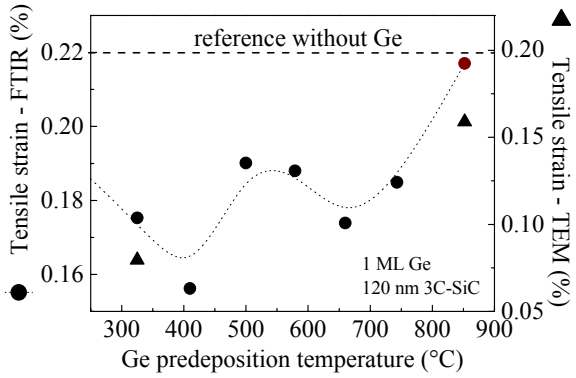

Fig. 3: Tensile strain versus Ge predeposition temperature at 1 ML Ge and a 3C-SiC(111) thickness of 120 nm on Si(111).

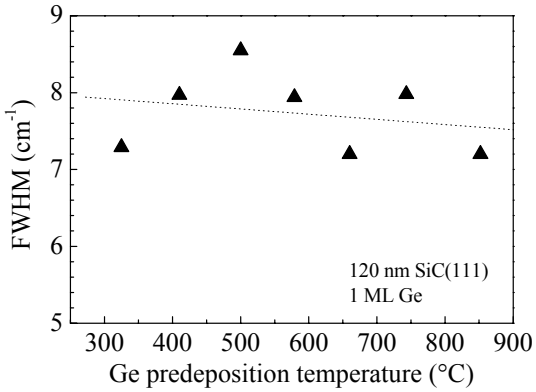

Fig. 4: FWHMs versus Ge predeposition temperature at 1 ML Ge and a 3C-SiC(111) thickness of 120 nm on Si(111).

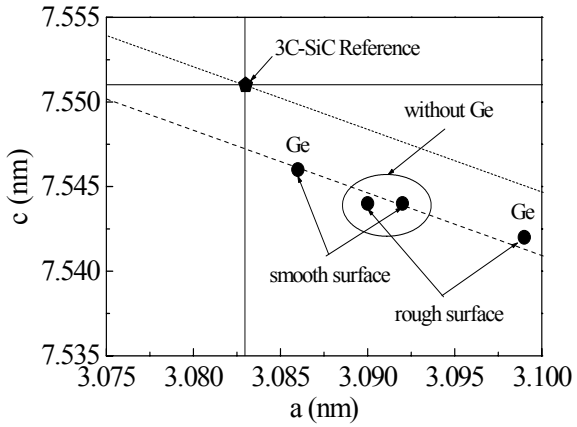

Fig. 5: Out of plane lattice constant c versus in plane lattice constant a of 120 nm 3C-SiC(111) measured with high resolution x-ray diffraction in dependence on different Si(111) surface preparation techniques.

The influence of the surface morphology on the residual strain in the 3C-SiC layer was studied with differently prepared surfaces. The first surface consists of an as etched surface with a nanoscopically rough morphology and hydrogen termination (*rough surface*). The second surface morphology was achieved by annealing the *rough surface* 1 h at 750°C. As a result of the annealing procedure a stepped (7×7)-Si reconstructed surface was formed (*smooth surface*). On both surfaces a 3C-SiC epitaxial layer was grown by SSMBE without and with Ge predeposition. The samples were investigated by HXRD. Fig. 5 shows the obtained results of the in plane a and out of plane c lattice constants in comparison with the values for a single crystal of 3C-SiC [3]. In all cases tensile strained layers were obtained. The *smooth surface* led to a decrease of the residual strain where as in the case of the *rough surface* the stress was observed to increase. So, if a reduction of the tensile stress is desired a flat surface is needed. For biaxial strained layers the lattice distortion in vertical and lateral direction is coupled by the Poisson ratio. None of the investigated samples follows this rule and in all SSMBE prepared samples a hydrostatic pressure is present resulting in a decreasing of the effective volume of the SiC material. This might be due to an increased defect density in the layer, originated from the interface.

Method 2

The strain and the I_{LO}/I_{TO} ratio in the 3C-SiC layers grown by UHVCVD on Si(100) substrates versus the Ge precoverage is shown in Figs. 6 and 7.

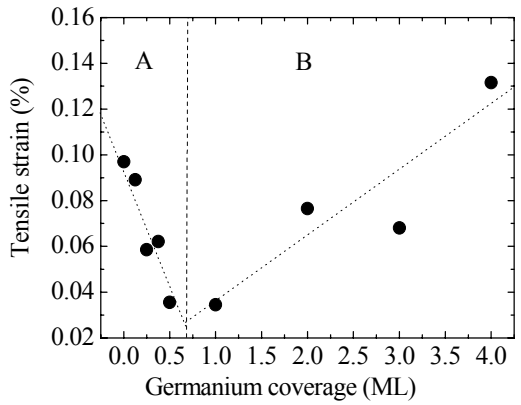

Fig. 6: Residual strain variation versus Ge predeposition prior to the carbonization process and growth on Si(100).

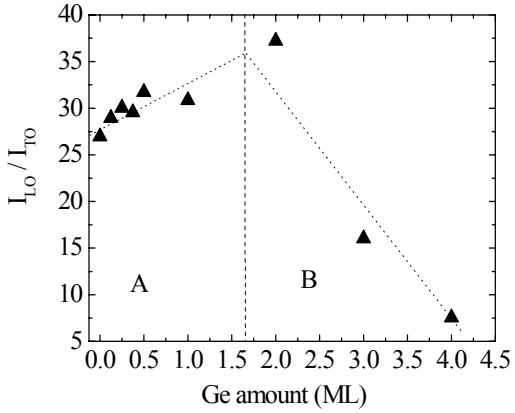

Fig. 7: LO/TO intensity ratio versus the Ge predeposition prior to the carbonization and growth on Si(100).

As in the case of the SSMBE grown layers the strain state in the 3C-SiC layers is always tensile. Two strain regions, A and B, can be observed. In region A the strain decreases linear with increasing Ge precoverage and approaches a minimum at 0.5 to 1 ML Ge. If the predeposition exceeds 2ML Ge (region B) the residual strain in the 3C-SiC epitaxial layer starts to exceed the value of the sample without Ge modification. The strain value determined for the reference sample is comparable to the strain obtained for thick layers grown at temperatures above 1300°C [4]. If Ge is used the residual strain can be reduced to values comparable and lower than in the case of 3C-SiC grown on SOI substrates [4]. Fig. 7 shows the I_{LO}/I_{TO} intensity ratio as a function of the Ge coverage prior to the carbonization. This ratio according to [5] is a measure of the crystalline quality of the grown layers. The obtained intensity ratio increases up to a Ge predeposition of 2 ML where it reaches a maximum. If this limit is exceeded, the SiC quality decreases. As in the case of the SSMBE grown layers it can be concluded that the strain reduction is not due to a deterioration of the overall crystalline quality and can be effectively tuned by the proposed technique.

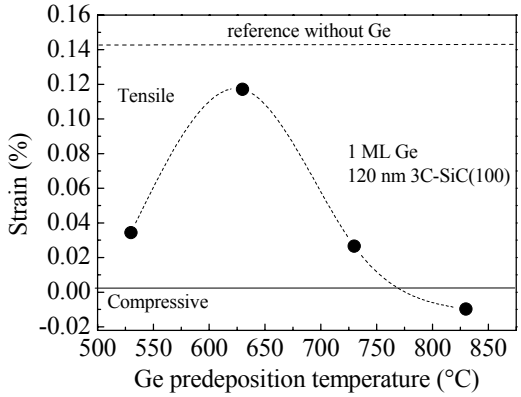

Fig. 8: Strain variation versus predeposition temperature for 120 nm 3C-SiC(100) grown on Si(100).

The influence of the substrate temperature during the Ge deposition onto Si(100) on the residual strain in the 3C-SiC(100) layers grown by UHVCVD is shown in Fig. 8. Independent on the substrate temperatures a reduction of the tensile strain was achieved. At the highest Ge predeposition temperature, i.e. at substrate temperatures above 800°C, a change of the strain state from tensile to compressive was achieved. At substrate temperatures around 625°C the Ge predeposition gave the smallest effect compared to the silicon substrate without Ge modification. So, substrate temperatures above and below these value can be used if strain reduction in the 3C-SiC/Si(100) heterostructure is desired.

Method 3

The strain values calculated from the determined phonon position of the samples grown with the APCVD technique resulting in compressive strained layers without interface modification are summarized in Fig. 9. The results obtained indicate an increase of the compressive in-plane strain for Ge precoverages prior to the carbonization up to 1 ML. If the predeposited amount exceeds this value the compressive strain decreases. The Raman intensity ratio I_{LO}/I_{TO} of the LO and TO phonons of the 3C-SiC epitaxial layers increases with increasing stress relaxation. The increase of the intensity ratio indicates an improvement of the crystalline properties of the grown 3C-SiC(100) layers when the compressive stress is decreasing.

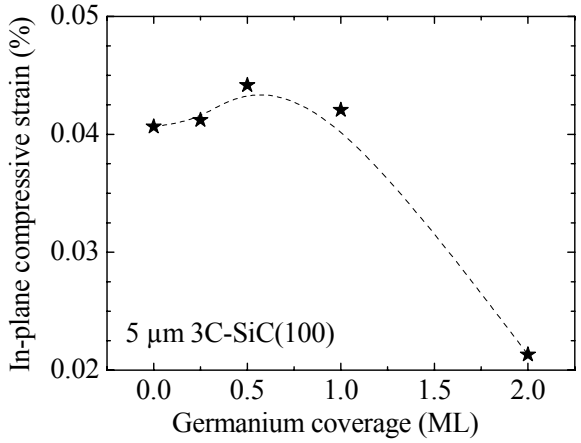

Fig.9: In-plane compressive strain versus Ge precoverage in the case of the 3C-SiC(100) compressive stressed CVD on Si(100).

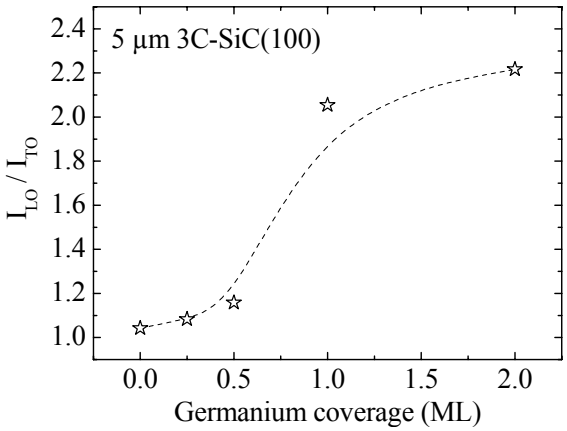

Fig.10: Intensity ratio I_{LO}/I_{TO} of the phonon peaks versus Ge coverage in the case of the 3C-SiC(100) compressive stressed CVD on Si(100).

Method 4

In the case of the APCVD growth process leading to tensile strained 3C-SiC(100) layers on Si(100) substrates two different sample sets were investigated. The first set consists of Si(100) on-axis substrates with a 3C-SiC(100) epitaxial layer grown without Ge modification. This layer was compared to an epitaxial layer grown on silicon substrate, which was modified by depositing 1 ML Ge. In the second series the impact of the Ge predeposition on the strain state in the 3C-SiC layer grown on Si(100) 4° off was investigated. The results of the carried out µ-Raman measurements are summarized in Table 1.

Table 1 Strain and FWHM measured in the 2.5 µm thick 3C-SiC(100) grown on Si(100)

Sample	Strain in %	FWHM TO, cm^{-1}	FWHM LO, cm^{-1}
0 ML Ge, Si(100) on axis	0.062	6.6	7.3
1 ML Ge, Si(100) on axis	0.009	7.4	7.5
0 ML Ge, Si(100) 4° off axis	0.062	6.0	6.7
1 ML Ge, Si(100) 4° off axis	0.12	7.2	8.3

From the results presented in Table 1 it can be concluded that in the case of on-axis wafers Ge incorporation led to a decrease of the tensile strain, where as in the case of off-oriented wafers the tensile strain increases. Off oriented wafer normally led to a more pronounced stepped structure on the surface and to larger step heights due to step bunching [6]. Higher step heights can be interpreted as increase in surface roughness which in turn may led to an increase of stress if germanium is incorporated into the interface as shown in the case of SSMBE (*method 1*) grown samples on *smooth* and *rough* silicon substrates. The FWHMs values of all epitaxial layers are nearly the same. Nevertheless, a slight increase can be

noticed if Ge modified layers are used. TEM investigations carried out on the samples (not shown here) revealed a higher defect density (stacking faults) in the case of the Ge modified substrates in the near interface region. These defects might be the cause for the slight increase of the FWHMs of the phonon peaks. The higher concentration of the oblique stacking faults recombine in the near interface region and do not affect the crystalline quality of the epitaxial layer in the near surface region as found by TEM investigations.

Conclusion

An alternative type of substrates for the heteroepitaxy of 3C-SiC(100) on Si(100) and 3C-SiC(111) and Si(111) has been developed. These substrates consist of a silicon wafer with a chemically modified surface. Here germanium was used. It allows to reduce the stress and to improve the crystalline quality of the grown 3C-SiC layer in a comparable way to SOI substrates, if the Ge coverage is in the range between 0.5 to 1 ML, especially in the case of thin layers. Independent on the growth method and the growth temperatures used the residual stress is shifted towards compressive strain if the initial surface roughness prior to the carbonization process is not to high. This allows to reduce the residual strain in tensile strained layers. These results can provide a promising route towards the optimization of the heteroepitaxial growth of wide band gap semiconductors on silicon substrates.

Acknowledgement

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Two recipes to stabilize the surface melting in FLASiC structures

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Due to the lattice misfit between the silicon and the silicon carbide lattices the epitaxial deposition of SiC layers normally results in a highly defected carbide layer. Short time annealing seems to be an effective method to improve the crystal structure of the epitaxial layer using intense light pulses from flash lamps [1]. From the present point of view the annealing mechanism is based on the rapid melting of a thin silicon interface layer due to the intense light pulse, giving the non molten SiC layer the possibility for relaxation and annealing [2]. Consequently, after the pulse is over and the liquid silicon intermediate layer solidifies epitaxially on the monocrystalline substrate one receives a high temperature annealed epitaxial SiC on silicon structure.

Although the annealing of the SiC layer due to the flash irradiation could be verified by TEM investigations a serious problem remains, connected with the facetted melting of the monocrystalline silicon surface after rapid heating above the melting temperature. Due to the layer by layer crystallisation within the molten pyramides, including a lateral growth component and due to the 5 % higher density of liquid silicon in comparison to solid silicon a surface relief will be formed after the solidification process is completed [3].

Two techniques were tested to circumvent the deep facetted melting. The first procedure to homogenize the melting depth is based on the introduction of a so called melt stop layer in a certain depth below the SiC / Si interface. For this purpose carbon admixture which increases the melting temperature of silicon was implanted at a dose of $2*10^{17}cm^{-2}$ and a energy of 140 keV through a 30 nm thick SiC layer into silicon, forming a approximately 200 nm thick melt barrier in a depth of 400 nm. As a further possibility to prevent the facetted melting ion implantation of germanium admixture, as a element, reducing the melting temperature of silicon was tested.

It could be experimentally shown that both, the introduction of a melt stop layer at any depth behind the Si / SiC interface as well as the modification of the silicon surface, leading to a decrease of the silicon melting temperature, are usefull methods for the homogenization of the melting depth at the bulk silicon / liquid silicon interface.

1. Introduction of a buried melt stop layer

High dose ion implantation was used to form a buried carbon rich layer with a maximum concentration of about 20 %. Corresponding to the phase diagram these high carbon concentration locally increases the silicon melting temperature to about 2000 C, forming in this way a effective melt barrier. To prevent amorphisation in the layer system the implantation was carried out at 600 C. In Fig. 1 the mechanism of the controlled surface melting by carbon implantation is shown.

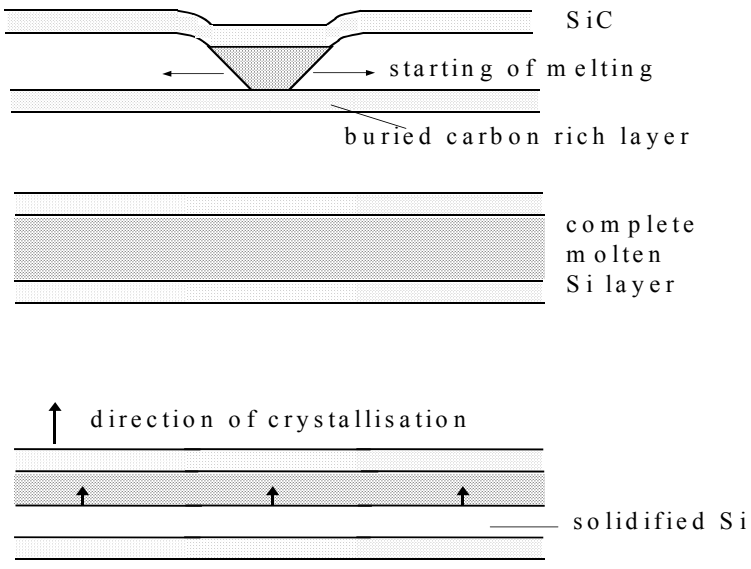

Fig. 1: Scheme of the influence of a buried carbon layer on the melting behaviour of bulk silicon after flash lamp irradiation

If a spontaneous molten island extends to the C implanted layer having the increased melting temperature, vertical melting stops. Nevertheless melting proceeds in horizontal direction until the single molten islands touch each other forming a thin molten silicon layer between the buried carbon rich but crystalline silicon layer and the SiC overlayer. After the pulse is over the molten silicon layer crystallizes epitaxially on the C implanted but crystalline layer. Thereby the C concentration in the melt increases due to the low segregation coefficient of carbon in silicon what involves that the melting temperature increases and the crystallisation velocity decreases. This mechanism results consequently in a self adjusting crystallisation i.e. the crystallisation velocity will be laterally homogenized by the carbon content.

Fig. 2 illustrates the effect of the C implantation on a pure silicon surface. Whereas the flashed non implanted surface shows the typical facetted structures characterising deep bulk melting, the implanted surface remains flat after the flash with a certain energy sufficient for the melting of the silicon layer between the SiC and the buried C – implanted layer. Only in the case that the energy is high enough to melt the bulk silicon behind the melt stop layer surface degradation starts likewise.

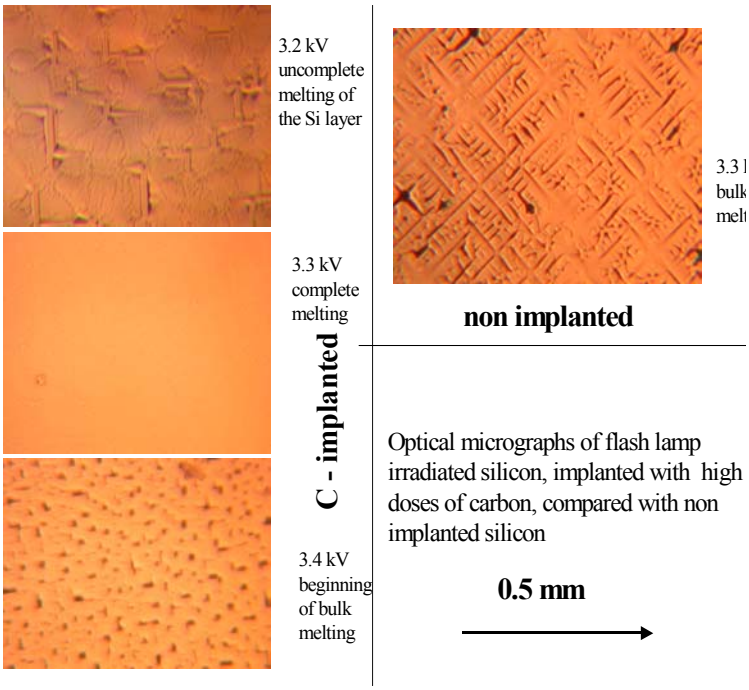

Fig. 2: Surface of carbon implanted and flashed (100) silicon samples in comparision to a non implanted sample

In Fig. 3 the surface of a real SiC / Si FLASiC structure (30 nm SiC on Si), implanted with carbon, after the flash is shown. Like in the case of the pure silicon surface no buckling is visible at a mean flash energy of 3.3 kV. However, if the flash energy exeeds 3.5 kV, even in the case of carbon implantation buckling is observed. This can be related to the beginning of bulk melting after the carbon rich layer is completely dissolved. TEM investigations have shown, that in this case the implanted carbon is completely transferred to the SiC layer.

From the recent experiments we can conclude, that the high dose implantation of carbon is a effective way to prevent deep bulk melting in FLASiC structures whereby the buckling effect can be reduced dramatically. However, the flash energy window for the successful application of the melt stop layer seems to be quite small, what requires, consequently, a very good flash homogeneity.

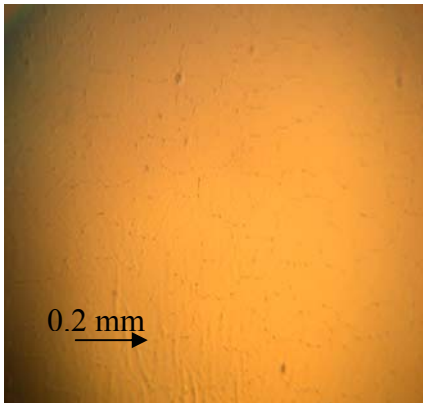

Fig. 3: C implanted, 30 nm SiC structure, flashed at 3.4 kV, 3 ms (preheating 750 C)

2. Introduction of a germanium rich surface layer reducing the silicon melting temperature

As a further possibility to prevent the facetted surface melting of silicon ion implantation of germanium as a element reducing the melting temperature was tested.

A ion dose of $2*10^{17}cm^{-2}$ was implanted at 90 keV, 120 keV or 190 keV through a 40 nm SiC layer into the silicon surface. A high implantation temperature of 600 C was chosen to prevent amorphisation in the layer system. According to the phase diagram (Fig. 4), the Ge content for the 120 keV implantation, for example, leads to a approximately 60 C reduction of the silicon melting temperature in a buried, 50 nm thick silicon layer.

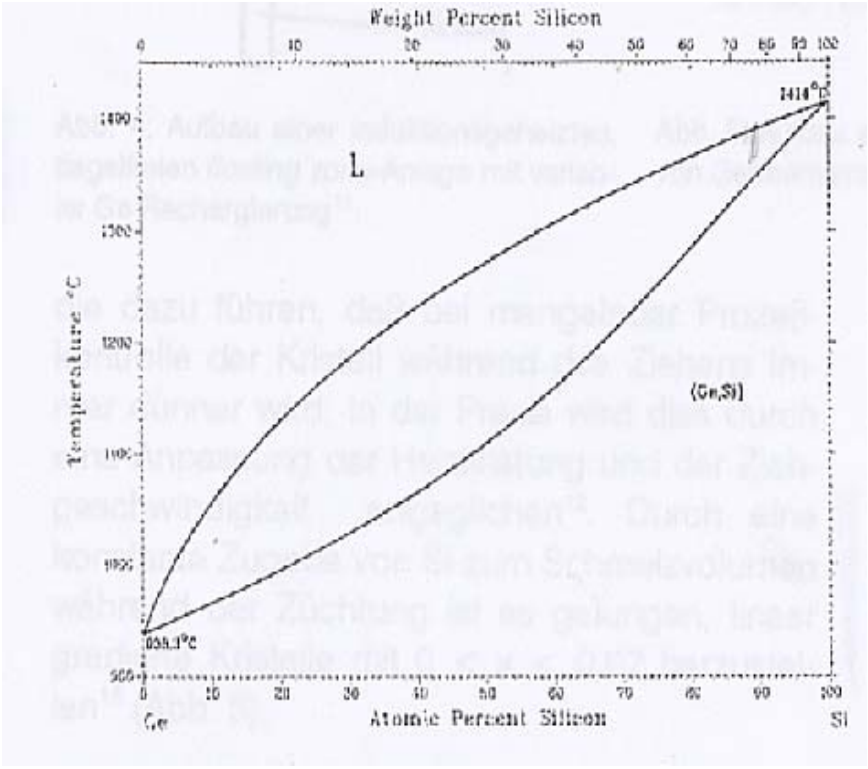

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Fig. 4: Si / Ge phase diagram

It could be shown, that after the flash lamp irradiation the surface of the samples remained flat in a wide range of flash energies, in contrary to the non implanted samples. This could be verified by XTEM investigations showing after the flash irradiation only small pyramide stubs (Fig. 5) instead of full pyramides, which are characteristic for non implanted material. The thickness of the stubs does not exceed 30 nm even at the highest flash energy of 3.4 kV.

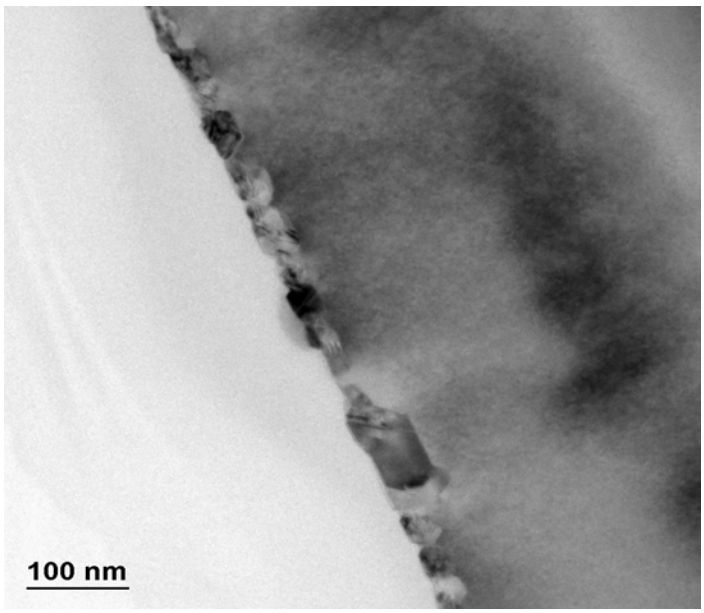

Fig. 5: XTEM micrograph of a Ge implanted SiC / Si sample after flash lamp irradiation

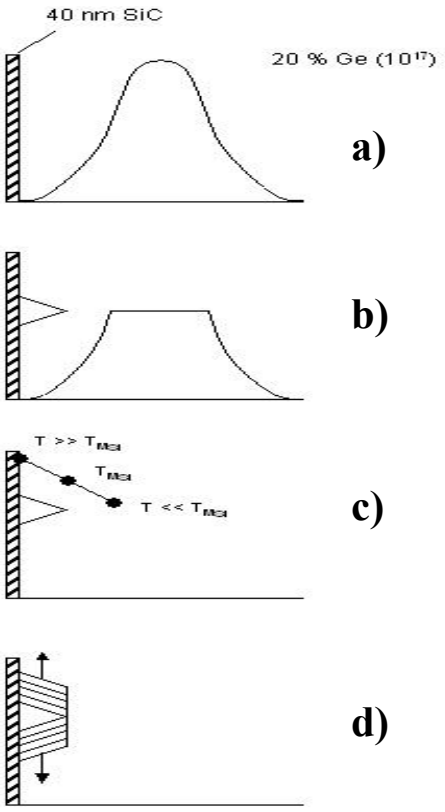

Fig. 6: Stages of the melting process

In Fig. 6 a scheme of the sequence of the discrete stages in the flash melting process is shown.

a) After the implantation of a dose of $10^{17}cm^{-2}$ the melting temperature in the profile maximum is reduced by about 40 degree

b) During the flash irradiation melting starts at the Ge profile maximum because of the melting temperature reduction in the profile maximum.
After the temperature at the surface exceeds the silicon melting temperatuere, facetted surface melting takes place

c) Due to the heat consumption in the Ge rich, molten layer by latent heat, the temperature in the layer remains below the silicon melting temperature. Nevertheless the sample surface is overheated and starts facetted melting as indicated by the pyramides. A very high temperature gradient is formed

d) As soon as the peak of the pyramide in the pure molten silicon reach the depth, where$T = T_{mSi}$ the vertical melting stops and broadening of the molten zones in direction, parallel to the surface takes place until they touch each other, forming a homogeneous thick molten silicon layer

Conclusion

Both, the introduction of a melt stop layer in any depth behind the Si / SiC interface and the installation of a surface layer, decreasing the silicon melting temperature, are usefull methods to homogenize the melting depth in the bulk silicon. For both approaches high implantation doses ($\sim 10^{17}$ cm^{-2}) are necessary to have success. However, the range of energy density is much more broader for the Ge implantation than for the melt stop carbon implantation, what may be of prime importance for the pulse homogenity requirements to the flash lamp equipement.

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SiC as a high-performance material for microheaters

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Abstract:

In the present paper we report on novel device architectures, which employ hetero-epitaxially deposited ß-SiC and antimony-doped tin oxide (SnO_2:Sb) layers as high-temperature stable membrane and heater materials, respectively. We show that in this way micro heater devices can be realized that extend the high-temperature capabilities of such devices to temperatures into and beyond the 1000°C range. Reaching such elevated temperature ranges, novel device applications such as bright thermal IR emitters, surface ionization sources, flameless ionization detectors and the like come within reach.

Key words: silicon carbide, β-SiC, hotplate, high-temperature device, doped metal oxide

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I. Introduction

During the past decade micro heater devices have been an active field of investigation. Driver applications for such devices are thermal mass flow sensors, metal oxide gas sensors and thermal infrared emitters [1]. In the majority of these investigations standard silicon micro-machining technologies have been employed to produce the thermally insulated membrane structures. These investigations have convincingly shown that micro-miniaturisation leads to low levels of heating power consumption (~50 mW at 400°C) and small thermal response times (~10 msec). Up to the present time the vast majority of such microstructures have been realized using standard silicon micromachining technologies, which means that thermally

insulating membranes consist of SiO_2, Si_3N_4 or polysilicon layers deposited onto the base silicon wafers.

As an alternative to dielectric membrane structures also hotplate architectures have been investigated in which the dielectric membrane materials have been replaced by monocrystalline silicon layers shaped into spider-like geometries to compensate for the much higher thermal conductivity of Si as compared to SiO_2 and Si_3N_4 [2]. Electrical heating of such structures is generally accomplished using evaporated or sputtered films of platinum (Pt). Using such material combinations long-term stable device operation has been found to be feasible up to about 600°C.

In order to extend the temperature limitations of micro-heater devices, novel kinds of material combinations need to be employed. In this paper we report on micro heater devices that employ spider-like membrane structures formed from hetero-epitaxially deposited ß-SiC and heater meanders consisting tin dioxide degenerately doped with antimony impurities (SnO_2:Sb). The first base technology for realizing such devices is the ability of depositing ß-SiC layers onto Si wafers using methylsilane (CH_3-SiH_3) precursors. At deposition temperatures T_d of about 1160°C, this kind of epitaxy process is selective to the kind of substrate material encountered: whereas SiC can grow directly on a Si surface, growth on SiO_2 covered parts of the same is inhibited. In this way a direct deposition of patterned ß-SiC layers can be achieved simply using pre-patterned SiO_2 masks. As the electrical conductivity of ß-SiC can be controlled by in-situ doping, in principle, hotplate and heater meanders can be fabricated within one and the same material system. A drawback of ß-SiC heater meanders, however, is that they suffer from ongoing surface oxidation and thus changes in the heater resistance as the device is operated for prolonged periods of time. In order to alleviate such problems, heater meanders were formed from degenerately doped tin dioxide (SnO_2:Sb) layers. With such oxidation-resistant heater elements peak membrane temperatures of the order of 1500°C and long-term stable heater operation in the vicinity of 1000°C could be reached.

II. Design

For reasons of low power consumption and short thermal response time, micro-heater devices should be based on micro-machined membrane structures [3]. For reasons of enhanced high-temperature stability the membrane structures should consist of materials capable of operating at temperatures up to 1000°C for prolonged periods of time. In this respect silicon carbide (SiC) is one of the most suitable materials [4], [5]. As the thermal conductivity of silicon carbide (SiC) is about three times higher than that of silicon, suspended membrane designs need to be employed to reduce the heat flow from the heated area to the supporting silicon rim [6].

In ambient atmosphere both silicon and silicon carbide form natural oxides whose growth is diffusion-controlled and thus self-limiting. SiC has the advantage of a smaller oxidation rate as compared to silicon, whose oxidation rate is larger by a factor of 5 to 10 in the relevant temperature range [7], [8]. Furthermore the band gap of SiC is about twice as large as that of Si. For this reason the onset of plasticity can be expected to shift from the silicon onset of 600°C to about 1500°C in the case of SiC.

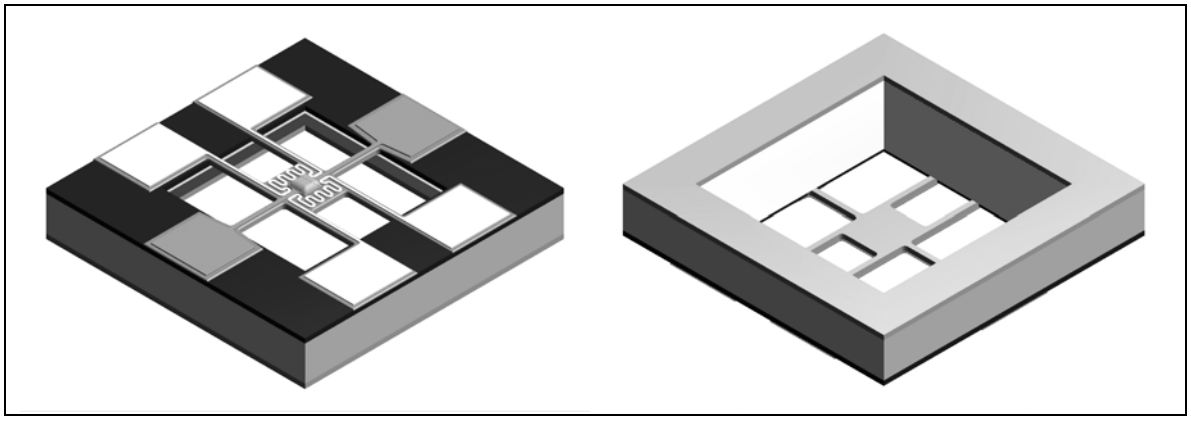

Fig. 1: **(left)** Design of a high temperature micro-heater chip based on a suspended β-SiC membrane. Heating is provided by two heater meanders (white) positioned on both sides of an optional gas sensing film in the middle of the SiC - membrane. The heater meanders consist of heavily doped tin dioxide; an optional gas sensing film is contacted by interdigital Pt electrodes (grey); **(right)** backside view of the chip revealing the membrane opening and an oxidised SiC layer, which acts as an etch mask during the fabrication process.

In order to give an idea about the geometrical dimensions of the micro heater design in **Fig.1**, all relevant geometrical parameters are listed in **Table1**. The central hotplate area measures 400 x 400 µm² and is suspended on six 400µm long bridges.

Table 1: Geometrical hotplate design parameters.

Outer chip dimension	2500 µm
Outer membrane dimension	2500 µm
SiC Membrane size	400 µm
Length of SiC suspensions	400 µm
Width of SiC suspensions	40 µm
Thickness of Membrane and suspensions	2 µm
Heater metallisation thickness	950 nm

III. Growth of 3C-SiC on Si Substrates

The base technology needed for realizing such devices is the ability to deposit ß-SiC onto Si substrates using methylsilane (CH_3-SiH_3) precursors. Furthermore the crystalline properties of

the deposited β-SiC layers need to comply with certain quality standards to enable long-term high-temperature operation.

a) Deposition-technology to obtain β-SiC thin films

The 3C-SiC layers are grown by means of low-pressure chemical vapour deposition (LPCVD) in a self-developed cold wall reactor (**Fig.2**). A thermal graphite resistor heats the substrates inside the reactor to the needed temperature. The dimensions of the reactor limit the substrate size. The maximum size of the substrate is limited to 4 x 4 cm² by the reactor dimensions.

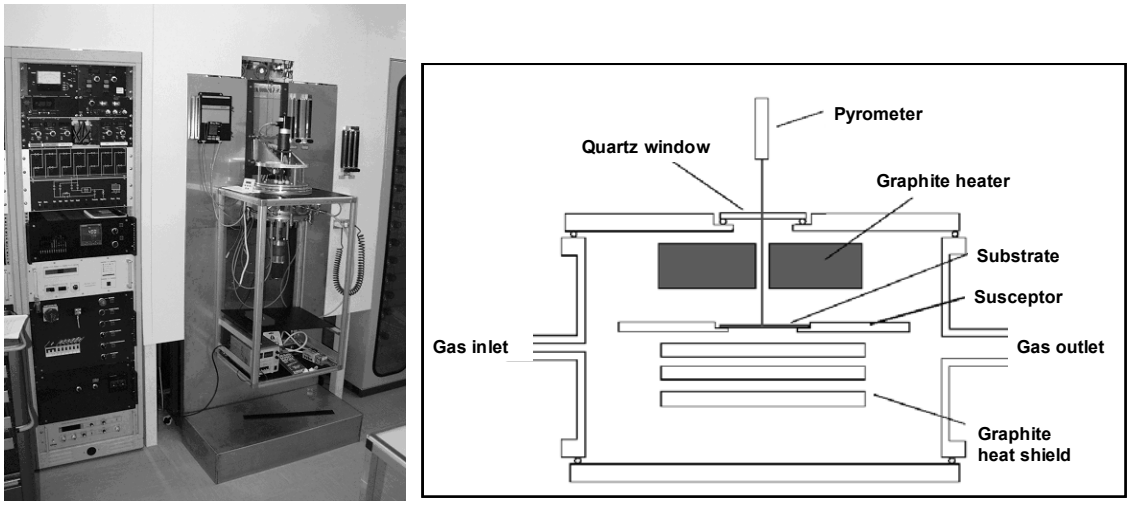

Fig. 2: (left) photograph of the LPCVD installation and its control panel; **(right)** schematics of LPCVD reactor. SiC is epitaxially grown at 1200°C on Si substrates.

The right picture of **Fig.2** shows the schematic build-up of the reactor. The substrate is suspended on two sides in a rotating susceptor. Additional heat shields under the substrate maintain the homogeneity of the deposition temperature. A pyrometer system controls the substrate temperature during the deposition process.

The deposition process is divided into two phases: at first a carbonisation step is performed to form a transition layer that allows to gradually adapt the smaller ß-SiC lattice parameter of 4.36 Å to the much larger lattice parameter (5.43 Å) of the Si substrate [9]. Thereafter the very ß-SiC layer is grown to the required thickness. Using such a two-step process a much higher crystalline quality can be achieved in the upper SiC layer. The carbonisation step is performed at T_d ~ 1220°C in a flow of 50 sccm ethene (C_2H_4) and 50 sccm argon (Ar) at a process pressure of 0.2 mbar. The subsequent ß-SiC layer is grown at T_d ~ 1200°C in a gas flow of 50 sccm hydrogen (H_2) and 3.3 sccm mono-methylsilane (CH_3-SiH_3) at a process pressure of 0.5 mbar. In this way 2µm thick ß-SiC layers can be grown within about 30 min.

b) Quality of the obtained thin layers of β-SiC

The quality of the obtained cubic ß-SiC was evaluated by XRD measurements. Hereby only the 200 and 400 reflexes of the cubic SiC and of the silicon bulk substrate was observable with a very significant <100>-orientation. These results show that the deposited SiC is almost mono-crystalline which results in a favourable high temperature stability.

IV. Patterning of SiC by means of selective epitaxial growth on silicon.

One disadvantage of employing SiC within a MEMS process is the difficulty of structuring the deposited layers. Due to the inertness of ß-SIC it is almost impossible to structure the material using standard wet chemical etching processes. Also dry etching processes like ion beam etching (IBE) require very long etch times and lack selectivity to the underlying silicon substrate. For this reason an area-selective epitaxy process was employed for depositing patterned ß-SiC layers.

The selective epitaxial growth of SiC on Si takes advantage of a thin layer of thermal SiO_2 on top of the Si substrate, which has been pre-patterned prior to the SiC deposition step. This latter process is illustrated in **Fig.3**. On the left-hand-side the Si substrate with the patterned SiO_2 layer is shown. In order to initiate a direct growth of SiC hotplate structures, the SiO_2 was removed by standard wet chemical etching in the white areas. On the right hand side the same substrate is shown after the deposition of the ß-SiC layer had been completed. Obviously, SiC has only grown in those areas that were initially uncovered by SiO_2. This patterning is due to an ongoing evaporation of the SiO_2 layer as SiC is grown on top of the evaporating SiO_2 layer.

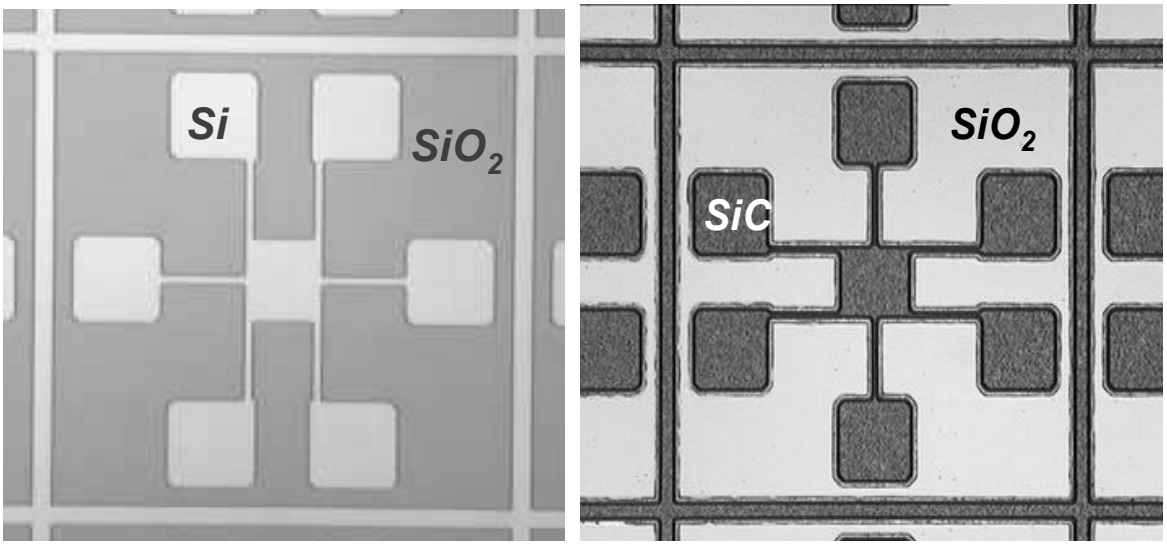

Fig. 3: (left) Patterned SiO_2 mask at the surface of a Si wafer. Wet etching easily patterns the SiO_2 layer**; (right)** SiC pattern grown by selective epitaxy at 1200°C.

In this way the SiC hotplate structures could be directly deposited onto the Si substrate. After the SiC deposition the SiO_2 masking layer was removed to make the wafers ready for the next series of processing steps.

V. Fabrication

For the realization of the micro heater devices of **Fig.1**, <100> silicon substrates of 2 cm x 4 cm size with a thickness of about 300µm were used as starting materials. The specific resistance of the employed <100> Si was about 30-50 Ω·cm at room temperature. For reasons of process simplicity mainly standard process technologies were applied to finalize the sensor device. The first processing step consists in the growth of a 700nm thick oxide on both surfaces of the Si substrate by means of a thermal wet oxidation step. Subsequently the SiO_2 layer was patterned by a wet etching process with the help of a photo resist mask. After this pre-treatment the wafers were ready for the above-described epitaxy process [10].

Following the SiC deposition, a thermal oxidation process was performed to grow a high-quality insulation layer between the supporting hotplate structure and the heater meanders to be deposited on top. This latter wet oxidation step was carried out at 1150°C for 6 hours, which results in a 100 nm thick SiO_2 surface layer. Subsequently the heater structures were realised (**Fig.4)**. At this point highly doped metal oxides rather than standard heater materials such as platinum (Pt) were employed. The reason for employing doped metal oxides is to arrive at well-adhering, high-temperature-stable and oxidation-resistant heater materials.

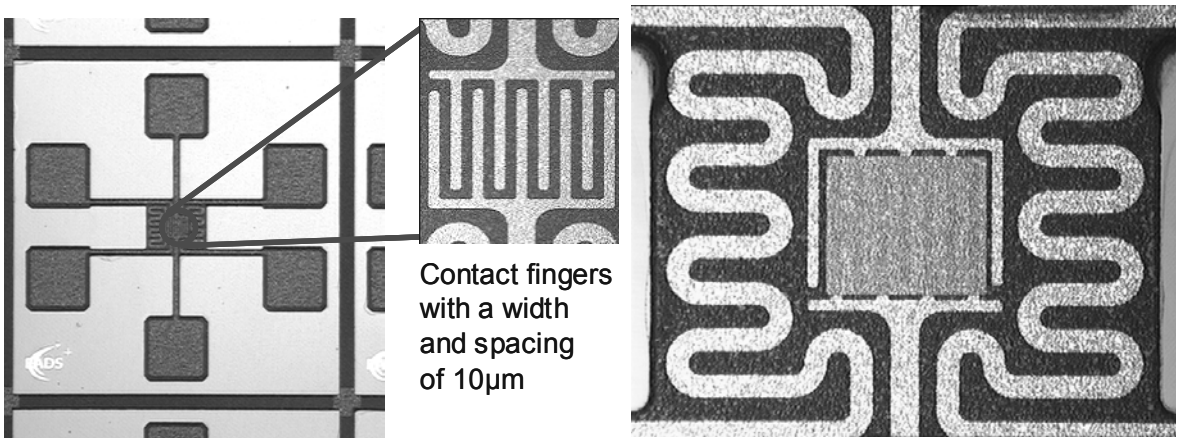

Fig. 4: (**left**) Metallisation structures on top of a passivated SiC hotplate; (**right**) Enlargement of the digital contacting structure in the centre of the suspended membrane covered with a gas-sensitive layer of metal oxide surrounded by two laterally displaced heater meanders. The contacts to the sensitive layer consist of Pt structured in a wet chemical etching process, the laterally displaced heater meanders consist of degenerately doped metal oxide material.

After the top-surface processing had been completed, membranes were realized by anisotropic wet etching from the backside of the Si substrate. Patterning of the etch trough was performed by removing part of the back-surface SiO_2 layer by means of wet etching in buffered HF at 30 °C.

During the membrane etching process problems occurred due to a large number of dislocations introduced into the Si substrate during the high-temperature SiC deposition. **Fig.5** illustrates the lateral under-etching of the SiC layer and a disturbance of the etching itself. As anisotropic silicon etching is sensitive to the orientation of the Si crystal planes [11], dislocation formation disturbs the selectivity of the etching of [111] relative to the [100] and [110] planes. The origin of these dislocations is the large lattice mismatch between Si and SiC (20%) at the SiC/Si boundary surface and the high deposition temperature which causes the dislocations to propagate throughout the entire Si substrate.

In order to alleviate such etching problems, the size of the back-surface etch mask was reduced. In this way the size of the etch troughs were fitted to the hotplate size (**Fig.6**). Problems with dislocation formation, however, remained. In the future these latter problems will be solved by employing dry etching and/or wet etching techniques that are not sensitive to the crystalline orientation of the Si substrates.

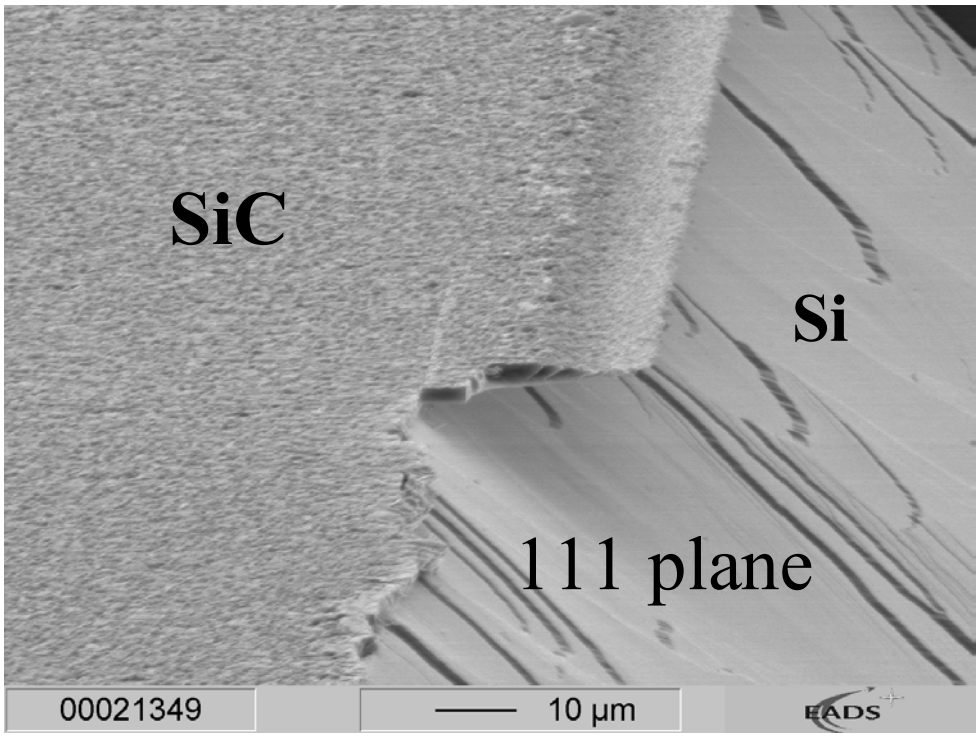

Fig. 5: SEM picture demonstrating the quality of the anisotropic etching process. Two effects are visible: a lateral under-etching of the SiC layer and a disturbance of the etching itself, caused by dislocations introduced into the Si substrate during the chemical vapour deposition of the top-surface ß-SiC at temperatures of about 1200°C.

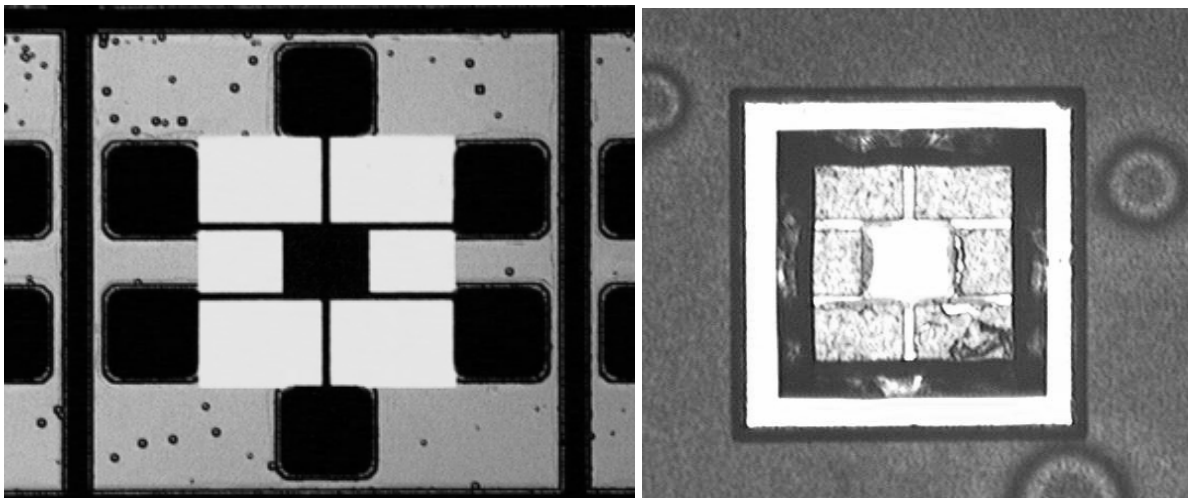

Fig. 6: (left) Thermally insulated SiC microstructure suspended in a Si substrate; **(right)** backside view of the membrane structure. The white area corresponds to those parts of the SiO_2 masking layer that became laterally under-etched during the membrane etching in the dislocation-damaged Si substrate.

Finally, aluminium (Al) contact pads were realized to improve the bonding properties of the MEMS device. **Table2** lists all important materials and their properties.

Table 2: Properties of materials used for the hotplate design [7], [12], [13], [14]

Material	Melting point (°C)	Oxidation rate (Å/sec at 1000°C)	Specific Resistance (Ω·cm /20°C)	Expansion coefficient (ppm/°C)
Si	1415	4	10^{-3} - $2.3 \cdot 10^{5}$	2.6
SiO_2	1713	0.4	$1 \cdot 10^{14}$	0.5
SiC	2800	-	$2 \cdot 10^{3}$ - 100	6
SnO_2:Sb	1920	< 0.1	10 - $4 \cdot 10^{-3}$	1
Pt	1769	-	$1.1 \cdot 10^{-5}$	9

VI. Heater metallisation (SnO_2:Sb)

Using in-situ doping during the SiC epitaxy, heavily doped SiC heater meanders could be formed for heating the above-described hotplate structures. However, when operated in ambient air, ongoing oxidation of the SiC would slowly consume the heavily doped SiC by transformation into insulating SiO_2. For this reason alternative heater materials were sought, which resist oxidation during high-temperature operation in ambient air and which also provide good adherence to the underlying SiC hotplate structure.

Both requirements are best fulfilled by degenerately doped metal oxide semiconductors. In our work we applied thin layers of tin dioxide (SnO_2) doped by small admixtures of antimony (Sb). Such layers can be deposited by e-beam evaporation followed by a subsequent annealing step in air at 1050°C for 2 hours. During this latter annealing step the deposited amorphous SnO_2:Sb changes to a rutile structure, which causes the Sb atoms to become incorporated in the form of substitutional dopants [15], [16]. **Fig.7** shows that the annealing-induced ordering of the SnO_2 structure reduces the conductivity of undoped SnO_2 films by at least 8 orders of magnitude. **Fig.7** further shows that by introducing Sb impurities into such ordered structures, a high conductivity can be restored. Once established this extrinsic conductivity is stable under prolonged high-temperature operation. The highest conductivity of about 4500μΩcm was obtained for Sb additions of about 5% by weight. Chemical analysis of the annealed layers indicated solid state concentrations of about 1% Sb. At higher Sb concentrations a slight decrease in the conductivity was observed - likely due to the onset of alloying effects, i.e. the formation of mixed SnO_2/Sb_2O_3 oxides.

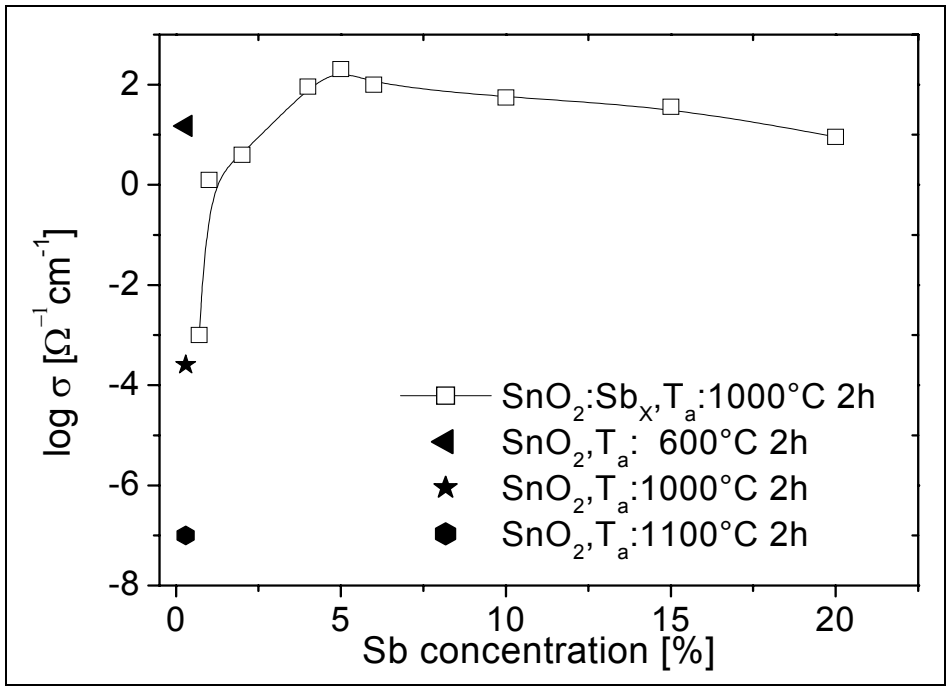

Fig. 7: Electrical resistivity of SnO_2 as a function of Sb dopant concentration and annealing temperature T_a.

Structuring of such layers was performed by lift-off prior to the SnO_2:Sb annealing step using a pre-patterned mask of photo resist. This simple method of structuring SnO_2:Sb layers is enabled by the fact that SnO_2:Sb can be room-temperature deposited with the high-temperature dopant activation step following after the film patterning. The average thickness of our SnO_2:Sb layers was about 900nm.

VII. Operation and stability of SiC-based micro heaters

The left-hand-side of **Fig.8** displays the finalized micro heater chip. This picture also shows contact needles lowered onto the Al contact pads on the solid silicon rim. Through these needles electrical heating power can be applied to the micro heater device. The right-hand-side of **Fig.8** shows the same device with 600mW of electrical heating power applied to it. With this power input white glow could be obtained. Reference to tabulated glow colours indicated temperatures on the order of at least 1000°C.

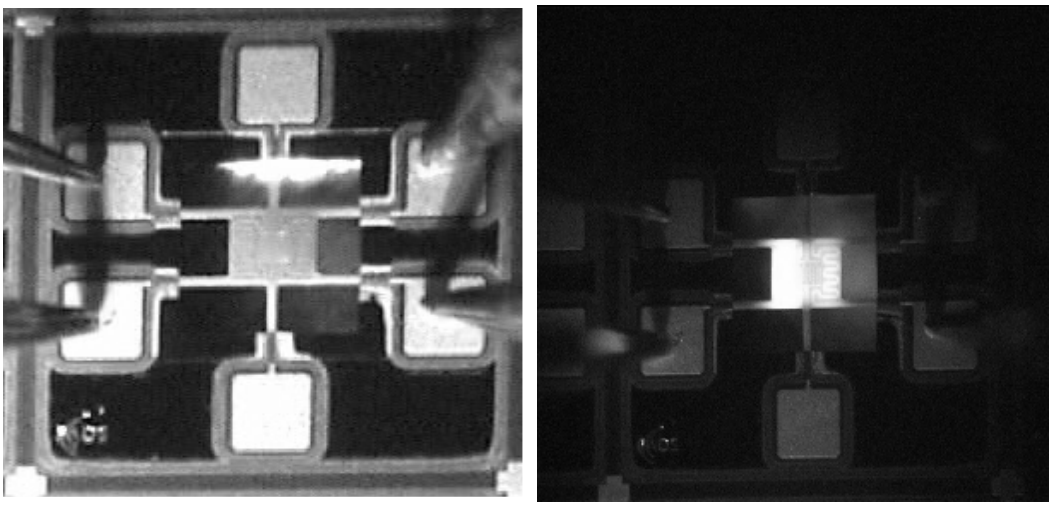

Fig. 8: (left) Finalized micro heater device connected to a power supply with contact needles; **(right)** Micro heater glowing at a temperature of about 1000°C.

In order to assess the long-term stability of our micro heater devices, accelerated degradation tests were performed. During such tests the heating power input into the test device was increased by 50mW every 30 min, until the heater finally failed.

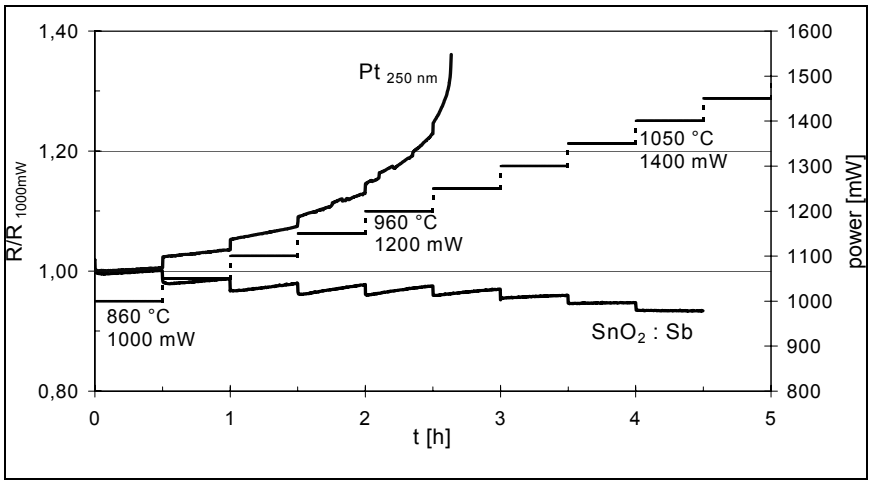

Fig. 9: Rapid thermal degradation experiment of Pt and SnO_2:Sb heater elements deposited onto hotplates.

Fig.9 clearly exhibits, that Pt heater elements rapidly fail at temperatures above 800°C, whereas SnO_2:Sb ones survive up to at least 1000°C. The seeming instability of the SnO_2:Sb heaters at lower temperatures is caused by a residual gas sensing effect, which can easily be avoided using ambient-air packaging [17].

From raw data such as those shown in **Fig.9** Arrhenius plots for the degradation rate were derived. In this way was possible to obtain degradation rates at relatively low operation temperatures where short-term experiments fail to reveal any degradation. With the Pt data shown in **Fig.9** the lifetime of Pt-based micro-heaters can be estimated to be longer than 10 years in case the micro heaters are not operated at temperatures above 600°C [18]. Due to the residual gas sensing effect of SnO_2:Sb layers such extrapolations are not possible in this latter case. Direct long-term tests on SnO_2:Sb-based micro heaters have so far been extended to about two months. During this period of time a measurable degradation could not be detected.

VIII. Potential device applications

So far the most prominent device applications of micro heaters have been heater substrates for metal-oxide-based gas sensing elements. Temperatures on the order of 400°C are typically sufficient for such devices. With the largely improved high-temperature performance of our present devices, a number of novel device applications become possible.

First of all, bright thermal infrared emitters with a short thermal response time can be made. Such emitters form critical parts in non-dispersive infrared (NDIR) gas sensing systems. A particularly interesting method of NDIR gas detection is photo-acoustic gas detection [18]. In addition NDIR methods can also be employed to a number of industrially important liquid-monitoring problems. Further applications which require high-temperature operation of micro heaters in ambient air are flameless ionisation detectors [19] and surface ionisation devices [20]. Both methods of gas detection promise high sensitivity and selectivity to a number of interesting gas species.

Acknowledgment

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Fabrication of 3C-SiC/Si MEMS and NEMS for sensor applications

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Abstract

A technology for the fabrication of silicon carbide MEMS and NEMS based on chemical vapour deposition technique at high vacuum conditions and an electron cyclotron stimulated plasma etch technique was developed. The influence of the residual stress in the 3C-SiC(100) epitaxial layers on the resonator properties is demonstrated.

Introduction

Silicon carbide exhibits outstanding electronic, thermal and chemical properties compared to silicon. For this reason for a long time SiC is in the focus of device research and development for high power, high frequency and high temperature electronic devices as well as for gas and liquid sensors. Recently, SiC received an increasing interest for micro- and nanoelectromechanical systems (MEMS and NEMS) due to its mechanical and chemical properties. The advantage of SiC in comparison to Si, the dominating material in micro- and electromechanical systems, adds challenges to the device processing, which have to addressed before a wide spread application of complex MEMS and NEMS based on SiC can be realized. If the combination of SiC with Si is the target the most important technological processes are: (1) low temperature SiC deposition on large area Si substrates, (2) stress tuning in the SiC/Si heterostructures, (3) residual and etch damage free anisotropic and isotropic etching of SiC and Si, (4) packaging and passivation of the formed structures. In the current presentation low temperature SiC deposition and stress tuning as well as dry etching for the fabrication of SiC based MEMS and NEMS will be demonstrated.

Resonator processing

For the excitation of the vibrations of the SiC resonators in the current investigation, the known magnetomotive effect was used. In such a scheme a driving RF current flows through the resonator placed in ambient conditions with an external static magnetic field. The interaction of the electromagnetic field caused by the flowing current with the static magnetic field causes the Lorentz force. The oscillatory displacement of the beams from their equilibrium position induces an electromotive force, which is proportional to the displacement. If the driving frequency meets the fundamental mechanical resonant frequency of the beam, or a higher harmonic, the deflection of the beam and thereby the induced voltage reach a maximum. To achieve a stable current flow on top of the resonator bars a metal has to be deposited. To fabricate the resonator beams the processing sequence was as follows: (1)

epitaxial growth of 3C-SiC(100) on Si(100) with stress design, (2) deposition of 50 nm Au, (3) photolithography and lift-off technique to structure the metal layer, (3) anisotropic dry etching of the 3C-SiC and the underlying Si, (4) isotropic dry etching of the Si substrate to realise free standing SiC resonator bars, (4) bond pad formation, (5) bonding.

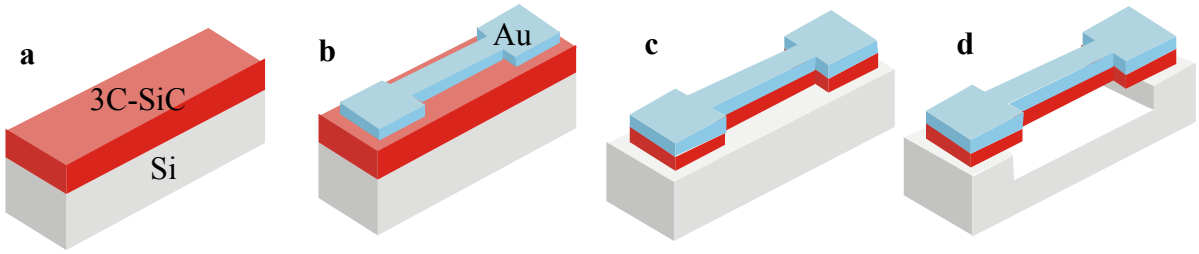

Fig. 1: Process sequence for the resonator fabrication: (a) SiC epitaxy, (b) metallisation, (c) anisotropic etching, (d) isotropic etching

Epitaxial growth

For the epitaxial growth of the 200 nm thick 3C-SiC films a chemical vapour deposition technique was used which is based on an ultra high vacuum chamber (UHVCVD) [1]. The base pressure of the equipment was 1×10^{-9} mbar. As chemical precursors, a mixture of SiH_4 , C_2H_4 and H_2 was used. The epitaxial growth of 3C-SiC(100) on Si(100) was carried out in a temperature range between 700°C and 1100°C. The substrate temperature was chosen in dependence on the necessary crystallinity and the stress state of the 3C-SiC. The stress in the SiC layer can be controlled by: (1) the substrate temperature, (2) the layer thickness and (3) adjusting the SiH_4 to C_2H_4 ration.

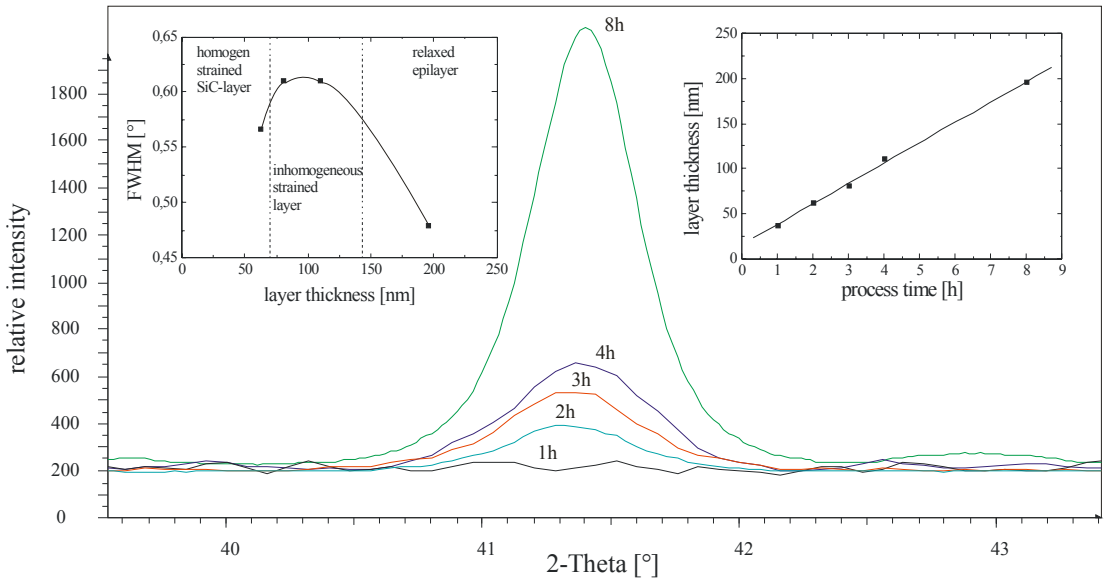

Fig. 2: Relationship between growth time, layer thickness and the state of the stress in the 3C-SiC(100) layers grown at 1050°C determined by x-ray diffraction.

Fig. 2 displays the correlation between the layer thickness, the growth time and the state of the stress in the grown 3C-SiC layers. As it is evident in Fig. 2 the full width of the half maximum (FWHM) of the (002) 3C-SiC peak narrows with increasing layer thickness and shifts towards the unstressed peak position. Furthermore, the diffraction peak looses the asymmetric behaviour with increasing 3C-SiC thickness. The interpretation of the observed changes in the XRD peaks is shown in the left inserted graph of Fig. 2. At the early growth stages up to a thickness of the epitaxial layer of approximately 75 nm the 3C-SiC is homogenously strained. With increasing thicknesses the strain distribution of the grown layer

turns into an inhomogenous strained one. Starting with a layer thickness of about 150 nm plastic relaxation in leading to a reduction of the residual strain and to an narrowing of the FWHM of the (002) 3C-SiC diffraction peak.

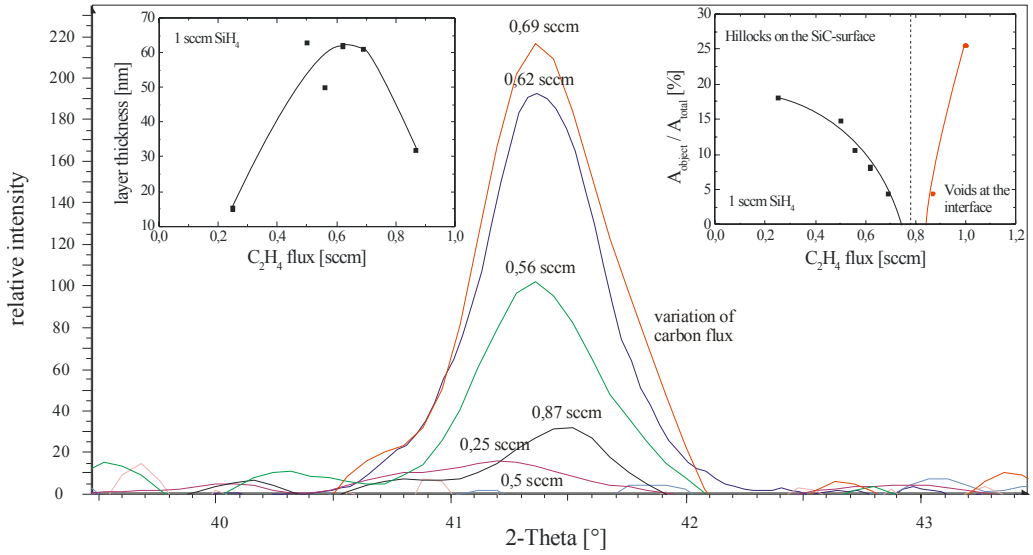

Fig. 3: Correlation between the 3C-SiC growth at 1050°C and the SiH_4 to C_2H_4 flux ratio.

The dependence of the growth rate, the stress state, and the surface and interface morphology versus the SiH_4 to C_2H_4 flux ratio at a fixed SiH_4 flow rate is shown in Fig. 3. The left insert in Fig. 3 displays the layer thickness versus C_2H_4 flux at a constant SiH_4 input. This behaviour is typical for the UHVCVD growth. At higher C_2H_4 flux rates the growth rate drops down due to deficiency of silicon at the growth front. At these conditions the lack of the silicon adsorbed on the surface is compensated by a silicon supply through the growing layer from the substrate side. Consequently, pits are formed in the substrate beneath the SiC/Si interface in the silicon substrate. The dependence of the fraction of the surface area entered by the formed voids is shown in the right insert of Fig. 3. These pits have an inverse pyramidal shape with a square base on (100) substrates. At this growth conditions the surface of the 3C-SiC layer is smooth. At lower C_2H_4 fluxes the surplus of silicon leads to the formation of silicon hillocks increasing the surface roughness of the heterostructure. The relative surface area covered by the formed hillocks is shown in the left side of the right insert in Fig. 3. As a consequence of these two processes the temperature distribution and the SiH_4 to C_2H_4 flux ratio has to be controlled at substrate temperatures around and below 1000°C very carefully in a narrow region. In our case a void and hillock free epitaxial growth was achieved at 0.79 sccm C_2H_4 and a growth temperature of 1050°C.

The differences in the surface morphology affect the stress state of the grown layer. In the case of silicon excess on the growing 3C-SiC surface the void formation at the SiC/Si interface is suppressed and strongly inhomogeneous strained layers are formed. As was shown in [2] the high defect densities at the SiC/Si interface lead to a compressive strain in the interface region. The stress decreases with increasing distance from the SiC/Si interface. At a certain thickness the strain changes into a tensile strain, which overcompensates the compressive component near the interface. For this reason the average strain in the SiC layer is tensile. This inhomogeneous strain causes an upward bending of free standing beams (Fig.4). If the SiH_4 to C_2H_4 flux ratio is shifted in direction of a silicon deficiency the hillock formation probability reduces and finally voids starts to be formed. The voids at the interface

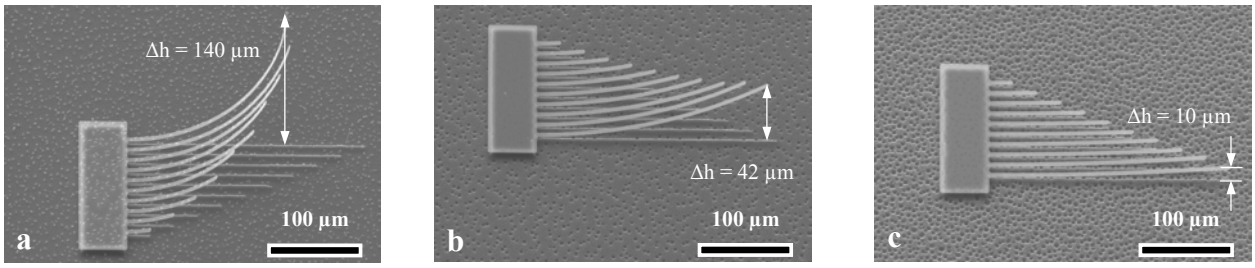

Fig. 4: Beam bending versus surface morphology: (a) hillocks, (b) small pits, (c) voids.

lead to a relaxation in the grown layer promoting a reduction of the residual strain in the 3C-SiC layer. In the transition region and on the void side the stress can be reduced (Fig.4b and 4c). In our case a nearly complete strain reduction was achieved at 0.87 sccm C_2H_4.

Etching

For the dry etching of the MEMS and NEMS structures an electron cyclotron resonance (ECR) source (Roth & Rau) mounted on a plasma laboratory system (Balzers) was used. The ECR source operated at the usual ISM frequency of 2.45 GHz, and a magnetic flux density of 87.5 mT. Two independent gas inlet systems were used for the etch process. The first system enabled the plasma gases, or so called working gases, Ar and O_2 to enter the chamber near the plasma source. The second one controlled the flow of the gases required for the fluorine process for the SiC/Si structures. A special gas distribution ring, located very close to the sample, enhances the chemical reaction and the efficiency of the reactive species inside the plasma. This design allows the excitation of the etching gases by the Ar and/or O_2 plasma directly above the processed surface. The substrate holder allowed water cooling at 18°C or heating up to 600°C. By adjusting the temperature of the substrate the etch behaviour could be controlled. Higher temperatures support the under-etching of three dimensional structures because of the increased isotropic etch component. Low temperatures facilitate the realisation of steep sidewalls and a better anisotropic etch profile. A more complete description of the etch technique can be found in [3, 4].

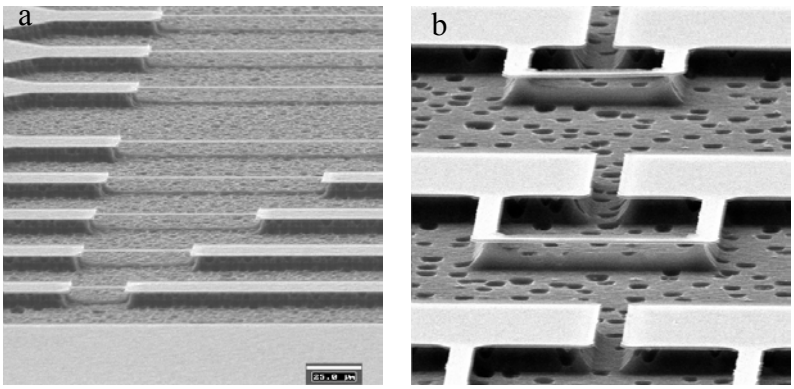

Fig. 5: Double side clamped (a) and U-shaped (b) SiC resonators.

To process three dimensional structures, in our case double side clamped and U-shaped SiC resonators (Fig. 5), a two

step dry etch process was applied. In the first step, a 4:1 mixture of Ar and SF6 was used to etch through the silicon carbide layer, and to realise a some microns deep etching of the the silicon substrate. This etch process was designed to have a pronounced anisotropic behaviour. A low DC bias voltage ~100 V on the substrate was applied to obtain a smooth and straight step profile as well as low etch damage. In the second step, the three dimensional structure was finalised by undercutting the SiC bars. Fr this purpose a high isotropic etch process was developed. To support the under-etching, the gas composition was changed to a 1:1:1-mixture of SF6, CF4, and CHF3.

Resonator properties

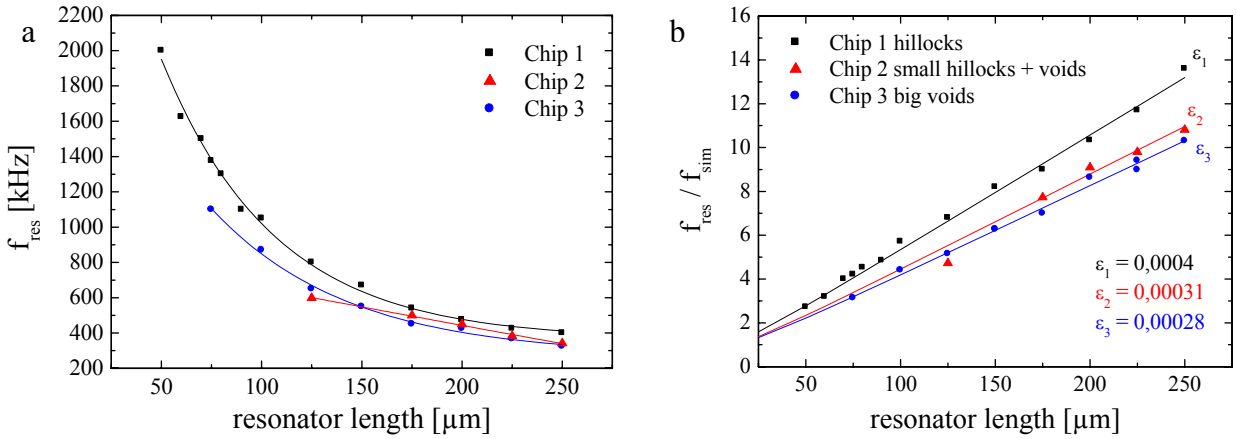

Fig. 6: Resonance frequencies f_{res} versus beam length (a) and the ratio between the measured f_{res} and the simulated f_{sim} resonance frequency (b). ε_i is the determined strain for the differently strained 3C-SiC determined from the simulations.

To investigate the influence of the internal strain of the grown layers on resonator properties the resonators were fabricated on differently strained 3C-SiC layers. The results of the carried out resonance frequencies measurements and the deviations from Euler-Bernoulli theory in the case of double clamped resonator beams are shown in Fig. 6a and Fig. 6b, respectively. According to the Euler-Bernoulli theory the resonance frequencies have to scale with L^{-2}, where L is the resonator length. The measured resonance frequencies are scaling with L^{-1}. As it is evident in Fig. 6b, the deviation of the measured resonance frequency for the layer with the largest strain, i.e. the chip 1 formed on layers exhibiting hillocks, shows the most pronounced deviation from the Euler-Bernoulli theory. The found dependence is in agreement with theoretical predictions in [5, 6].

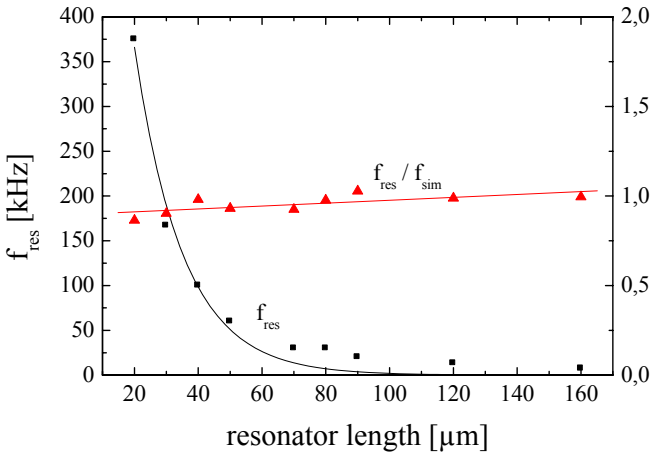

Fig. 7: Dependence of the resonance frequency f_{res} and ration between the f_{res}/f_{sim} versus the resonator length for U-shaped SiC resonators.

In the case of the U-shaped resonators no pronounced deviation between the Euler-Bernoulli theory and the determined dependency of the resonance frequency on the geometric dimensions was found (Fig. 7). The ration between the experimental determined resonance frequency and the theoretical calculated resonance frequency in nearly 1. In this case, due to the geometry of the beams (see Fig. 5b), the resonator is able to relax by bending. This causes a negligible residual strain in the

resonator and only a change in the average elastic constant along the resonator or geometrical fluctuations can contribute to the deviation of the measured resonance frequencies from the theoretically expected. The quality factor determined for the resonators were between 150 and 350 for the double clamped and between 10 and 150 for the U-shaped SiC resonators. These values are comparable with resonators fabricated out of PZT [7].

Conclusion

Free standing both side clamped and U-shaped resonator beams of different geometries were fabricated from heteroepitaxial 3C-SiC(100) epitaxially grown on Si(100) substrates. The resonant properties and the mechanical stability of the beams actuated under ambient conditions in a static magnetic field were evaluated. It was shown that the residual strain in the resonators affects the resonance properties of the SiC resonators. This effect can be used as a tool for tuning of the resonance properties of the resonators.

Acknowledgement

This work has been funded and supported by the Deutsche Forschungsgemeinschaft, SPP 1157: “Integrierte elektrokeramische Funktionsstrukturen”, contract no. AM 105/2-1 and in part by the European Union under Growth project No. GRD 1-2001-40466.

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Fabrication and characterisation of 3C–SiC resonators

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ABSTRACT

This paper summarises recent work performed at the University of Edinburgh on the fabrication and characterisation of 3C–SiC resonators. A simple one-step inductively coupled plasma etching technique has been developed for the fabrication of SiC resonant beam structures. Straight cantilever and bridge devices have been made successfully. The structures have been actuated and resonant frequencies ranging from ~120kHz to ~5MHz have been measured. Comparison of the theoretically simulated and experimentally measured resonant frequencies shows the presence of significant tensile stress (~ 400–500 MPa) in bridge structures while the cantilever beams are free of stress. The degree of the tension in the bridge structures has been found to be independent of the bridge length. Additionally, successful electrostatic actuation of the resonators has been demonstrated.

I. INTRODUCTION

The motivation for developing sensor technologies associated with silicon carbide (SiC) for operation in extreme environments such as high temperatures, high wear and corrosive media, is because of the unique SiC material properties. These include a large band gap, large breakdown field, great hardness, high wear resistivity, excellent thermal conductivity and chemical inertness [1]. In the past, micromachined SiC resonant devices have been fabricated, including pressure sensors [1], lateral resonant structures [2] and micromotors [3]. However, most of the fabricated devices make use of bulk micromachining or micromolding techniques that tend to be more complex than surface micromaching. Significant bending effect has also been observed in released cantilever beams, especially in longer beam structures. The bending effect has been attributed to the result of a bending moment induced by a residual stress gradient through the film thickness [1] and also due to surface tensions encountered in wet etch processes. Recently, nanoelectromechanical systems have been fabricated using surface micromachining techniques and a two-step dry-etch process [4]. In this paper, we report on a simple one-step dry-etch process for the fabrication of released SiC cantilever and bridges. Our simplified dry etch method avoids the potential damage due to surface tension encountered in wet etch processes. The fabricated cantilever and bridge structures have been successfully actuated and the fundamental resonant frequencies have been measured and compared theoretically with simulated data [5]. Moreover, the process has been applied to fabricate nichrome (NiCr) coated SiC cantilevers that could be electrostatically actuated by applying voltages between the top NiCr/SiC electrode and bottom substrate electrode [6].

II. FABRICATION AND TESTING

Two types of starting material have been employed. For the externally actuated resonators, the material used is nominally undoped 2 μm thick single-crystalline 3C-SiC film heteroepitaxially grown on Si (100) wafers – single layer structure. The details of the 3C-SiC growth using a two-step,

carbonization-based, atmospheric pressure chemical vapour deposition process has been described elsewhere [7]. After the samples had been ultrasonically cleaned in acetone and isopropanal, a 3 μm thick SiO_2 etch mask layer has been deposited on the samples using plasma-enhanced chemical vapour deposition system. Photoresist (Megaposit SPR2-2FX 1.3) has been spun on top of the SiO_2 covered samples. Photolithography has been performed to pattern the oxide in the shape of the cantilevers and bridges. The cantilevers are of widths 15 μm and of lengths 25, 50, 100, 150, 200 μm. The bridges have widths 15 μm and lengths of 50, 100, 150, 200, 250 μm. After photoresist development, a plasmatherm PK 2440 reactive ion etching system has been used to remove the patterned SiO_2 layer exposing the SiC underneath. The remaining photoresist has been removed using O_2 plasma. Subsequently, inductively coupled plasma (ICP) using SF_6/O_2 gas mixtures has been optimised to etch the SiC anisotropically and the underlying silicon isotropically with high selectivity using the patterned SiO_2 etch mask. This SF_6/O_2 plasma first etches the SiC layer highly anisotropically because of the dominance of the ion-induced etch mechanism [8] and then continues to etch the Si underneath highly isotropically. The undercut step finally releases the cantilevers and forms the suspended cantilever structures. During this procedure, a SiC etch rate of 270nm/min and silicon etch rate of 4 μm/min have been found, which gives an etch selectivity of Si to SiC of about 15. This indicates that SiC could automatically act as an outstanding mask material during the undercut of the Si. The high etch rate selectivity of Si to SiC coupled with the highly isotropic nature of the Si etch means that the same recipe could be used to pattern and release the SiC beams in a single, continuous process without damaging beams during the release period of the process. The process schematic is shown in figure 1.

The fabricated cantilever and bridge structures have been tested dynamically by attaching them to a piezoelectric disc with a low-melting-point soft wax and vibrating them in a vacuum system. The piezoelectric disc has been driven from a swept sine source and the vibration of the beams as a function of frequency has been detected using an optical vibrometer, the experimental set-up of which has been detailed elsewhere [9,10]. To gain more understanding of the effect of stress in our resonators, simulation of the fabricated structures has been performed using finite element technique (ANSYS) whereby the theoretically predicted resonant frequencies of the devices have been compared with the measured resonant frequencies.

For the electrostatic actuators, the starting substrates consisted of 3 μm thick poly-Si films deposited by low-pressure chemical vapour deposition on thermally oxidised Si wafers of 100mm diameter – multi-layer structure. The thickness of the thermal oxide is nominally 1.5 μm. The poly-Si film actes as sacrificial layer and the SiO_2 film served as an insulating layer when applying electrostatic actuation. A 250nm-thick NiCr layer to be used as a SiC etch mask as well as the top electrode has been deposited onto the SiC surface by thermal evaporation (Edwards Auto306). Following the NiCr deposition, a photoresist (Megaposit SPR2-2FX 1.3) layer has been spun on the NiCr film and photolithographically patterned into cantilever shapes. The cantilever patterns had widths of 15 μm and lengths of 25, 50, 100, 150, and 200 μm. The patterned wafers have been exposed to a NiCr etchant for an optimal time which has been found to be sufficient to remove the unmasked NiCr film as well as minimise the undercut to the formed patterns.

Following the NiCr patterning step, the poly-SiC structures have been released using the inductively coupled SF_6/O_2 plasma described. The process schematic is shown in Figure 2. Figure 3 show scanning electron microscope (SEM) images of released cantilever and bridge structures on the single layer structure and figure 4 show SEM images of similar structures fabricated on the multi-layer structure. The straightness of cantilever beams in the absence of the SiO_2 mask indicates the absence of stress gradient within the SiC film.

III. RESULTS AND DISCUSSIONS

Simple Resonators

The cantilevers and bridges fabricated on the single layer structure have been actuated mechanically and the fundamental resonant frequencies have been measured in a vacuum system. In addition, the fabricated structures have been simulated (including the existence of undercut) in order to compare the theoretically predicted resonant frequencies to the measured resonant frequencies. Figure 3 show fundamental resonance peaks of 200 μm long cantilever and bridge. The experimentally

measured and the theoretically simulated resonant frequencies of all the fabricated beams are shown in Figure 5. A correction factor has been used to quantify the discrepancy between the theoretically predicted and the experimentally measured fundamental resonant frequencies. The correction factor is calculated from the measured frequencies divided by the correspondingly simulated frequencies. It is evident that the correction factors for the cantilevers are almost constant while the correction factors for the bridges decrease with decreasing bridge lengths. For the cantilevers, it is possible to match the simulated resonant frequencies to the measured frequencies by taking into account the possible variation in the SiC layer thickness. In this case, using a SiC layer thickness of 3 μm instead of 2 μm would bring the theoretical and measured values into alignment, i.e. a correction factor of 1.

For the bridge structures, the higher measured frequencies could result from the existence of stress. The equation relating the natural frequency of a bridge to the degree of stress along its length is as follows:

$$\omega^2 L^4 = \alpha + \beta P L^2$$

where ω is 2π times the frequency of the stressed bridge, α and β are constants depending on beam material and dimensions, L is the length of the beam and P is the stress in the bridge. Figure 5 shows a plot of $\omega^2 L^4$ as a function of L^2 which follows a linear trend. This result shows that the bridges are under tensile stress and the constant slope of the fitted line indicates that the degree of tension is independent of the bridge length. Assuming stress-free and string-mode shapes for the bridges, a significant tensile stress of ~ 400 – 500 MPa can be estimated. The intercept of the fitted line corresponds to the value of $\omega^2 L^4$ for bridge structures in the absence of stress, from which the unstressed frequency of a bridge of length L can be determined.

Electrostatic Actuators

The fabricated cantilevers in the multi–layer structure can be considered to consist of two adjacent electrodes forming two plates of a variable capacitor. For such a structure, the cantilever constitutes the movable plate of the capacitor and its displacement is controlled by the voltage applied across the plates, namely the top NiCr/SiC and bottom bulk Si electrodes. In a small deflection range, simple parallel–plate theory [11] can be applied to characterise the dynamic behaviour of an electrostatically actuated cantilever. The electrostatic force, $F_{electrostatic}$, between the capacitor plates generated by applying a voltage V is:

$$F_{electrostatic} = \frac{V^2 \varepsilon A}{2d^2} = kZ \,, \qquad (1)$$

where ε is the permittivity in vacuum, d is the gap between the two electrodes, A is the area of one capacitor plate, k is the spring constant of the cantilever and Z is the amplitude of deflection due to V. It is obvious from this equation that amplitude $Z \propto V^2$.

For an a.c. voltage with a d.c. component, the square of the voltage is:

$$V^2 = (V_{ac} \sin \omega t + V_{dc})^2 = 2V_{ac}V_{dc} \sin \omega t + 0.5{V_{ac}}^2 (1 - \cos 2\omega t) + {V_{dc}}^2 \,, \qquad (2)$$

where ω is the angular frequency of the applied a.c. voltage (V_{ac}).

It is obvious from the above equation that, only the first and second terms contribute to the resonance of the actuators. When the applied frequency of V_{ac} is chosen to be a fundamental resonance frequency (f_0) of the cantilevers, namely $\omega = 2\pi f_0$, only the first term can drive actuators into resonance at f_0. In contrast, when the applied frequency of V_{ac} is chosen to be $f_0/2$ ($\omega = \pi f_0$), only the second term can result in a fundamental resonance at f_0.

The electrostatic performance of the actuators have been characterised by applying a combination of a sinusoidal a.c. voltage (V_{ac}) and a d.c. (V_{dc}) voltage between the top NiCr/SiC and bottom bulk Si electrodes. The actuators have been excited electrostatically and the vibration of the beams as a function of frequency has been detected using an optical vibrometer (Polytec OFV 3001). The applied frequencies of the a.c. voltages have been chosen to be f_0 and $f_0/2$ respectively, where f_0 had been obtained from the dynamical measurements described above. Since the cantilevers with different lengths behave similarly during the test, here we only present the results from the cantilevers of 200 μm long (f_0=66.65kHz). Figure 4 show the observed fundamental resonance peaks for a

200 μm long cantilever excited by electrostatic actuation when the applied a.c. actuation frequency had been 66.65 kHz (f_0). Also shown in figure 4 are the detected linear relationships between the amplitude and the applied V_{dc} and V_{ac} components when a.c. voltage had been applied at 66.65kHz (f_0). These results are in agreement with the expected performance of electrostatic actuators as determined by equation (1) and (2).

IV. CONCLUSIONS

A one-step dry etching method has been developed to fabricate suspended SiC cantilever and doubly clamped bridge structures using SF_6/O_2 ICP plasma. The dry etch condition has been optimised to take advantage of the anisotropic etch of the SiC layer and the isotropic Si etch (for the release) as well as the high selectivity between the SiO_2, NiCr mask and the Si layer. Straight cantilever and bridge structures have been fabricated successfully and the resonant frequencies of the devices have been theoretical simulated and experimentally measured. By comparing the theoretically simulated and experimentally measured resonant frequencies, it has been found that the cantilever beams are free of stress while the bridge structures are under significant tensile stress whose magnitude is independent of the bridge length. Additionally, successful electrostatic actuation of the resonators has been demonstrated**.**

ACKNOWLEDGEMENTS

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Figure 1

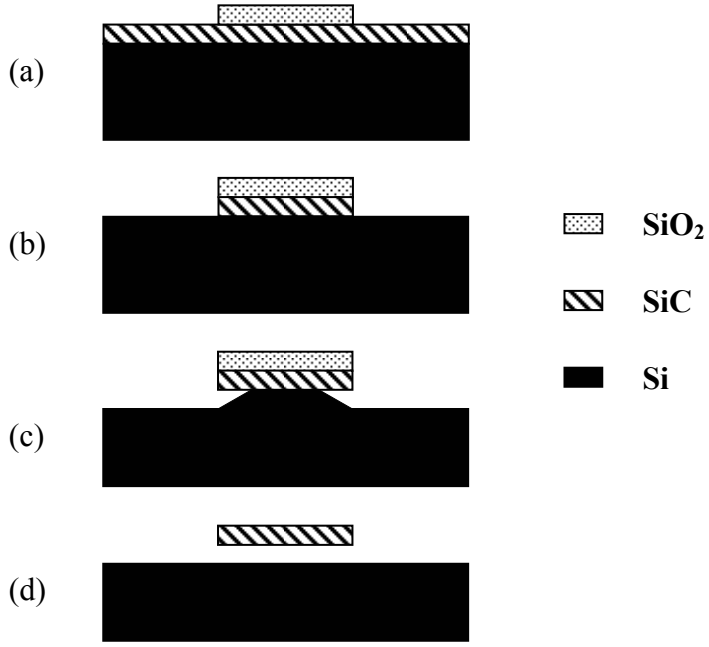


Figure 2

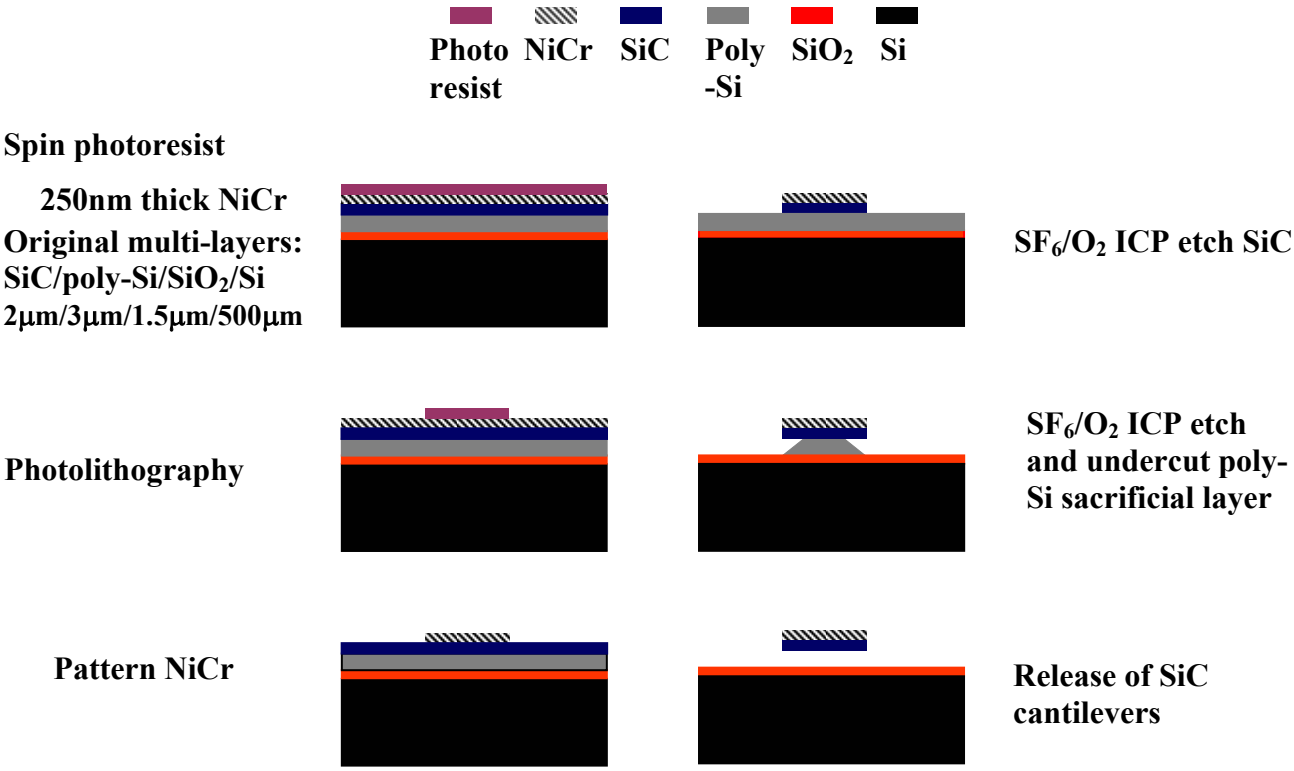
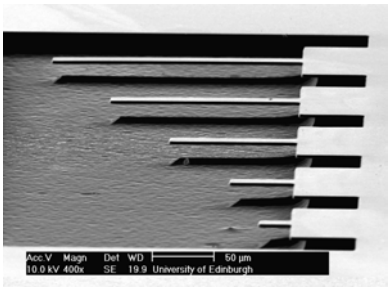


Fig. 3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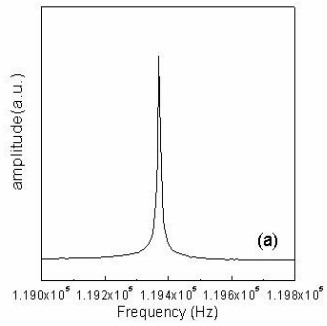
10.0 kV 400x SE 19.9 University of Edinburgh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(a)
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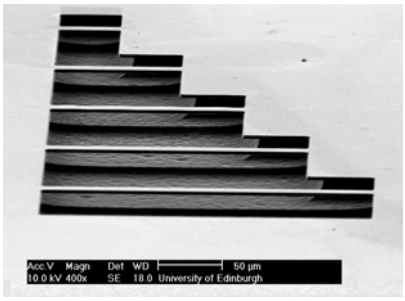
Frequency (Hz)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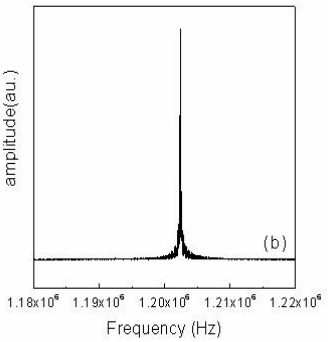
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(b)
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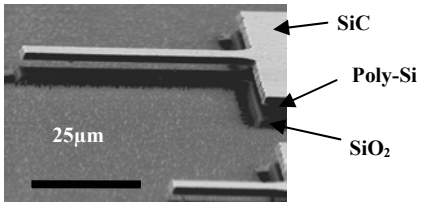
Frequency (Hz)

Fig. 4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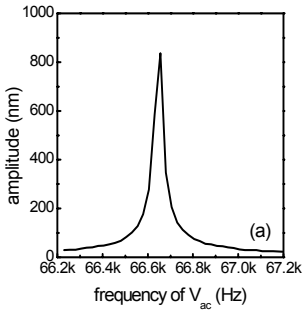
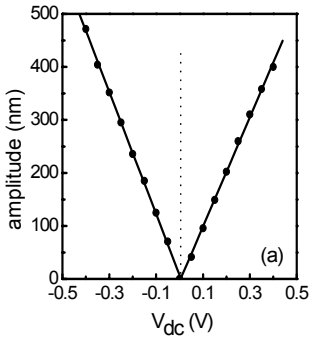
Poly-Si
25µm
SiO2


amplitude (nm)
1000
800
600
400
200
0
(a)
66.2k 66.4k 66.6k 66.8k 67.0k 67.2k
frequency of V_ac (Hz)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400
300
200
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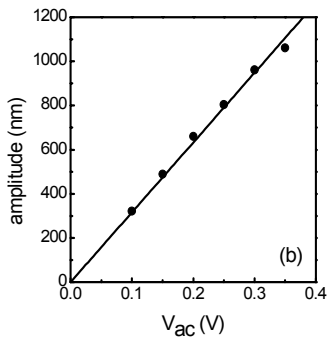
0
(a)
-0.5 -0.3 -0.1 0.1 0.3 0.5
V_dc (V)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800
600
400
200
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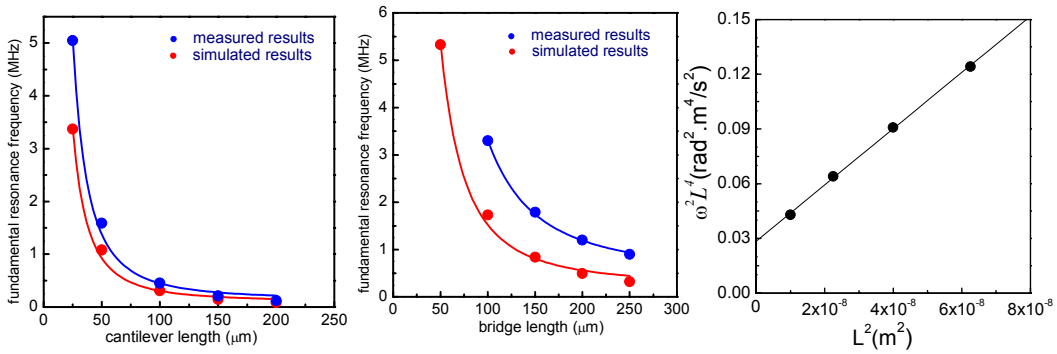
(b)
0.0 0.1 0.2 0.3 0.4
V_ac (V)

Figure 5


measured results
simulated results
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cantilever length (μm)
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50
100
150
200
250
1
2
3
4
5
measured results
simulated results
fundamental resonance frequency (MHz)
bridge length (μm)
0
50
100
150
200
250
300
1
2
3
4
5
6
$\omega^2 L^4$(rad^2.m^4/s^2)
L^2(m^2)
0
2x10^{-8}
4x10^{-8}
6x10^{-8}
8x10^{-8}
0.00
0.03
0.06
0.09
0.12
0.15

ZnO thin films grown by pulsed laser deposition on 6H-SiC single crystals

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Abstract

ZnO thin films were grown by pulsed laser deposition (PLD) on 6H-SiC single crystals and for comparison on a-plane sapphire substrates. ZnO on 6H-SiC is compressively strained with lattice mismatch of +5%, whereas ZnO on sapphire develops tensile strain due to –18% lattice mismatch. The ZnO thin films on 6H-SiC were found to be c-axis textured, however, without preferential in-plane orientation of the grains. The photo- and cathodoluminescence spectra taken at 300K show clear dependence on the excitation depth. ZnO thin films on 6H-SiC show n-type carrier concentration down to 10^{14} cm^{-3} without any buffer layer.

Introduction

The interest in combining the II-VI semiconductor ZnO with other innovative electronic materials as for example different polytypes of SiC is increasing. At the 3rd international ZnO workshop in Sendai, three examples were presented: In [1], the MOCVD growth of ZnO on 6H-SiC for optical cavity fabrication was described. An amorphous interface layer of 2 nm thickness was detected by TEM. [2] shows the improvement of rocking curves and of photoluminescence (PL) ultraviolet (UV) intensity of ZnO films on Si(111) by 3C-SiC buffer layers. The reproducible growth of p-type conducting ZnO is still a challenge. Therefore, [3] successfully demonstrates p-SiC / n-ZnO heterostructures and their electroluminescence spectra. In our preceding paper [4] published in this volume on the growth of ZnO thin films on 3C-SiC buffered Si(100) and (111) we found an improvement of the luminescence properties of ZnO thin films on Si by inserting nm-thin 3C-SiC buffer layers in dependence on the SiC growth process. In this paper we present first results on structure and luminescence properties of PLD ZnO thin films grown on hexagonal 6H-SiC single crystals and on a-plane sapphire. Table 1 compares structural, thermal and electronic properties of 3C-SiC, 6H-SiC, ZnO, GaN and Al_2O_3 as partially taken from [5].

Table 1. Comparison of selected properties of 3C- and 6H-SiC [5], ZnO, GaN, and Al_2O_3.

	3C-SiC	6H-SiC	ZnO	GaN	Al_2O_3
Crystal structure	cubic	hexagonal	hexagonal	hexagonal	rhombohedral
a / c lattice constants (Å)	4.3596 / -	3.081 / 10.053	3.246 / 5.205	3.189 / 5.185	4.758 /12.995
Thermal expansion coeff. (10^{-6} K^{-1})	3.8	4.3	7.2	3.2	7.7
Thermal conductivity (W / cm K)	3.3	3.3	0.6	1.3	0.35
Bandgap structure	indirect	indirect	direct	indirect	
Bandgap energy (eV)	2.2 – 2.4	2.9 – 3.0	3.4	3.5	9.5
Mobility of electrons / holes (cm^2/Vs)	900 / 100	375 / 100	200 / ~2	900 / 30	
Homoepitaxial substrates	no	yes	yes	no	yes

Growth, structure and electrical conductivity of ZnO on 6H-SiC

Three ZnO thin films were grown by PLD on 6H-SiC single crystals, and for comparison on an a-plane sapphire substrate 10 x 10 mm^2 with the same deposition parameters except the growth temperature, as shown in Table 2. The 6H-SiC (0001) single crystals were weakly n-type conducting (N-doped), and had a micropipe density MPD < 100 / cm^2 (grade B).

For details of the PLD growth of high-quality ZnO thin films see [6, 7]. Here, the growth temperature was varied between about 580°C and 700°C (Table 2), as estimated from the temperature of the heater element and a temperature gradient of about 100°C to the heated substrate. The oxygen partial pressure during PLD was controlled at 0.016 mbar for all films. At first, one test film was deposited with much higher thickness of 1.3 µm, however, due to the lattice misfit and resulting strain of ZnO on 6H-SiC [1], this thick film partially defoliates from the substrate, as shown in the photograph in Fig. 1.

Fig. 1. Photo corresponding to about 3 x 2 mm^2 ZnO film surface area with partial defoliation from the SiC-6H substrate. ZnO film thickness was 1.3 µm.

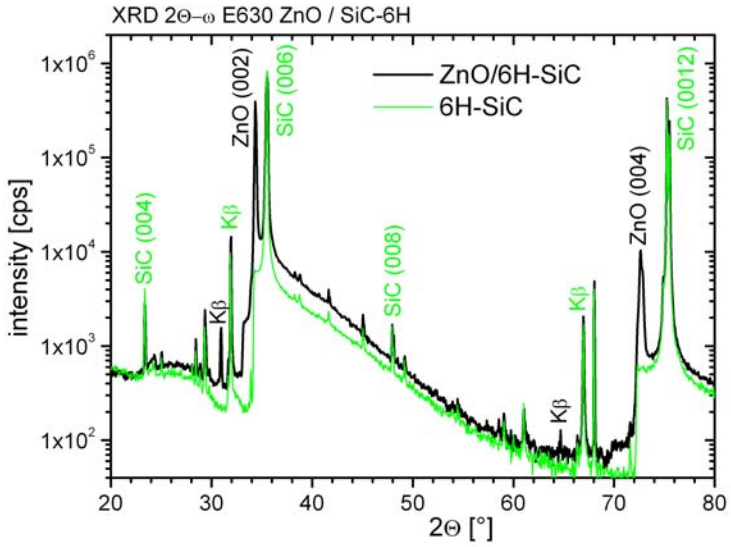

Fig. 2. XRD 2Θ–ω-scan of ZnO 300nm on 6H-SiC single crystal (black) and of 6H-SiC alone before ZnO deposition (green). Only peaks of c-axis textured ZnO are appearing.

Therefore, for all the following ZnO films only 10.000 laser pulses were applied to grow a ZnO film thickness of about 300 nm. The reflection high-energy electron diffraction (RHEED) image of one of the 300nm thin films on 6H-SiC is depicted in [4] in Fig. 2. Because the pattern did not change by azimuthal rotation of the film, no preferential in-plane orientation of the ZnO crystallites seems to be given, although the 6H-SiC substrate is single crystalline, hexagonal and the amount of lattice misfit is smaller for ZnO on 6H-SiC compared to ZnO on Al_2O_3 [1]. The c-axis texture of the ZnO crystallites on 6H-SiC is confirmed also by X-ray diffraction (XRD) 2Θ–ω-scans. We used a Philips X'pert diffractometer and copper K_α radiation (Fig. 2). In Fig 2, only ZnO (002) and (004) peaks appear in addition to the peaks of 6H-SiC. Most of the low-intensity peaks can be attributed to K_β peaks.

The surface morphology of the ZnO films is demonstrated by scanning electron microscopy (SEM) in Fig. 3. Due to the expanding lattice deformation of ZnO on 6H-SiC (see table 1. and the strain relaxation study in [1]), microcracks are visible at the ZnO surface in Fig. 3 (a). At higher substrate temperature, some droplet-like particles are collected at these cracks as surface defects, as shown in Fig. 3 (b). In contradiction, the surface of epitaxial ZnO on a-plane sapphire appears very smooth without any structure in SEM, except the single larger particle in Fig. 3 (c). Fig. 3 (d) shows for comparison a ZnO film surface grown on 3C-SiC 3µm / Si(100) without visible crack formation, however larger hill like structure with diameter of several µm in the center and many surface crystallites with size in the 100 nm range.

After deposition, the DC resistance over the 10 x 10 mm² films was simply measured using a 2-point measurement, for the results see Table 2. Hall results are unsteady because of the cracks in the ZnO films on 6H-SiC, which cause unstable current paths (Table 2).

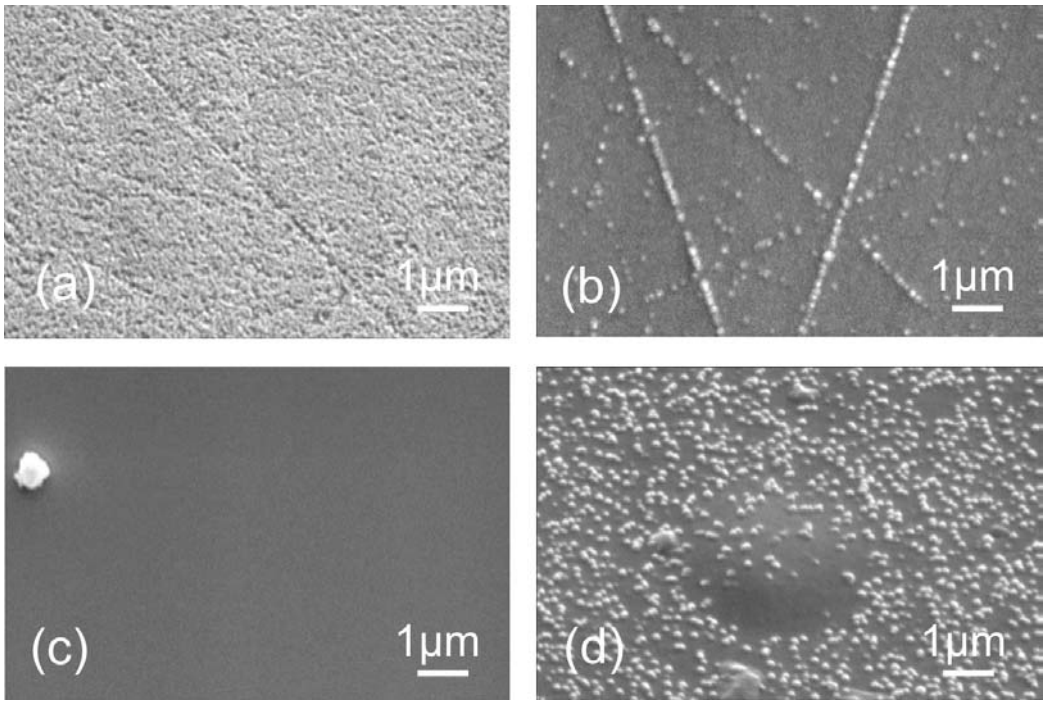

Fig. 3. SEM images of (a) ZnO grown at 580°C on 6H-SiC, (b) ZnO (700°C) on 6H-SiC, (c) ZnO (700°C) on a-plane sapphire, and (d) ZnO on 3C-SiC 3µm / Si(100). ZnO on 6H-SiC shows microcracks due to the ZnO lattice deformation [1].

Optical and electrical properties of ZnO on 6H-SiC

The room temperature photo- (PL) and cathodoluminescence (CL) of the ZnO thin films shows a dominating excitonic luminescence at 3.3 eV and the defect induced green luminescence band around 2.35 eV. The intensity ratios I_{UV} / I_{VIS} of the PL and the CL spectra are shown in Table 2. The excitation depth dependence of the PL and CL spectra shown in Table 2 is similar to that of the ZnO films on various 3C-SiC buffer layers as discussed in more detail in [4].

Table 2. DC resistance (2-point) and carrier concentration (Hall effect) at 300K, and intensity ratio I_{UV}/I_{VIS} of excitonic emission near 3.3 eV to green emission around 2.2 eV taken from PL, and CL at 5 and 10 keV excitation energy for 300 nm thick ZnO films on 6H-SiC and on sapphire. The maximum excitation depth range is given in the first line. PL results are position sensitive.

No. film (growth temp.)	DC resistance Hall carrier conc.	I_{UV}/I_{VIS} PL (range: 60nm)	I_{UV}/I_{VIS} CL 5keV (range: 250 nm)	I_{UV}/I_{VIS} CL 10keV (range: 750 nm)
E775 ZnO/6H-SiC (580°C)	2,400 kΩ ~ 10^{14} /cm^3	3.8	1.2	0.46
E630 ZnO/6H-SiC (640°C)	1,600 kΩ ~ 10^{15} /cm^3	90 - 92	2.9	1.1
E744 ZnO/6H-SiC (700°C)	260 kΩ Hall unstable	5 - 22	4.0	1.9
E745 ZnO/a-Al_2O_3 (700°C)	38 kΩ 3.8*10^{16} /cm^3	346	138	58

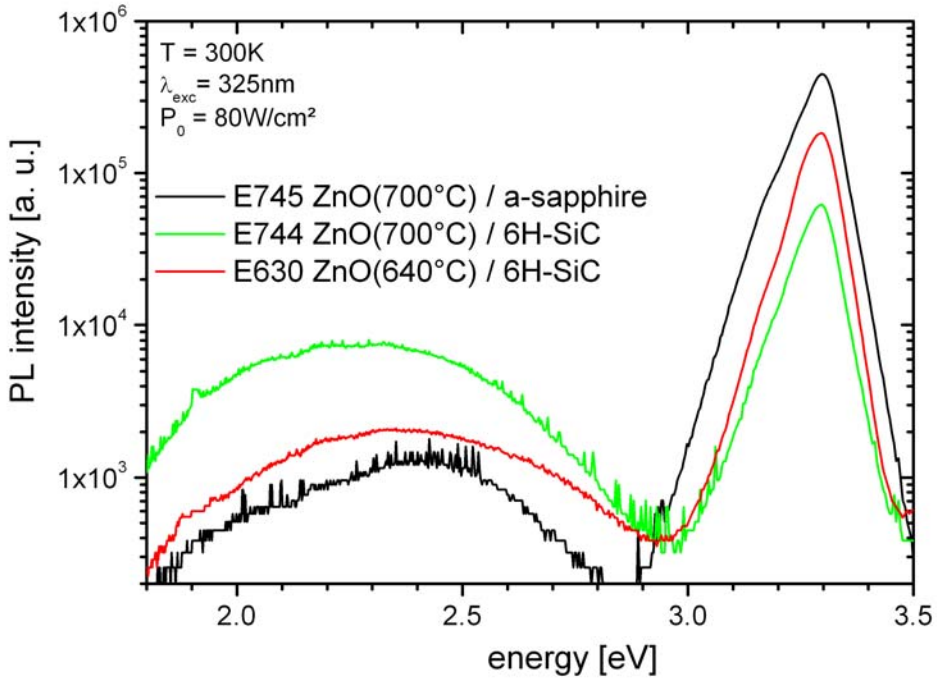

Fig. 4. Photoluminescence spectra (300K) of 300 nm thick ZnO thin films. The legend shows the ZnO growth temperature and the used substrate. PL is most surface sensitive.

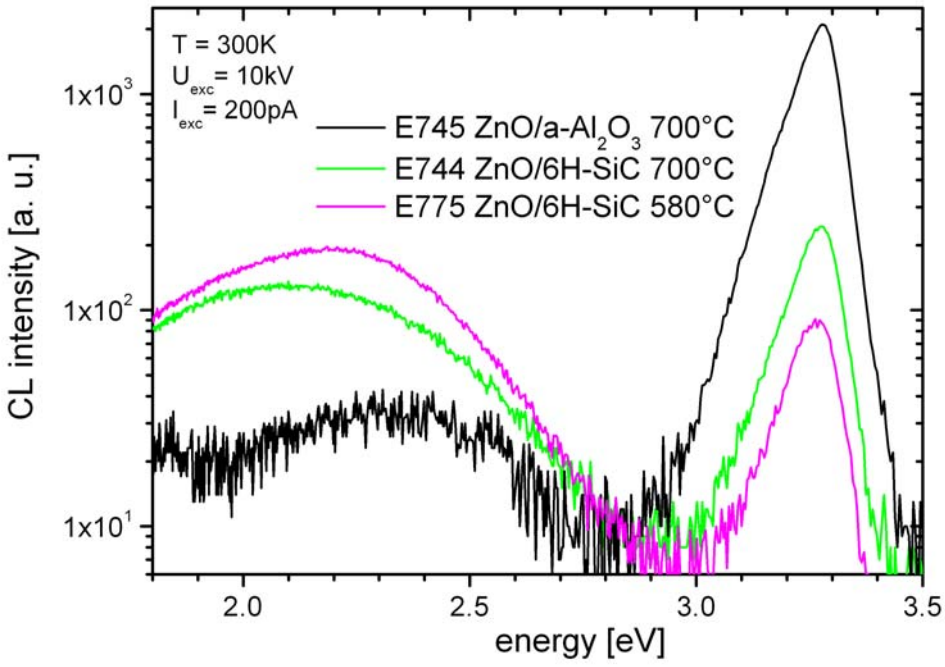

Fig. 5. Cathodoluminescence spectra (300K) taken at 10keV electron energy of 300 nm thick ZnO thin films. The legend shows the ZnO growth temperature and the substrate.

Figure 4. and 5. show typical PL and CL spectra of the investigated films from which the I_{UV} / I_{VIS} ratios in Table 2 were derived. Again, the dependence of luminescence emission of the 300 nm ZnO films on the particular excitation volume is demonstrated. The PL spectra in

Fig. 4. sample the surface region of the ZnO films only, which obviously has the lowest defect density because of the high ratios of excitonic emission to green band emission in the range of 4 to 350 (Table 2).

With increasing excitation depth as controlled by the energy of the electron beam in CL, the intensity of green luminescence band increases considerably, as shown in Table 2 and Fig. 5. This is due to increasing defect density in the ZnO film near the interface, as demonstrated recently by TEM cross sections [8]. Table 2 shows also the DC resistance (2-point measurement) and the carrier concentration from Hall measurement. Interestingly, a relatively low carrier concentration of the ZnO films on 6H-SiC down to 10^{14} cm^{-3} is measured, compared to several 10^{16} cm^{-3} for ZnO on sapphire. Probably, the lower carrier concentration is due to less interdiffusion due to the different chemical nature of the substrates. In order to decide about possible applications of ZnO thin films on 3C-SiC [4] and on 6H-SiC (this work), further optimisation and characterization of the ZnO films on SiC are necessary.

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Effects of implantation of magnetic ions into ZnO

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Abstract

Recent achievements in the field of diluted magnetic semiconductors are summarized. Then, effects of the implantation of magnetic ions into ZnO single crystals are studied by various highly sensitive analysis methods. It is found that the implantation of Fe ions at elevated temperatures (620 K) yields the formation of small ferromagnetic Fe particles. Moreover, the host lattice exhibits open-volume type damage confined at the near surface region. Both effects strongly depend on the ion fluence. On the other hand, after 25 keV focused ion beam implantation of Co^+ no magnetic domains could be detected on a ZnO single crystal surface. However, unscreened electric charges are locally introduced effectuating a contrast within a lift mode-operated atomic force microscope that can easily be confused with magnetic field gradients.

Introduction

Direct and indirect semiconductors exhibiting a wide band gap are currently under intense research due to the fact, that they are good candidates for diluted magnetic semiconductors in room-temperature spintronics[1] (or spin electronics) devices if doped with transition metal ions. In semiconductor devices the spin of the electrons/holes is ignored so far. Especially in high density data storage this leads to a conflict since data are stored by means of magnetic bits on a hard disk while they are processed by magnetically inert semiconductor microprocessors. Hence, a new technology “spintronics” has emerged combining magnetic and transport properties in novel multifunctional materials (Fig. 1).

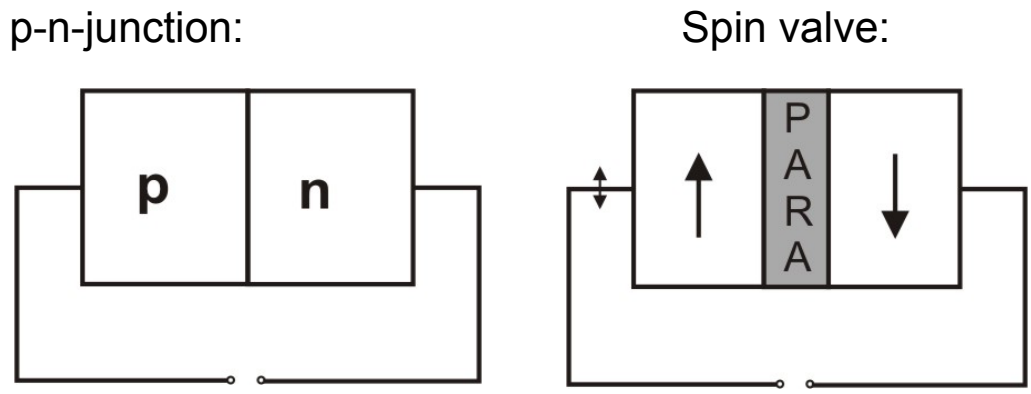

Fig. 1: Comparison of a common p-n-junction and a spin valve used in novel read heads of hard disk drives. Upon application of an external magnetic field the magnetization direction in the two ferromagnetic layers (separated by a paramagnetic layer) are aligned parallel. Therefore, the electric resistance of the spin-valve changes even with respect to a non spin-polarized current (Mott´s two current model)[2].

Some of them, namely giant magneto resistance (GMR) systems, are currently used in hard disk read heads. GMR systems are based on a stack of magnetic multilayers that exhibit a drastic decrease of electric resistivity upon application of an external magnetic field.[3, 4]

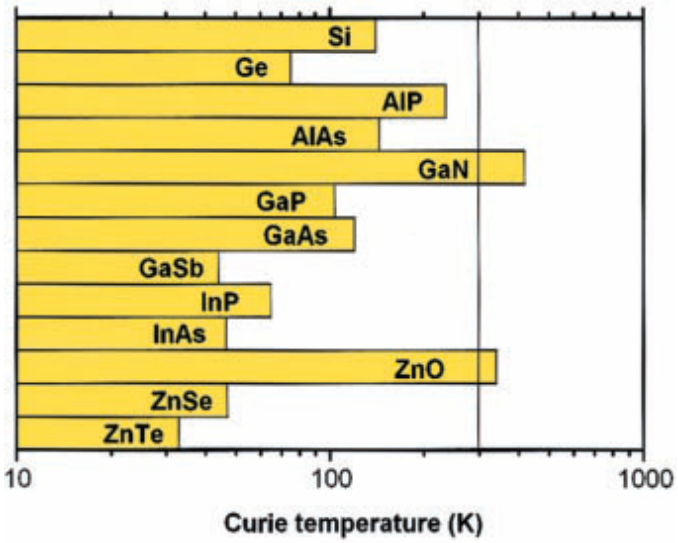

Fig. 2: Curie temperature for various semiconductors with p-type conductivity (3.5×10^{20} holes/cm^3) doped with 5 at.% of Mn predicted from the Zener-model[5].

Another new class of spintronic materials is set up by diluted magnetic semiconductors (DMS). DMS should exhibit spin polarized charge carriers with adjustable carrier density and polarity and thus would allow the production of spin-FET (field effect transistor), spin-LED (light emitting diode), spin-RTD (resonant tunnelling device), quantum bits for communication etc. The charge carrier spin polarization in DMS does *not* arise from ferromagnetic inclusions (2nd phases), but from localized magnetic moments of separated

ions, residing on substitutional anion sites in the host, aligned via an indirect kind of magnetic exchange interaction (Zener-exchange)[5]. Theory predicts several common semiconductors to be ferromagnetic if doped with Mn in the range of 5 at. % (Fig. 2). Experimental confirmation of the theoretical predictions is currently very intensively studied. The only "trustworthy" DMS found so far is that of $Ga_{1-x}Mn_xAs$ showing a Curie-temperature of up to 150 K[6-8]. Besides GaMnAs the wide band gap semiconductor ZnO (E_g=3.2 eV) doped with transition metals exhibits ferromagnetism, i.e. for $Zn_{1-x}TM_xO$[9, 10] (TM = Sc, Ti, V[11], Cr, Mn[12,13], Fe[14,15], Co[16-18], Ni). In Ref. 9 this behavior was explained assuming a spin split "impurity band" of the ZnO host originating from n-type charge carriers introduced by O-vacancies (Fig. 3). A ferromagnetic coupling between the d-states of the dopant only occurs, if the impurity band overlaps with the d-band. For Cr and Mn doped n-type ZnO this is not the case, in p-type ZnO it would.

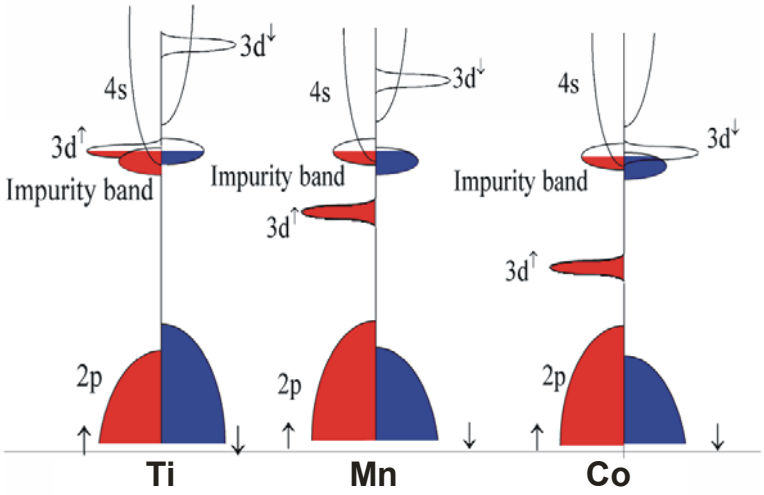

Fig. 3: The spin-split impurity band model explains the measured magnetization for n-type ZnO doped with different 3d-metals in Ref. 9: Only if the impurity band overlaps with the 3d-band of the dopant, ferromagnetic coupling occurs[9].

The impurity band model was tentatively confirmed by Mn-implantation into n-type ZnO with different carrier concentration and mobility prior to implantation[19]. The implantation energy was chosen to be 250 keV, the fluence was $3x10^{16}$ cm^{-2} at 573 K implantation temperature. After implantation the sample was annealed for 1 minute at 873 K in dry air. In this work it was found, that a decrease in carrier concentration triggered by annealing leads to an increase of the saturation magnetization of the sample (Fig. 4).

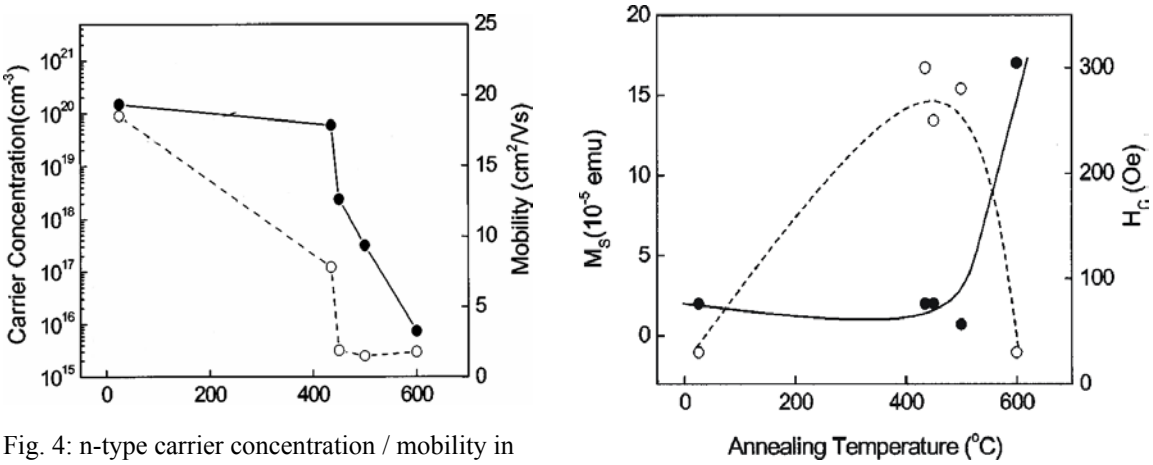

Fig. 4: n-type carrier concentration / mobility in ZnO (left) and saturation magnetization / coercivity (right) depending on the annealing temperature[19].

In contrast to the two above mentioned works, ferromagnetic precipitates can also be responsible for ferromagnetic properties of ZnO but such systems are useless for spintronics. E.g., in Ref. 20 it is shown, that Co-implantation into ZnO single crystals leads to ferromagnetism, but the reason for that is clearly found to be a precipitation of Co-nanoparticles with hex-on-hex-orientation with respect to the ZnO host matrix. The implantation energy was 250 keV, the ion fluence was 3 and $5x10^{16}$ cm^{-2}, and the temperature was chosen to be 620 K. After implantation the sample was annealed at 973 K for 5 min.

Thus the main goal in ZnO-spintronics nowadays is the identification of the position of the transition metal ions within the ZnO host matrix and the search for secondary phases - mainly in order to exclude them. On that field already some progress has been achieved, especially for Fe doped ZnO. Low dose ion implantation ($2x10^{13}$ cm^{-2}) of ^{59}Fe into ZnO single crystals yielded the surprising result, that right after implantation already 90% of the implanted Fe-ions are on substitutional Zn-sites[21]. After annealing the sample up to 1073 K the fraction of substitutional Fe-atoms increases up to ~ 100%, but further annealing at 1323 K causes a decrease of that fraction. On the other hand, $Zn_{0.95-x}Fe_{0.05}Cu_xO$ samples, produced by a solid state reaction method, have been investigated by means of ^{57}Fe nuclear magnetic resonance and neutron diffraction[22]. It was found that the observed room ferromagnetism stems from an inverted spinel $ZnFe_2O_4$ phase. This phase is formed due to the presence of CuO.

Our work on ZnO, as described in detail below, is performed in order to help clarifying whether the source of the ferromagnetic moment in Fe implanted ZnO comes from secondary phases formed within the ZnO, or from substitutionally incorporated Fe atoms on Zn lattice sites.

Experiments, results and discussion

For our present experiments, hydrothermally grown ZnO single crystals from supplier MaTecK/Germany were chosen. The samples have been epi-polished using a chemo-mechanical method. Proton-induced X-ray emission (PIXE) experiments gave some hints of Cu-contamination of the material, maybe due to the production process (see Fig. 5). Rutherford backscattering/channeling (RBS/C) measurements of the virgin samples showed χ_{min}=4%. χ_{min} is the the channeling minimum yield, which is the ratio of the backscattering yield when the impinging beam is aligned parallel to a crystallographic axis to that for a random beam incidence. It is a measure of the overall crystallographic disorder of the lattice. Therefore, an amorphous sample shows a χ_{min} of 100%, while a perfect single crystal corresponds to a χ_{min} of 0% (practically 1-2% for single crystalline film, e.g. GaAs). Nevertheless, the virgin samples are "clean" diamagnets without para- or ferromagnetic inclusions down to a temperature of 5 K, as observed by SQUID magnetometry. The susceptibility amounts -1.48x10^{-6} emu·Oe^{-1}·cm^{-3}.

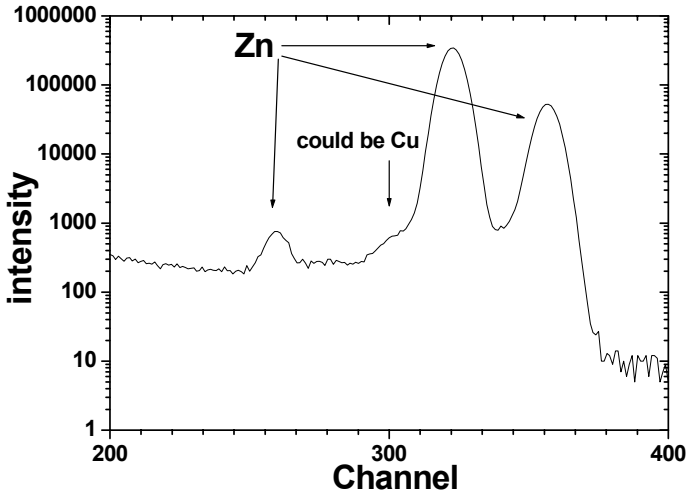

Fig. 5: PIXE-spectrum of the virgin sample. 320 ppm of contamination, probably Cu, was found.

After analysis of the virgin samples they have been implanted with $^{57}Fe^{+}$ ions. The implantation temperature was chosen to be 620 K, the implantation angle with respect to the sample normal amounts to 7° in order to prevent channelling. The ^{57}Fe ion energy was 180 keV leading to a Gaussian shaped ion distribution within the host matrix with a projected ion range of R_P = 82 nm and a straggling of ΔR_P =±35 nm. The values were calculated using the TRIM code[23]. Two fluences, i.e. a high ($\phi = 4x10^{16}$ cm^{-2}) and a low ($\phi = 4x10^{15}$ cm^{-2}), were chosen thus leading to a maximum atomic concentration of 5 and 0.5 %, respectively.

The virgin as well as the as-implanted samples were characterized by positron annihilation spectroscopy in the form of slow positron implantation spectroscopy (SPIS)[24]. Conservation of momentum during the annihilation process is the reason for the fact that the annihilation radiation contains information about the electron momentum distribution at the annihilation site. In our SPIS case, the energetic Doppler-broadening of the annihilation γ-line - due to the motion of the electron-positron-pair before the individual annihilation process - is measured and quantified by the 'S-parameter', which is defined as the area of the central low-momentum part of the spectrum, divided by the area below the whole curve after background subtraction. In Fig. 6 the dependence of the S-parameter on incident positron energy E is given indicating depth-dependent properties of any sample.

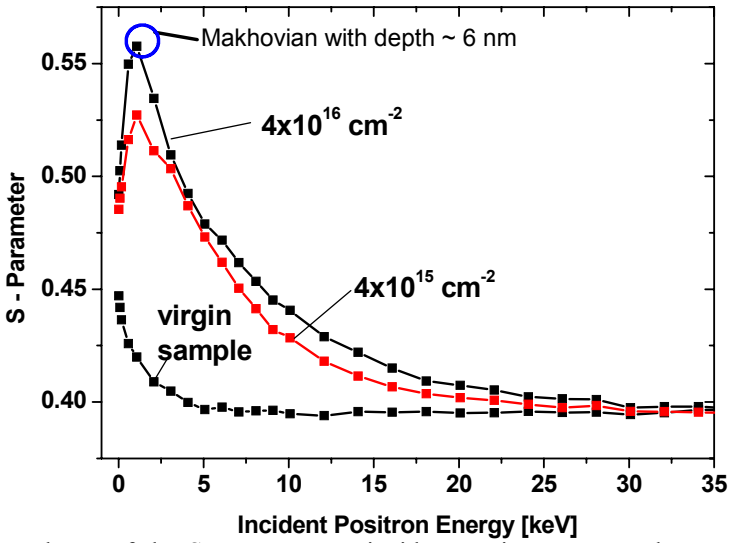

Fig. 6: The dependence of the S-parameter on incident positron energy shows clear differences between the virgin and as-implanted sample.

It shows that open-volume type damage is created proportional to the ion implantation fluence applied. Surprisingly, this damage is almost confined at the near surface region and not at the depth predicted by the TRIM[23] simulation, which might be the result of defect mobility during implantation at 620 K. To elucidate the true nature of this damage, i.e. its structure and concentration, further comprehensive investigations will be necessary.

Magnetic properties of the as-implanted samples have been investigated using conversion electron Mössbauer spectroscopy (CEMS). It was found, that for both samples, i.e. the low and high fluence one, that Fe mainly develops two different charge states. The first fraction exhibits an isomer shift (with reference to α-Fe) that lies between the values expected for Fe^{3+} and Fe^{2+} and shows large quadrupole splitting. The interpretation of this fraction therefore is rather difficult. On the other hand, a non quadrupole split Fe^{3+} state is present for both

fluences. Such a Fe^{3+} state has been observed already earlier[25] using different analysis methods than CEMS and probably represents a diluted situation. Both fractions are magnetically inert. Nevertheless, in the high fluence sample a fraction was found showing ferromagnetic interaction. The isomer shift amounts -0.05 mm/s and the magnetic hyperfine field amounts 305 kOe. Since both values are very close to those of α-Fe, this fraction represents small ferromagnetic metallic Fe-clusters. The relative spectrum area of this fraction amounts to 12%.

In order to prove the suggestion about the Fe nanoparticles as a source for the ferromagnetism, high resolution X-ray measurements have been performed at the ROBL-beamline of the Forschungszentrum Rossendorf in Grenoble where the X-ray intensity is much higher compared with conventional X-ray sources and therefore makes it possible to detect the very tiny amount of Fe nanoparticles. Fig.7 shows a symmetric 2θ/ω scan of Fe implanted ZnO with a fluence of $4x10^{16}$ cm^{-2}. Those sharp and strong peaks are from bulk ZnO. At 2θ is around 44.5°, the peak can be decomposed to a rather broad and weak peak and a very sharp peak originating from the substrate. The broad peak is from bcc-Fe(110) with a theoretical Bragg angle of 22.387° (2θ=44.674°). The nanoparticle size is estimated to be around 6 nm by Scherrer formula[26]. Besides the bcc-Fe, no other phases, e.g. fcc-Fe, Fe-oxides, are detected.

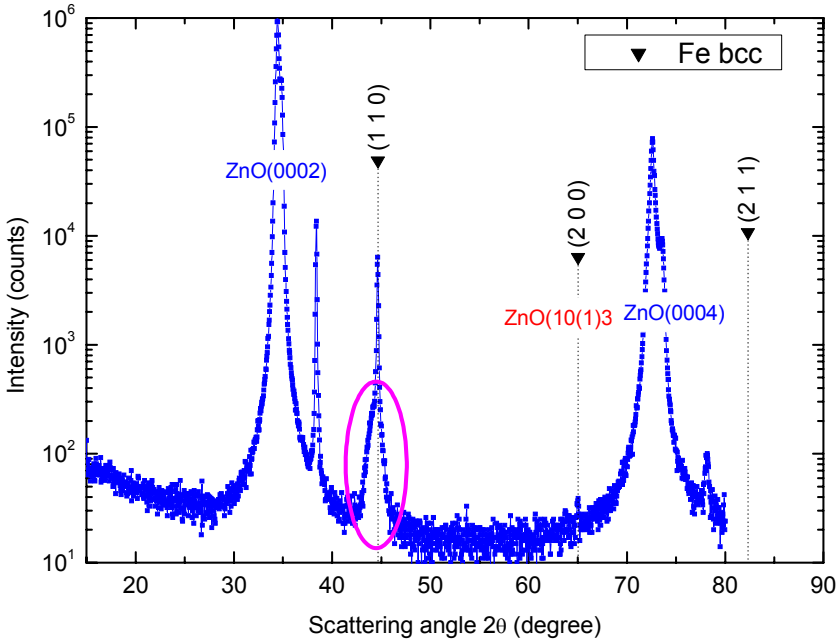

Fig. 7: XRD 2θ/ω scan of Fe-implanted ZnO with a fluence of $4x10^{16}$ cm^{-2}.

In order to achieve laterally structured DMS, Co was implanted into ZnO single crystals by means of focused ion beam (FIB) technique. Rectangular areas of 3x3 μm have been irradiated with Co^+ ions at different fluences using a scanning ion beam of ~50 nm diameter at an energy of 25 keV. The analysis of the structures was performed by means of atomic force microscopy (AFM) in tapping/lift mode. Results are shown in Fig. 8. Tapping mode means that a ferromagnetic tip mounted on an oscillating cantilever is driven line by line across the surface. Every line is scanned two times, the first time in a distance of ~10 nm, where the electrostatic forces of the electric charges bound at the surface are dominant giving the height information and a second time in a distance of ~70 nm, where the electric and magnetic fields of free charges at the surface are dominant (lift mode). Using nonmagnetic as well as magnetic tips in the patterned region an equal force gradient could be detected, thus originating from free electric charges introduced into the surface by the accelerated ions. In any case they would overlap the magnetic interaction. Thus lower fluences and post-implantation annealing are required in order to suppress the free electric charges and to get a pure magnetic signal.

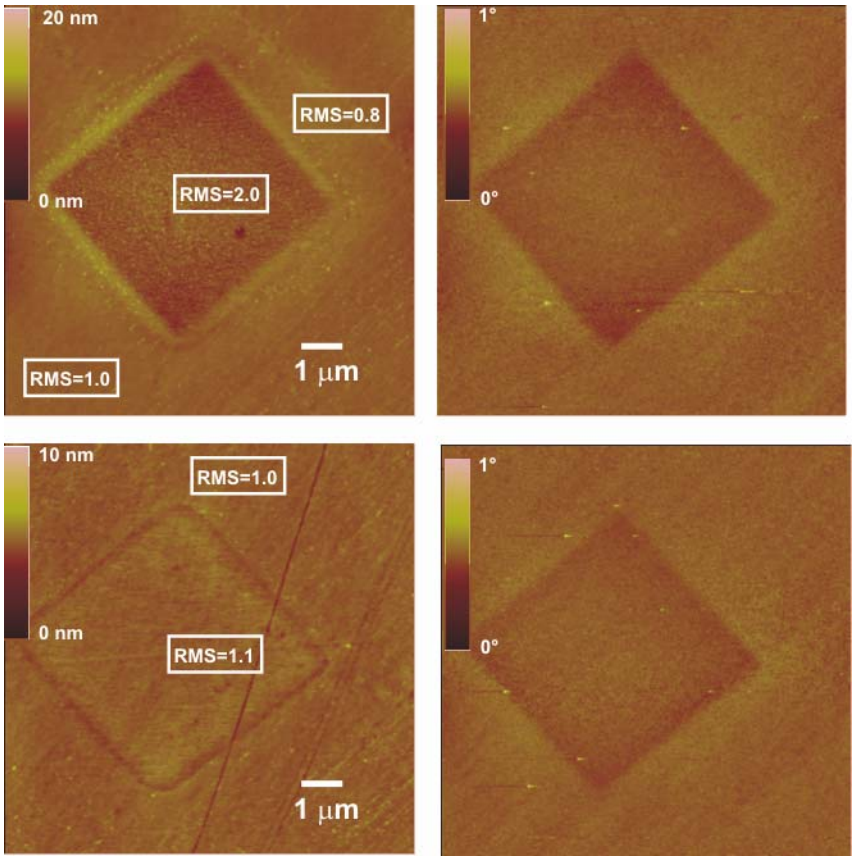

Fig. 8: Tapping mode AFM measurements on a Co implanted ZnO single crystal using FIB. Images a) and c) display the height information for fluences of 6 and $2x10^{16}$ cm^{-2} respectively, images b) and d) display the phase modulation during lift mode scan (height = 70 nm) for both fluences respectively. The irradiated square shows an increase of the root mean square (RMS) roughness that depends on the ion fluence. Note the peculiarity that

the region close to the irradiated square shows a lower root mean square (RMS) roughness then the distant region. This effect is believed to arise from local heat dissipation during irradiation. The contrast in b) and d) is equal for AFM tips with or without magnetic coating and thus is attributed to electric rather then magnetic charges.

Conclusions

ZnO single crystals have been implanted with $^{57}Fe^{+}$ ions at elevated temperatures using two different fluences. Thus, a maximum atomic concentration of 5 resp. 0.5 at.% was achieved in a depth of ~82 nm. By means of CEMS and synchrotron radiation XRD it was found, that at the higher fluence small Fe nanoparticles are created within the ZnO host matrix exhibiting ferromagnetic properties. These particles can hardly be detected using conventional XRD lab equipment. Surprisingly, the damage region of the host lattice is limited only to the near surface region.

On the other hand, Co was implanted at an energy of 25 keV by means of focused ion beam techniques. AFM/MFM analysis of the patterned area revealed, that the tapping/lift mode shows a contrast for magnetically coated and uncoated tips, respectively, and thus can be assigned to unscreened electric charges introduced due to the implantation.

For future experiments it can be concluded, that ion beam techniques are an appropriate method in order to dope ZnO single crystals with transition metals ions leading to a high atomic concentration of diluted ions far from thermal equilibrium. Care has to be taken since - probably due to the introduced defects - Fe shows a high mobility already at an implantation temperature of 620 K and thus forms metallic ferromagnetic secondary phases. For the magnetic activation of the implanted ions low temperature implantation followed by a rapid annealing, e.g. using flash lamp annealing (FLA), is required in order to prevent secondary phase formation.

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Luminescence of ZnO thin films grown by pulsed laser deposition on 3C-SiC buffered Si

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Abstract

ZnO thin films were grown by pulsed laser deposition (PLD) on three different 3C-SiC template layers on Si(100) and Si(111) substrates. The 3C-SiC buffer layers were either grown 3 µm thick by atmospheric pressure chemical vapor deposition (CVD) or only 3 nm thin by ultra-high vacuum CVD (UHVCVD) or by rapid thermal processing (RTP). Up to now, all ZnO films on 3C-SiC/Si are c-axis textured, but no preferential in-plane orientation of the textured grains was found. The photo- and cathodoluminescence (PL, CL) spectra taken at 300K show clear dependence on the excitation depth, indicating a much lower defect density near the ZnO film surface. The intensity ratio of the excitonic luminescence to the defect-induced green emission of 300 nm thin ZnO films on silicon was increased by insertion of thin 3C-SiC buffer layers.

Introduction

The interest in the wide-bandgap oxide semiconductor ZnO has considerably increased within the last years because of the promising optical and electrical properties of high-quality epitaxial ZnO-based thin films and multilayers on sapphire substrates [1]. However, because of the considerable lattice mismatch of ZnO to sapphire, usually a high density of dislocation lines is found in ZnO thin film cross sections by TEM investigations. On the technologically important silicon substrates, the nm-thin SiO_x interface layer gives rise to the loss of in-plane orientation of the textured ZnO films. SiC is a superior material for active high-voltage, high-power, and high-frequency electronic devices [2] and shows a similar wide bandgap and a much smaller lattice mismatch to ZnO. The successful combination of ZnO films and SiC buffer layers or single crystals could open additional perspectives for ZnO-based

optoelectronic devices. Heterojunctions based on n-ZnO and p-SiC could be promising structures on the way to efficient ultraviolet light emitters. In this paper, first results on structural and luminescent properties of PLD ZnO thin films grown on cubic 3C-SiC layers on Si are given.

Growth of ZnO films and 3C-SiC buffer layers

ZnO thin films were grown by PLD on 3C-SiC buffered Si(100) and Si(111). For details of the PLD growth of high-quality ZnO thin films see [3, 4]. Here, the ZnO thickness was around 300 nm for the first film series (sample No. up to E745), and around 600 nm for the second series (E746 – E750). The growth temperature was kept constant at about 640°C. The oxygen partial pressure during PLD was controlled at 0.02 mbar for all films.

The 3C-SiC films have been grown on Si(100) and Si(111) by three different processes either about 3 µm thick (a) or only a few nm thin (b) and (c).

(a) The 3 µm thick 3C-SiC(001) layers were grown by atmospheric pressure CVD in a cold wall vertical reactor. Silane and propane were used as sources and purified H_2 as carrier gas. The Si(100) substrates were heated via a RF coupled graphite susceptor whose temperature was controlled and monitored by an optical pyrometer. The samples were grown with the classical two-steps procedure involving substrate carbonisation at 1150°C followed by thick epitaxial growth at 1350°C at a rate of 3 µm/h. It gives state of the art compressively strained 3C-SiC material on Si substrate [5].

(b) For the rapid thermal carbonisation, Si(100) and Si(111) wafers were loaded into the rapid thermal processing (RTP) equipment without any wet cleaning step. Prior to the carbonisation, an etching step in an Ar-H_2 mixture was carried out at 1000°C for 60 s. The carbonisation was carried out with C_2H_4 at 1220°C for 30 s at gas flow rates of 1000, 100, 1 sccm for Ar, H_2 and C_2H_4, respectively. The total processing time was about 20 min. The relationship of carbonisation conditions and structure is described in [6-8]. The formed 3C-SiC layers are 2 to 3 nm thick and showed a single crystalline structure as confirmed by reflection high energy electron diffraction (RHEED) (Fig.1).

(c) In the case of carbonisation by ultra high vacuum chemical vapour deposition (UHVCVD), Si(100) and Si(111) were cleaned with a standard RCA cleaning procedure finishing with a HF dip. After loading into the growth chamber, the samples were outgassed at 200°C for 1 h. Subsequently, a hydrocarbon adsorption step at 400°C for 10 min was carried out. The carbonisation was performed by using a heating ramp of 0.3 K s^{-1} up to 960°C. The interrelationship between the different process parameters and the structure of the carbonised silicon wafer can be found in

[9]. The UHVCVD process is nearly 10 times slower than the RTP process, although the thickness of the formed 3C-SiC layers is in the same range as for the RTP carbonisation case. However, the corresponding RHEED patterns in Fig. 1 show a more pronounced three dimensional growth for the UHVCVD process.

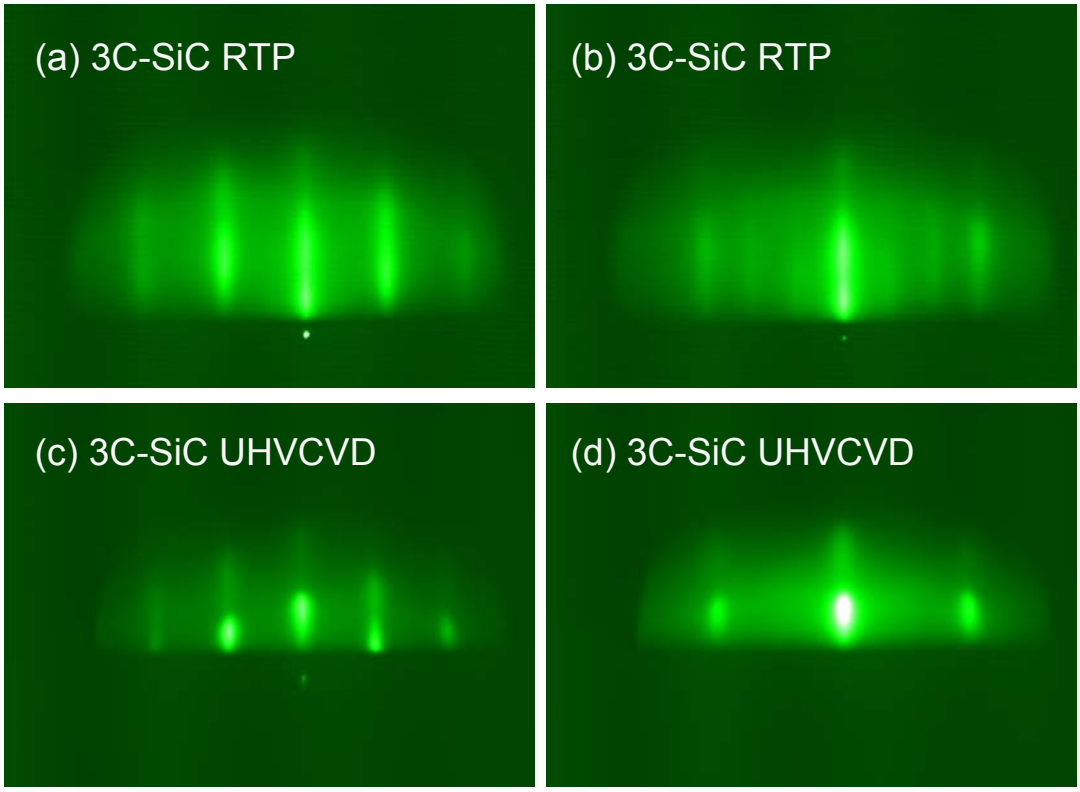

Fig. 1. RHEED patterns of 3C-SiC buffer layers grown on Si(111) (a, b) by RTP and (c, d) by UHVCVD process. Azimuth of (a, c) is [110], and that of (b, d) is [112].

Structure of ZnO on 3C-SiC buffered Si

Immediately after ZnO film growth, reflection high-energy electron diffraction (RHEED) images were taken. Fig. 2 shows the RHEED patterns of ZnO on the three different 3C-SiC buffered Si templates (a-c) and on a 6H-SiC single crystal (d). The growth of ZnO on hexagonal 6H-SiC is described in detail in [10]. For all substrates, the spotty RHEED patterns indicate crystalline ZnO grains which are aligned with their c-axis perpendicular to the film surface. However, because all RHEED patterns in Fig. 2 did not change by azimuthal rotation of the films, no preferential in-plane orientation of the ZnO crystallites seems to exist, although the 3C-SiC buffer layers showed a preferential in-plane orientation (compare the SiC RHEED patterns in Fig. 1). The RHEED patterns in Fig. 2 seem to originate from an overlap of all possible azimuthal directions (zone axis) of the textured grains.

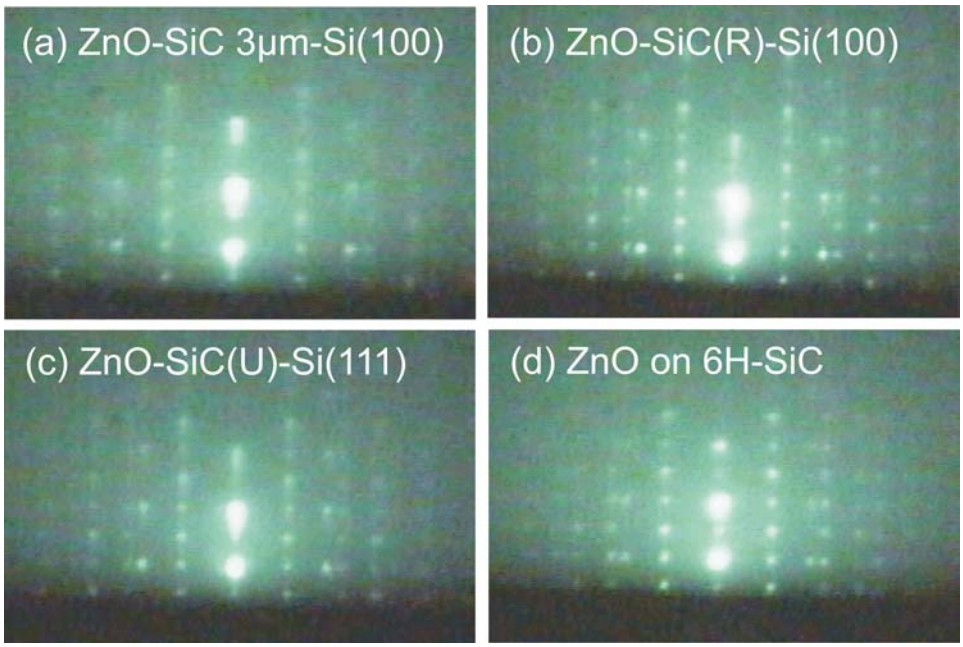

Fig. 2. RHEED patterns (30 kV) taken from ZnO films grown (a) on 3C-SiC 3µm / Si(100), (b) on 3C-SiC (RTP) / Si(100), (c) on 3C-SiC (UHVCVD) / Si(111), and (d) on a 6H-SiC single crystal. The RHEED patterns (a-d) are not sensitive to the azimuth. The crystalline ZnO grains don't show a preferential in-plane orientation.

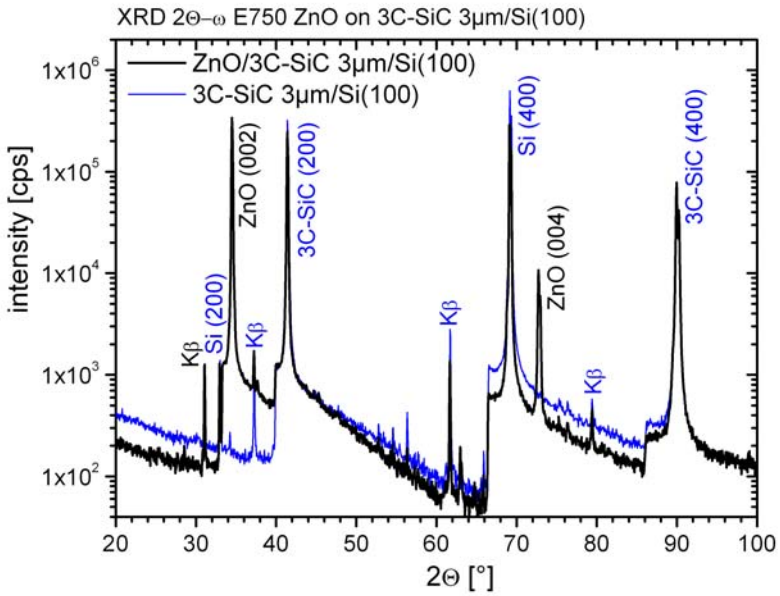

Fig. 3. XRD 2Θ–ω-scans of ZnO 600nm / 3C-SiC 3µm / Si(100) (black) and of the growth template before ZnO deposition (blue). Only peaks of c-axis textured ZnO are added.

The c-axis texture of the ZnO crystallites on the SiC growth templates is confirmed also by X-ray diffraction (XRD) 2Θ–ω-scans. We used a Philips X'pert diffractometer and copper K_α radiation (Figs. 3 - 4). In Figs. 3 and 4, only ZnO (002) and (004) peaks appear in addition to the peaks of the different growth templates. Most of the low-intensity peaks visible in the logarithmic intensity scaling can be attributed to K_β peaks. The surface morphology of a ZnO film on 3C-SiC 3µm / Si(100) is shown in the SEM images in [10] Fig. 3.

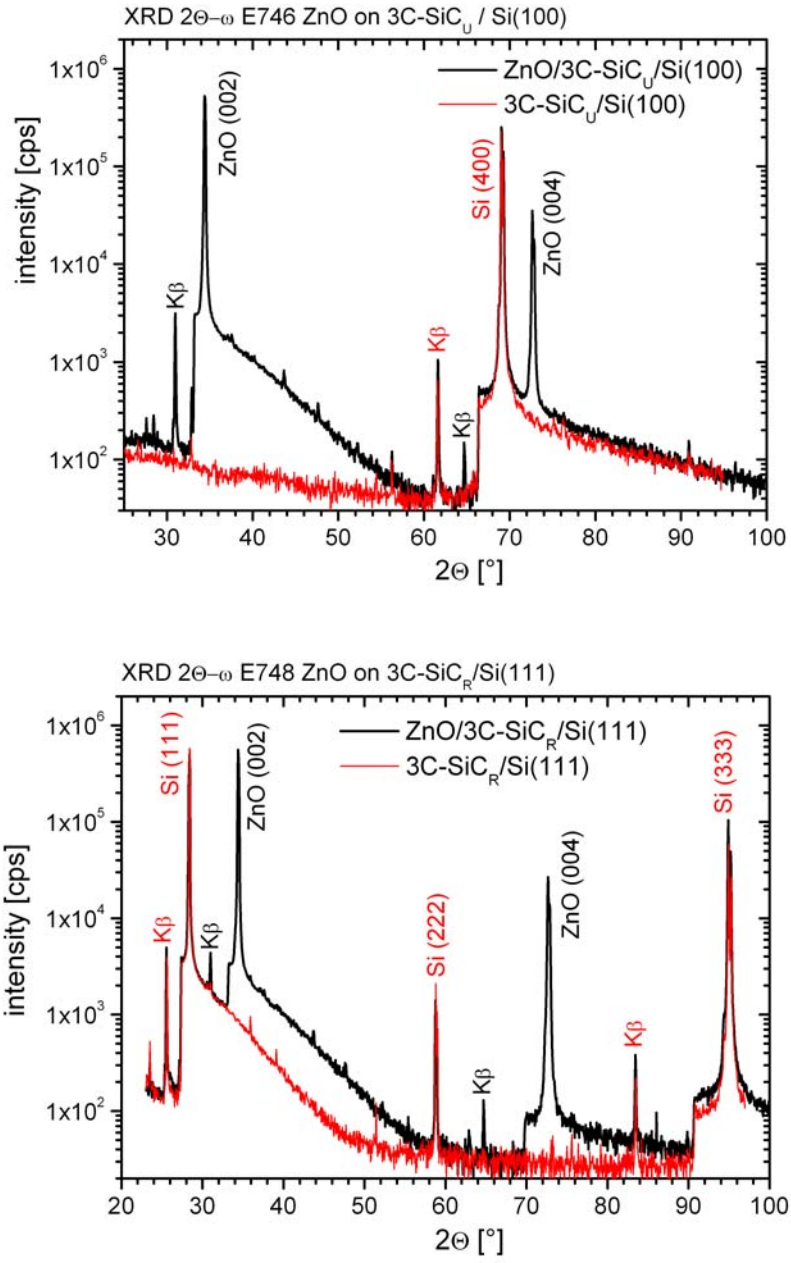

Fig. 4. XRD 2Θ–ω-scans of ZnO 600nm on 3C-SiC$_U$ / Si(100) (top) and on 3C-SiC$_R$ / Si(111) (bottom). Again the XRD patterns of the growth templates (red) are given, and only the ZnO (002) and (004) peaks of c-axis textured ZnO are added.

Photoluminescence and ellipsometry of ZnO on 3C-SiC 3µm / Si(100)

The room temperature photoluminescence (PL) of the ZnO thin films shows a dominating excitonic luminescence at 3.3 eV and the defect induced green luminescence band around 2.35 eV. Fig. 5 shows the PL spectrum of a 300 nm thin ZnO film on 3 µm 3C-SiC on Si(100). Due to the differences in the refractive indices of ZnO and SiC, strong interferences are visible. The origin of the intensity modulations in Fig. 5 was investigated by spectroscopic ellipsometry.

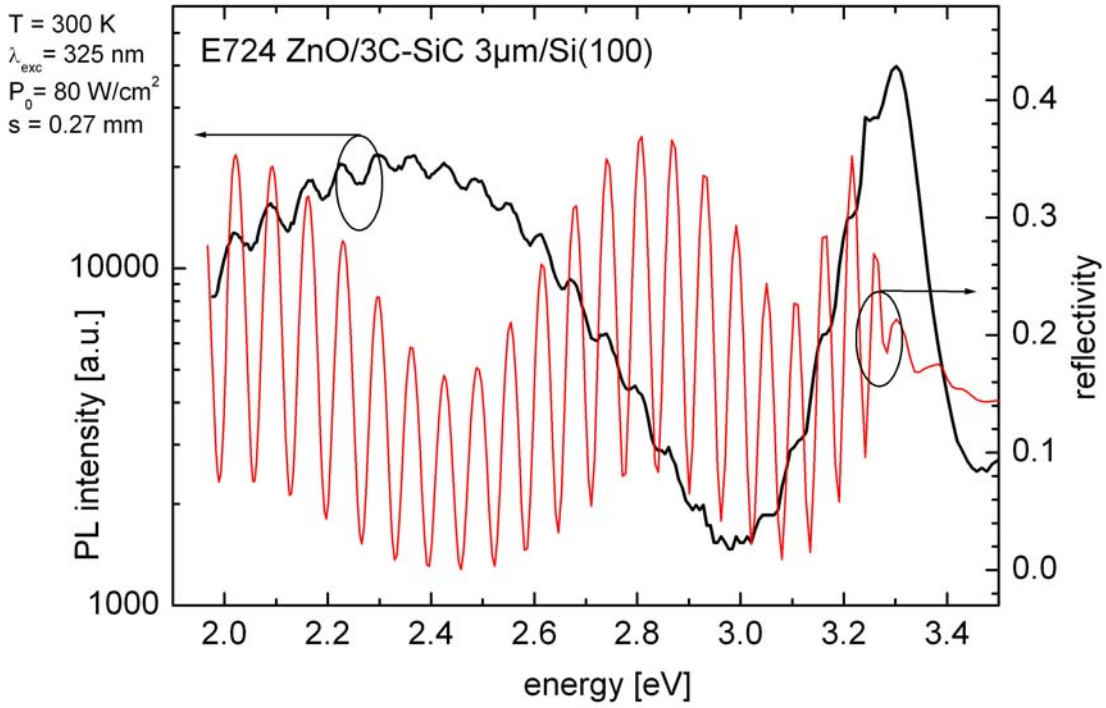

Fig. 5. PL spectrum of ZnO on 3C-SiC 3µm / Si(100) (black) and reflectivity obtained by spectroscopic ellipsometry (red). Between the interference structures observed in the PL- and reflectivity spectra, a phase shift should occur because the probe light in the PL measurement is generated in the ZnO layer, while the light in ellipsometry penetrates the sample from outside. In order to clarify the assignment of the oscillations observed in the PL spectra to thickness interferences, we have slightly varied the ellipsometric determined layer thickness of SiC (within the errors) in order to match the oscillations observed in the PL-spectra.

Due to its sensitivity to the complex optical sample response, spectroscopic ellipsometry provides a valuable tool to determine precise dielectric function spectra and layer thickness, even for thin layers [11]. We have measured spectra of the ellipsometric parameters at room temperature for photon energies between 0.75 eV and 4.5 eV and angles of incidence of 60° and 70°. For the ellipsometry data analysis, using standard multilayer calculation schemes, a four-layer-model is employed including the silicon substrate, the SiC and ZnO layers, and a thin cap layer which accounts for surface roughness. The dielectric functions of the respective materials were taken from Yao and Yan [12] (Si), Palik [13] (SiC), and Schmidt *et al.* [14] (ZnO). The thickness of the SiC and ZnO layer were found to be 3050 nm and 297 nm, respectively. From the best-fit model parameters, we have calculated the reflectivity spectra at normal incidence (Fig. 5.). Between 3.3 and 3.45 eV, features due to band-to-band transitions and exciton polarizabilities are observable. The structures below 3.3 eV are originated due to thickness interferences within the layer stack. By comparing the PL with the reflectivity spectra, we can assign the oscillations observed in the PL spectra to respective

thickness interferences of the generated light. The intensity ratios of the PL spectrum in Fig. 5 and of CL spectra are also included in the comparison in Table 1. The comparatively low intensity ratio I_{UV}/I_{VIS} could be due to the higher surface roughness of the 3 µm thick 3C-SiC film of about 8 nm average RMS on a 20 x 20 µm² AFM scan.

Photo- and cathodoluminescence of ZnO on 3C-SiC (RTP, UHVCVD) / Si

The excitation depth of the 325 nm He-Cd laser in PL is about 60 nm (at intensity 1/e), whereas the exciting electron beam in cathodoluminescence (CL) has maximum ranges in ZnO of about 250nm for 5keV and about 750nm for 10keV. The ZnO electron ranges were averaged from Kanaya-Okayama ranges for the elements Cu and Al. Therefore, by performing PL, and CL at 5 and 10 keV, we are able to sample increasing depth ranges of 300nm thick ZnO films, beginning from the surface region. Table 1 shows the intensity ratio I_{UV}/I_{VIS} of excitonic emission to green emission taken from PL spectra, and CL spectra taken at 5 and 10 keV excitation energy for 300 nm thick ZnO films on 3C-SiC buffered Si, and for comparison here also on a 6H-SiC single crystal [10]. The PL and CL spectra in Figs. 6 and 7, respectively, show clearly the dependence of luminescence emission of the 300nm ZnO films on the excitation volume. The PL spectra in Fig. 6 sample the surface region of the ZnO films only, which shows the lowest defect density as deduced from the high ratios of excitonic emission to green band emission, ranging from 2 to nearly 100 (Table 1).

With increasing excitation depth as controlled by the energy of the electron beam in CL, the intensity of green luminescence band increases considerably, as shown in Table 1 and Fig. 7. This is due to increasing defect density in the ZnO film near the interface to the growth template. The decreasing density of dislocation lines in ZnO films on sapphire from the interface to the surface and the decreasing number of misoriented grains in MgZnO films has been demonstrated recently by TEM cross sections [15].

Table 1. Intensity ratio I_{UV}/I_{VIS} of excitonic emission near 3.3 eV to green emission around 2.2 eV taken from PL, and CL at 5 and 10 keV excitation energy for 300 nm thick ZnO films on 3C-SiC buffered Si and on a 6H-SiC single crystal. See Figs. 5, 6, and 7 for the corresponding spectra. The maximum excitation depth range is given in the first line.

	I_{UV}/I_{VIS} PL, HeCd-laser 1/e: 60nm	**I_{UV}/I_{VIS} CL 5keV** range: 250 nm	**I_{UV}/I_{VIS} CL 10keV** range: 750 nm
ZnO/3C-SiC 3µ/Si(100)	1.9	0.56	0.33
ZnO/Si(111)	3.5	0.62	0.33
ZnO/3C-SiC_R/Si(100)	4.5	0.83	0.41
ZnO/3C-SiC_U/Si(111)	8.4	0.96	0.47
ZnO/3C-SiC_U/Si(100)	9.7	0.97	0.53
ZnO/6H-SiC	92	2.9	1.1

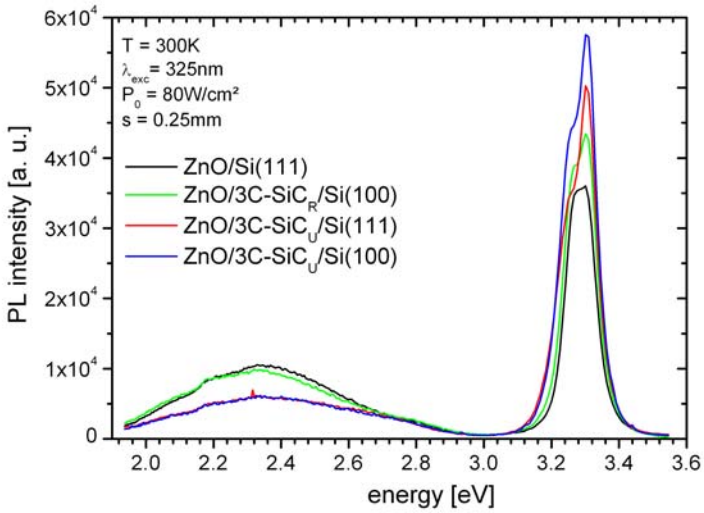

Fig. 6. Photoluminescence spectra (300K) of 300 nm thick ZnO thin films on Si and 3C-SiC-buffered Si. The 3C-SiC buffer layers were either grown by RTP or by UHVCVD process.

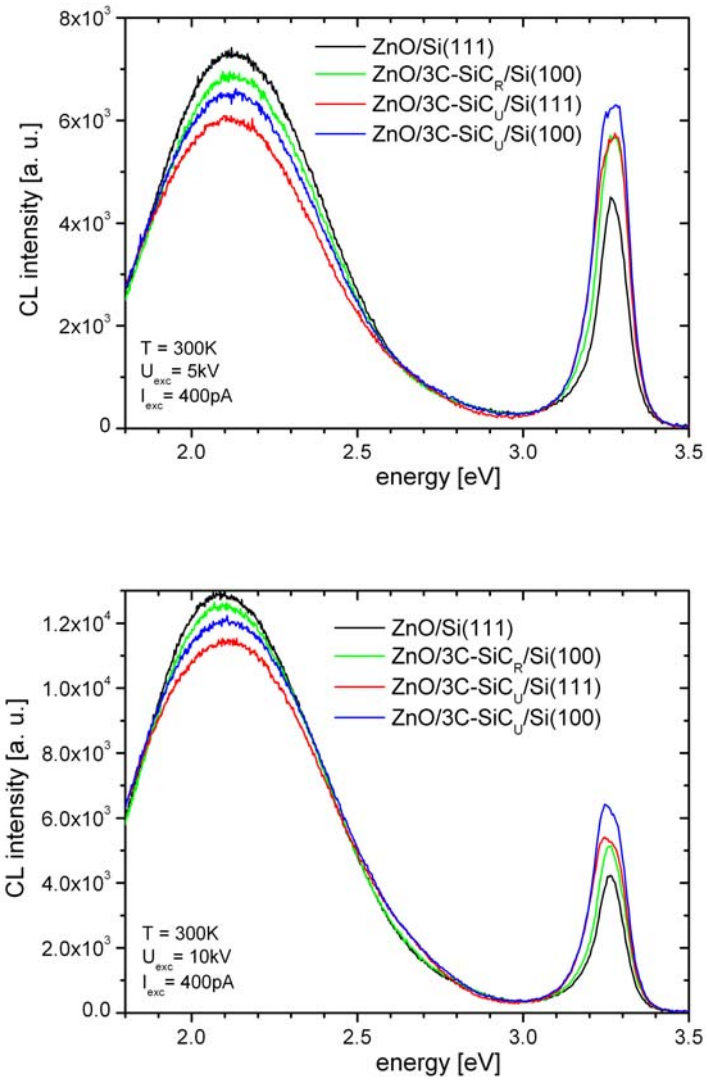

Fig. 7. Cathodoluminescence spectra (300K) taken at 5keV (top) and 10keV (bottom) of 300 nm thick ZnO thin films on Si and on 3C-SiC-buffered Si (the same as used in Fig. 6).

However, the intensity ratio I_{UV}/I_{VIS} of ZnO on Si was increased due to the insertion of thin 3C-SiC buffer layers (Table 1.). In Table 1, the samples are arranged from top to bottom with increasing optical quality. For the UHVCVD grown SiC films this effect is more pronounced than for the RTP grown SiC buffer layer, indicating a better crystalline quality of UHVCVD 3C-SiC films in all depth regions. So, the optical quality of thin ZnO films on Si is improved especially by UHVCVD grown 3C-SiC buffer layers. On 6H-SiC single crystal, the highest intensity ratios I_{UV}/I_{VIS} have been measured (Table 1 and [10] for more details), thus offering new possibilities for further improvement of the optical emission properties of ZnO thin films on the cubic and hexagonal SiC polytypes.

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Sensor applications of GaN-based solution gate field effect transistors

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Introduction

Today, GaN and the related alloys AlGaN, InGaN and AlInGaN represent a far developed material system for the application in optoelectronic devices like light emitting diodes, laser diodes and solar blind detectors for the ultraviolet (UV) spectral regime [1-4]. During the last years, metalorganic chemical vapour deposition (MOCVD) was the growth method of choice to realize layers and heterostructures with high structural quality that could satisfy the high requirements for optoelectronic applications and only recently the fabrication of UV laser diodes based on material grown by plasma assisted molecular beam epitaxy (PAMBE) has been demonstrated [5]. Due to their pyroelectric properties the group III-nitrides allow the realization of high electron mobility transistors (HEMTs) based on AlGaN/GaN heterostructures with a polarization-induced two dimensional electron gas (2DEG) at the heterointerface [6]. Due to the high sheet carrier density and the high carrier mobility at room temperature, these devices exhibit excellent properties for the application in high frequency electronics [7]. Sensor applications of the III-nitride system have been investigated only recently [8]. Whereas the high temperature stability of GaN and AlGaN has been exploited in high temperature gas sensors based on Pt:GaN Schottky diodes or HEMT-structures with a catalytic Pt-gate [9,10], their piezoelectric and piezoresistive properties have been shown to allow the realization of strain sensitive elements applicable in micromachined pressure sensors [11,12]

In recent publications we have demonstrated that the AlGaN system exhibits excellent material properties for biophysical applications, in particular the electronic properties of AlGaN/GaN HEMT structures, operated with an electrolyte gate electrode (solution gate field-effect transistors, SGFETs) suggest the utilization for the detection of biochemical processes [8,13-15]. In the present report we give an overview on earlier reported relevant material properties of AlGaN alloys and the characteristics of AlGaN/GaN SGFETs for biosensor applications.

Field-effect biosensors

Figure 1 shows a schematic of a field-effect semiconductor biosensor. In contrast to other semiconductor sensors, the response to biochemical processes is not an intrinsic material property as e.g. the generation of electron-hole pairs in photodetectors or the strain-induced resistance changes in piezoresistve sensors. Therefore, the immobilization of an adequate bio-receptor layer, which can consist of biomolecules like enzymes or proteins or of living cells is a basic requirement. The bio-receptor is needed to convert the biochemical stimulus of the analyte to a chemical or physical secondary signal that can be transformed to an electrical output by the semiconductor transducer. For the case of potentiometric sensors based on field effect transistors, charge transfer from or into the device is neglected and the secondary signal results in a change of the semiconductor surface potential which modulates the transistor current.

Whereas the action potential of living cells which are attached to the non-metallized gate area, leads to changes in the surface potential due to ion currents through specific ion channels in the cell membrane, the secondary signal of certain enzymatic reactions (e.g penicillinase, urease) can be a change in the local pH which can be measured if the surface potential of the

transistor depends on the environmental pH. In the following, both the pH-sensitivity of AlGaN/GaN SGFETs and the electrical recording of action potentials with such devices are discussed.

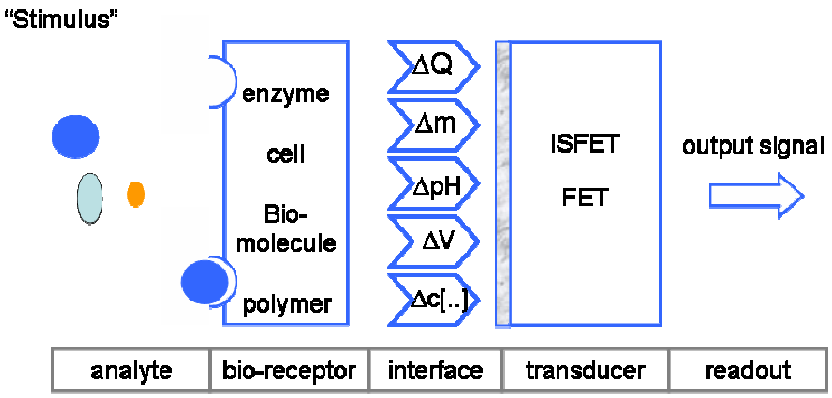

Figure 1: Schematic structure of a field-effect semi-conductor biosensor.

pH-sensitivity of AlGaN/GaN SGFETs

The response of semiconductor surfaces towards variations in the H^+-concentration can be used as a tool for cell metabolism monitoring. We have investigated the pH-sensitivity of both natively and thermally oxidized GaN surfaces on AlGaN/GaN SGFETs at a constant temperature of 23°C in a three-electrode setup. In a solution of 100mM NaCl/10mM HEPES the pH was adjusted by titration with diluted NaOH and HCl and measured with a pH-sensitive glass electrode. The pH-sensitvity of the GaN surface was measured using test devices such as shown in the inset of Figure 2. These AlGaN/GaN SGFETs consisted of a 1.5 µm undoped GaN buffer, a 25 nm AlGaN barrier with an Al-content of 20 – 30% and a 3 nm GaN cap layer. Room temperature sheet carrier concentrations and mobilities in the 2DEG obtained from Hall measurements were between $1x10^{13}$ cm^{-2} and $1.2x10^{13}$ cm^{-2} and from 1100 cm²/Vs to 1240 cm²/Vs, respectively. For the measurements, the gate potential was adjusted via the Ag/AgCl reference electrode to keep the channel current constant upon changes of the pH. In that case the pH-induced change of the surface potential is compensated by the gate potential variation. Figure 2 displays the obtained pH-sensitivities. For both GaN surfaces a linear dependence of the surface potential on the pH was found between pH 2 and pH 12. The similar slope of both curves indicates a similar pH-sensitivity of 56.6 mV/pH for the thermally oxidized and of 56.0 mV/pH for the natively oxidized surface [13]. Both values are close to the Nernstian limit of the pH response of 58.7 mV/pH. As discussed in ref. [13], the observed pH-response can be attributed to the presence of Ga-O bonds on the natively and thermally oxidized surface.

The observed pH-response can be explained in terms of the site-binding model [16] which has been applied to ion sensitive FETs (ISFETs) by Bousse and Fung [17,18]. Following this model, the Ga_xO_y layer on the surface forms hydroxyl bonds in contact with an aqueous electrolyte which are either protonated or deprotonated depending on the pH of the solution and the equilibrium constants K_b and K_a for the respective reactions [16]. These processes result in the formation of a pH-dependent surface charge. Based on our results [13] Bayer et al. have recently calculated that the surface charge of the Ga_xO_y vanishes at a point of zero charge of pH_{pzc} = 6.8, corresponding to K_a ~10^{-8} and K_b ~ 10^{-6} [19]. In contrast, the sensitivity towards other ions such as Na^+, K^+, Ca^{2+} was found to be more than one order of magnitude lower [20].

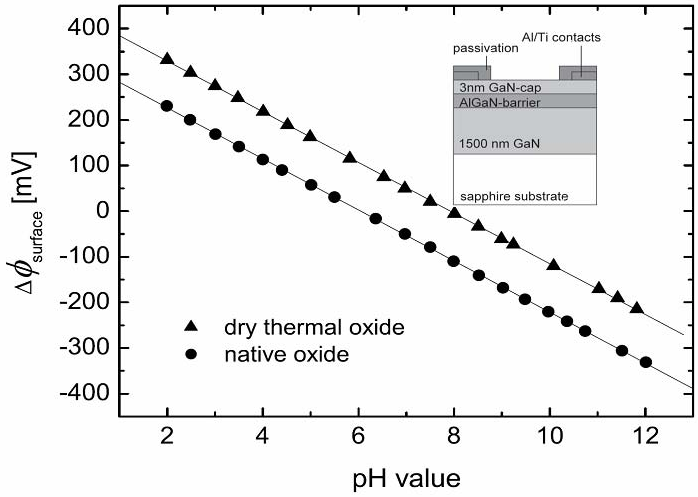

Figure 2: pH-sensitivity of natively and thermally oxidized GaN layers. The sensitivity was measured using the transistor structures shown in the inset. A linear, almost Nernstian pH-response was observed for both structures [13].

Electrical recording of cell activity with AlGaN/GaN SGFETs

Cell-transistor hybrid systems attract increasing interest for the realization of "whole cell biosensors" employing the combination of biochemical recognition with electronic devices. In this type of biosensors either the electrical cell activity or cell metabolism can be monitored. These sensors benefit from a high sensitivity and selectivity of specific receptors in the cellular membrane and are suitable for different applications such as environmental monitoring or the detection of toxins [21, 22]. Such systems require an electronic transducer which is suitable for long-term measurements under physiological conditions. The application of field effect transistor (FET) arrays, first reported by Bergveld [23] for the detection of muscle fiber activity, has been proven to be a promising approach combining high sensitivity with possible integration into specific electronic circuits. However, the main drawbacks of standard silicon technology - the long-term drift due to the poor electrochemical stability of SiO_2-surfaces upon exposure to electrolyte solutions [24] as well as the high noise level in standard MOS-transistors due defect states ate the Si/SiO_2 interface [25] still have to be solved. The group III-nitride alloys as a wide bandgap semiconductor system have recently been demonstrated to be chemically stable under physiological conditions and non-toxic to living cells [13] and the applicability of AlGaN/GaN SGFETs for field effect sensors in electrolyte solutions has been described in the preceeding paragraph. Here we show that AlGaN/GaN SGFET arrays are an excellent tool for electrical recording of cell activity [14].

The inset of Figure 3 shows AlGaN/GaN SGFET arrays with 4x4 active transistors that were used for the experiments (the transistor structure is the same as described before). Operated in a three-electrode setup, the channel current was controlled via an electrolytic gate contact leading to a maximum transconductance at a gate voltage of V_{GS} = -1.8 V as it is shown in Figure 3.

For the detection of cell activity cardiac myocytes were cultivated on the device surface according to the protocol reported in [14]. After culturing the cells were spontaneously beating at a stable frequency and their electrical activity was recorded by measuring changes of the junction potential V_J in the cleft between cell and transistor gate. As displayed in Figure 4, the monitored action potentials were 100 ms-150 ms in duration and the recorded frequency was stable over several minutes.

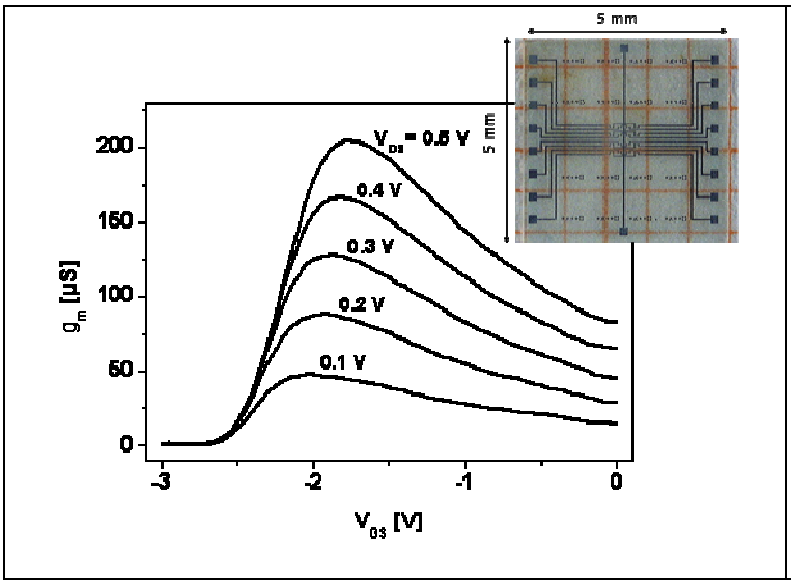

Figure 3: Transconductance of a single element of an AlGaN/GaN SGFET array for different source-drain voltages V_{DS}. The whole 4x4 SGFET array is shown in the inset [15] .

The action potentials are usually generated by ionic fluxes of sodium, potassium and calcium across the membrane. The fast rise of the action potential is triggered by an inward flux of sodium ions, whereas an outward flux of potassium repolarizes the cell membrane. In the data shown here [15], the signal shapes seem to be dominated by the potassium signal in contrast to other results based on silicon MOS-structures [26,27]. The origin of this behaviour is still being clarified.

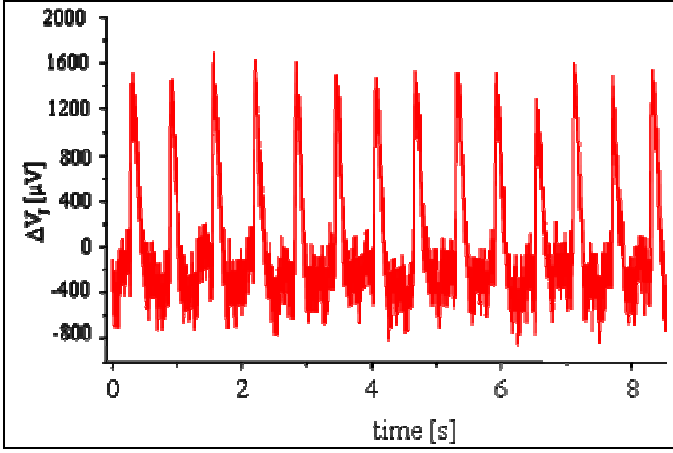

Figure 4: Signal of cardiac myocyte action potential recorded with an AlGaN/GaN SGFET [15].

Conclusion

In conclusion we have summarized the properties of AlGaN/GaN SGFETs for the application as field-effect biosensors operating in electrolyte solutions under physiological conditions. Thermally and natively oxidized GaN surfaces exhibit an almost Nernstian sensitivity towards pH changes which can be sensitively measured with AlGaN/GaN heterostructure field-effect transistors. The high chemical stability of the device surface allows the operation as “whole-cell” biosensors and electrical recording of cell activity has been demonstrated. Novel sensors for detection of biomolecular recognition processes can be realized after biochemical functionalization of the gate surface.

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